Thermal characterization and reliability testing of high power electronics

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February 1
Outline

- Problem definition
- Measurement approach
- Boundary conditions
- Single and multi-chip driving
- Effect of TIM quality and reliability
- Lessons learned and conclusion
Junction-to-case thermal resistance

- Junction-to-case metric is originally designed for devices with nearly 1D heat flow
  \[ R_{Thjc} = \Delta T_{J-C} = \frac{T_J - T_C}{P} \]

- In realistic structures 3D heat flow can be expected

- Despite these well known problems this metric is well used in data sheets for back-of-the-envelope calculations

- For most of TO-type power packages this approach yields reasonable results

- In best conditions chip and package area are comparable

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The transient dual interface method for $R_{thJC}$

- Original idea from 2005, **standard JESD51-14 published in November 2010**
- Change of thermal interface quality at the ‘case’ surface
- Divergence point in measured structure functions: ‘case’ surface

### Measurement
- Change the quality of the thermal interface
- Measurement of 2 setups (2x3 min), **structure functions**

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**SEMI-THERM 2005 Best Paper Award**

**methodology for single-chip and lateral or stacked multi-chip structures**

**SEMI-THERM 21, March 15 – 17, 2005, San José, California**

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High accuracy and repeatability

- This type of $R_{thJC}$ measurement provides high repeatability
  - the continuous measurement of thermal transients is very reliable and highly repeatable if the setup is not changed
  - repeatability is also high among different samples
  - structure functions are derived from the transients by a mathematically well defined numerical procedure, thus, resulting structure functions are also highly repeatable
Problems addressed

- The standardized way to measure the $R_{thJC}$ value is the transient dual-interface method (see JEDEC JESD 51-14)
- The diverging point of the structure functions or the derivatives of the measured transients give good and reproducible results, but ...

- The boundary condition changes the heat-flow path, and may influence the steady-state heat distribution
- If the cooling surface area is significantly larger than the chip the diverging point is hard to find – parallel running
- What happens in case of multiply heat sources?
Problems addressed

- Structure functions corresponding to a 7PM-GA package, wet and dry conditions

![Image of 7PM-GA package](image_url)

**Package Code: 7PM-GA**

![Internal Circuit Diagram](image_url)

**T3Ster Master: cumulative structure function(s)**

- FMG2G150US60_10A_T25 - Ch. 0
- FMG2G150US60_10A_T25_MY - Ch. 0

<table>
<thead>
<tr>
<th>Rth [K/W]</th>
<th>Cth [W/K]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.06339</td>
<td>0.101006</td>
</tr>
<tr>
<td>49.6756</td>
<td></td>
</tr>
</tbody>
</table>
Experimental approach

- To investigate these issues, Samsung engineers designed special test structures.
- IGBT modules were investigated with large package surfaced area (140mm*70mm, 12 chips).

Courtesy of: Shan Gao, Jongman Kim Seogmoon Choi
Central R&D Institute, Samsung Electro-Mechanics, Korea
Experimental approach

- Many thermal patterns were investigated — Both driving one pair only and all modules were tested
- For easier interpretation of the results different samples were used with slight modifications

<table>
<thead>
<tr>
<th>Sample Id.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>Standard module, reference to all others</td>
</tr>
<tr>
<td>S2</td>
<td>Module with half copper thickness</td>
</tr>
<tr>
<td>S3</td>
<td>Module with 75% aluminum thickness</td>
</tr>
<tr>
<td>S4</td>
<td>Combination of S2 and S3 cases</td>
</tr>
<tr>
<td>S5-1</td>
<td>Sample after 300 cycle reliability test</td>
</tr>
<tr>
<td>S5-2</td>
<td>Sample after 500 cycle reliability test</td>
</tr>
</tbody>
</table>
Electric connections

- Measurements carried out with the **T3Ster** thermal transient tester and its high power add-on
- Each pair was connected in the popular MOS diode arrangement
  - Gates are connected to the collector at each IGBT
  - Two pole device with app. quadratic characteristic
- 8 A heating current and 500 mA sensing current
  - 55 W for a single pair and 320 W to the whole device
  - Forward voltage was calibrated as a TSP in a water bath
Boundary conditions

- Very low $R_{th}$ can be expected
  - Designed for kW power
  - No ceramics or mylar can be used
  - Overheating should be avoided

- Wet and dry conditions were used

- Still the $R_{th}$ of the TIM is the same as the package’s

- 300 kPa controlled pressure makes results repeatable
Boundary conditions

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- 300 kPa controlled pressure makes results repeatable
Junction-to-case identification

- Differential structure functions are compared
- Inflexion point is sought – around 0.08 K/W
- Parallel running of the structure functions
Steady-state heat distribution

- **Wet case**
  - $dT=10^\circ\text{C}$

- **Dry case**
  - $dT=15^\circ\text{C}$
Obviously the measured $R_{th}$ should be different in both cases.

Re-scaled by the number of heaters:
- $R_{th}=0.36/6=0.06$ K/W
- Proves that the spreading cones overlap
- So underestimation

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Results at different geometries (Cu)

- Single and multi chip driving
- As heat fills up the total copper layer in both cases, the 2:1 and 6:1 relations are well seen
- Far regions are identical

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Results at different geometries (Al)

- Originally the thickness of S3 is 75% of S1’s.
- The thermal resistance is not significantly influenced.
- The measured curves run parallel, app 80% ratio.

![Graph showing thermal performance comparison between 100% Al and 75% Al structures.](image)
Different die attach qualities

- Cyclical reliability tests ensured a decrease in the Cu area compared to the reference sample.
Different die attach qualities

- Surprisingly the results are practically identical as on the original sample
- The copper is differently filled up, however the heat catches up in the aluminum
- The large volume of the aluminum blurs the effect
- Quality problems at the thermal interface material region may be more important
INVESTIGATING THE TIM PERFORMANCE IN-SITU
Power cycling testing of TIM-s

- Junction temperature change of a transistor may be a suitable failure criteria
- The probe is the heatflow — The TIM has to be a part of the heat-flow path
- A TO-220 packaged transistor is the heater and sensor element — To resemble real application
- The transistor is pushed against a cold-plate with constant force
- The power is supplied by a high power accessory of the transient tester
Measurement conditions

- App. 20 W power was applied
- Each sample was exposed to 2500 cycles and the thermal transients were captured after each cycle
- The temperature change of the transistor for a given power step was used as a sensor output
- The cold-plate was temperature stabilized at 40 °C
- Highest junction temperature was around 110 °C
- The thermal transients were captured by the T3Ster with high resolution in both time and temperature (1 µs and 0.01 °C)
- 2500 cycles lasted for app. 13 hours
Test results

- Most of the materials showed a slight improvement in $R_{th}$.

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Trends in Rth

- The temperature difference between a very early time and the last measured point

![Graph showing Rth tendency of TIM 1 material](image-url)
Verification of the results

- The junction temperature change may be influenced by many factors:
  - Die attach or other mechanical failures
  - Change in the pressing force
  - Changes of the TIM material

- The location of the diverging points in the structure functions corresponds to the failure mechanism
Verification with structure functions

T3Ster Master: cumulative structure function(s)

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High temperature storage tests

- Test environment defined
  - Selected TIM materials mounted on aluminum cold-plates
  - Temperature storage tests at 150 °C
  - Standard clamps used to press the transistors to the cold-plate
**Resulting curves**

- Junction-to-ambient thermal resistance measurements were carried out on each sample
  - Measurement time takes 4 minutes per sample
  - Measured resistances versus storage time plotted for each sample
  - Stability requirement: standard deviation of the results < 5% from the fourth measurement onwards

![Graph showing thermal resistance over storage time]

**Measurement results**

- Reference point
- Fourth measurement

**Standard dev**: 0.48%
Conclusions

- The dual interface method is a fast and reproducible way to measure the junction-to-case thermal resistance.
- If the area of the chip and package are similar, the results are easy to interpret.
- If the area of the heat-spreader is much larger than the area of the chip, some part of the heat-flow becomes lateral – parallel running STF.
- Poor heat conductance towards the cooling mount causes lateral spreading in the base.
- Measurements pointed out that the heat-flow is first vertical than it becomes lateral.
Conclusions II

- In modules containing many devices the spreading resembles the vertical case again if the spreading cones overlap.
- The cooling is always better when driving less chips because the heat-spreader is more effective.
- The effects caused by the DA problem were cancelled out by the large area aluminum base.
- It is also very important to measure the TIM performance in case of such packages as the TIM thermal resistance may be comparable to $R_{thJC}$.
- Using structure functions the performance of the TIM can be monitored on-line.