Challenges and new approaches for power module’s next generation packaging technology
Challenges and new approaches for power modules
Content

- MV power packages review
  - design
  - reliability issues & wear-out
  - robustness issues
- New requirements & SiC system case study
- Packaging research needs
MV power module design
MV power module design
High power IGBT modules

- IGBT insulated
- Traction and industrial drives applications
- AlSiC baseplate, AlN DCB
- Isolation up to 10.2kV$_{\text{rms}}$
- 1.7 - 6.5kV, up to 3600A
- Other modules up to 1.7kV: EconoPak, PrimePack, SkiM, SkiiP, ...

- IGBT press pack
- Transmission & distribution applications with series connections & redundancy
- Individual spring contacts for uniform pressure
- Short-circuit failure mode (SCFM) capability
- 2.5 and 4.5kV, up to 2000A
- Other press packs: IGBT capsules
MV power module design
Thyristor press packs (bipolar discrete)

- Discrete bipolar devices (Thyristors, Diodes) remain the most economic solution for many high-power applications (T&D, industry)
- Available up to 8.5kV and up to 6.1kA for 6” devices
- Press Pack design features
  - pressure loaded (~15MPa) dry & bonded contacts with Mo strain buffers
  - double-side cooling
  - inherent SCFM
  - hermetic housing
  - low-inductance gate connection (IGCT)
  - clearance and creepage distances up to 10kV
Power package reliability issues
Power package reliability issues
Introduction

- «Reliability issues»: Wear-out and degradation at the end of the hazard function bathtub curve
- General root cause for power package wear-out (ever present power electronic stressors):
  - temperature cycling
  - high temperature storage
- Review of
  - wear-out failure mode
  - wear-out failure mechanism
  - typical lifetime values
  - demonstrated and proposed improvement strategies

- Note: references are documented at the end of the presentation.
## Review on power package failure mechanisms

**Chip-related wear-out under thermal cycling**

### Failure mode

<table>
<thead>
<tr>
<th>Failure mode</th>
<th>Illustration</th>
<th>Mechanisms</th>
<th>Typ. values</th>
<th>Improvements</th>
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</table>
| Wirebond lift-off & heel crack        | ![Image](image1.png) | Bond wire fracture or lift-off due to wire flexural fatigue and thermomechanical (TM) stress | $N_f = 100k, T_{cycle} = 40-100^\circ C, t_{cycle} = 5s$ [2] | - Polymeric coating  
- Ribbon  
- Cu & Al coated Cu  
- Metal foil buffer  
- Mo top plate  
- Cu clips & flex foil  
- Galvanic Cu | ![Image](image2.png) |
| Die attach fatigue                    | ![Image](image3.png) | TM stress/strain field during cycling → solder fracture & delamination       | $N_f = 60k, T_{cycle} = 40-100^\circ C, t_{cycle} = 60s$ [2] | - $x\;10-100\;\Delta T = 60^\circ C$  
for LTB [4]  
- $x\;10-100\;\Delta T = 60^\circ C$  
for TLP [4]  
- Au/Ge, /Si, /Sn [5] | ![Image](image4.png) |
| Al metallization reconstruction       | ![Image](image5.png) | Al/Si CTE mismatch → stress beyond elastic limits → Al gets porous (grain bound. deformation) → increase in losses | $T_j >> 110^\circ C$ [1], 2.5 x resistivity increase after 50k pulses, 5ms, 250A/cm² [7] | - Ni coating [6]  
- Polyimide [1]  
- Mechanically stronger metallization | ![Image](image6.png) |
| Dry contact fretting corrosion (Thyristor) | ![Image](image7.png) | Al/Mo resistance incr. by breaking oxide films → hot spots, current filamentation & breakdown | $N_f = 50k, T_{cycle} = 30 - 120^\circ C, t_{cycle} = 5s$ | - Surface plating and interface materials  
(Rh, Ro, Ag, …)  
- Wafer bonding  
(LTB, Si/Al brazing) | ![Image](image8.png) |
## Review on power package failure mechanisms

### Substrate-related wear-out under thermal cycling

<table>
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<tr>
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| Substrate bond large area solder crack and fatigue | ![Image](Sn5Sb.png) | Same mechanism as die attach (can be more stress due to larger lateral dimension) | $N_f = 30k$, $T_{cycle} = 20-80^\circ C$, $t_{cycle} > 1h \ [2]$ | - Avoid too thin solder by spacers  
- SnSb solder (solid sol. str.),  
- SAC solders (precipitation str.) | ![Image](Sn5Sb.png) |
| Substrate & chip brittle crack            | ![Image](Si3N4.png) | - High TM stress ind. chip & substr. cracks → breakdown, lift-off  
- Cracks below US welding of terminals | $N_f = 500$, $-50 – 190^\circ C$  
DBC AlN/Cu \[8\] | $Si_3N_4$ DBC superior to AlN and $Al_2O_3$ \[8\] | ![Image](Si3N4.png) |
| Power terminal lift-off                   | ![Image](FlexibleTerminal.png) | CTE mismatch and pull-force lead to terminal solder crack & delamination | (Not known to authors) | - Stress relief (flexible terminal)  
- Ultrasonic welding | ![Image](FlexibleTerminal.png) |
| TIM dry-out and pump-out                 | ![Image](PolymerMatrix.png) | Polymer matrix gets fluid at high-T, filler remains (dry-out), TIM pushed out by thermal movements (pump-out) | (Not known to authors) | Optimized bow, gels, foils, pre-applied phase change materials, carbons, liquid metal, integr. cooler | ![Image](PolymerMatrix.png) |
Power package robustness issues
Power package robustness issues
Introduction

- «Robustness issues»: Issues due to insufficient margin against stresses under various operation conditions.
- Considered root causes for package robustness failure
  - voltage loads & field stresses
  - switching transients
  - surge currents
- Review of
  - failure mechanism
  - typical withstand value
  - demonstrated and proposed improvement strategies
### Review on power package robustness issues

**Insulation**

<table>
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<tr>
<th>Issue</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Partial discharges at substrate metallization edges</td>
<td><img src="10" alt="Image" /></td>
<td>Surface discharges along gel interfaces &amp; internal discharges in voids</td>
<td>10.2/6.9/5.1kV test for traction applications (6.5kV IGBT)</td>
<td>- High-strength layer</td>
<td><img src="11" alt="Image" /></td>
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<tr>
<td></td>
<td></td>
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<td></td>
<td>- Field grading (cap., res., nonlinear)</td>
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<td></td>
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<td>- Etching of braze protrusions</td>
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<tr>
<td>JT insulation &amp; interface leakage currents</td>
<td><img src="12" alt="Image" /></td>
<td>- Humidity enhanced JT degradation (oxidation, charges, delamination) [12]</td>
<td>- 6.5kV, ~1.5mm</td>
<td>Passivation layers to saturate dangling bonds and to drain trapped charges (SIPOS, DLC)</td>
<td><img src="12" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Insufficient JT cooling for Thyristor</td>
<td>- 8.5kV PCT, ~2mm</td>
<td></td>
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<tr>
<td>High-T encapsulation withstand</td>
<td><img src="10" alt="Image" /></td>
<td>Gel degradation, ruptures and integrity (hardness, oxidation, weight loss)</td>
<td>Silicone gel: ≤ ~175°C</td>
<td>- New gels up to 225°C [13]</td>
<td><img src="14" alt="Image" /></td>
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<td>- Tg &gt; 250°C mold compounds [14]</td>
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<td></td>
<td></td>
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<td></td>
<td>- Conformal coatings (eg., Parylene, PI)</td>
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## Review on power package robustness issues

### Switching transients

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| Induced over-voltages & ringing by commutation loop stray inductance | ![Illustration](image1) | $\Delta U = L_s \dot{I}$ leads to device over-voltages ($\rightarrow$ de-rating) and to resonances ($\rightarrow$ EMC issues & losses) | 2D layouts today: $L_s = 10$-$50\text{nH}$ | - Snubbers & RC/RL damping of oscil.  
- Parallel commutation cells (HBs) with strip-line interconnections  
- SoC, SiP, chip in polymer & 3D integration, eg. [15] | ![Illustration](image2) |
| Uneven current sharing | ![Illustration](image3) | Losses, asynchron. & oscillations by induced voltage noise on gate due to cross coupling and imbalance due to impedance mismatch | 2D layouts today: $\sim 1\text{V/nH}_{GE}$ per 1kA/$\mu$s | - Auxiliary emitter  
- Symmetric substrate impedance, busbar, and terminal design  
- Low-$L_s$ strip-line gate & power circuit [18] | ![Illustration](image4) |
| Unwanted leakage currents by $dU/dt$ | ![Illustration](image5) | $\Delta I = C_s \dot{U}$ leads to EMC compliance issues and leakage losses | 2D layouts today: $\sim 10\text{V/ns}$ | - Low-permittivity insulation  
- 3D concepts with minimum footprint | ![Illustration](image6) |
## Review on power package robustness issues

### Surge current and end-of-life

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</table>
| Surge current (device active over-current in fwd direct.) | ![Image](image1.png) | Device metal. & w/b over-heating by inrush currents, fault currents and short-term operation points | HiPak IGBT: x 8 In, 10ms  
StakPak IGBT: x 16 In, 10ms  
Thyristor: x 15 In, 10ms | - IGBT: Thick metal., Cu w/b, planar emitter contacts with improved $Z_{th}$  
- Thyristor: Improved $Z_{th}$ via bonding | ![Image](image2.png) |
| EoL SCFM (device failed, needs to support $I_{nom}$ for series connections) | ![Image](image3.png) | Wirebond melting, evaporation & arcing | Blocking failure of wirebonded 100A chip leads to arcing at ~1kA, 10ms | - IGBT: StakPak SCFM formation, 2kA: 10 ms, ~10J, ~0.1mΩ  
- Thyristor: Low ohmic SC (liquid Si channel) | ![Image](image4.png) |
| EoL explosion withstand of over-currents (eg. parallel connections) | ![Image](image5.png) | Massive local over-current in blocking direction leads to device evaporation, arcing & explosion. | - IGBT StakPak: x 20 In, 10ms  
- Thyristor: > x 10 In, 10ms | - Pressure contacts  
- External explosion proof boxes [24]  
- Arc protection by package internal shields (Thyristor)  
- Fuses | ![Image](image6.png) |
New requirements and power module implications
New requirements & power module implications
Trends towards higher package performance

- Higher current & loss density
  - Reduce costs, weight & volume
- Higher switching transients
  - WBG devices
  - Shrink magnetics by higher switching frequency
- Higher package E-field stresses
  - WBG devices with up to 10 x critical field (SiC)
  - Shrinked packages for low parasitics and reduced costs
- Higher load cycle reliability
  - Exploit max. Tj for load-cycle intensive applications (e.g., traction)
  - WBG high-T operation
- Higher surge and EoL withstand
  - Increasing power ratings in T&D
- Withstand against new environmental stressors
  - New applications off-shore, outdoor, on-vehicle, subsea, etc.
New requirements & power module implications
SiC cases study: f varied, $T_j = 120^\circ$C

- 1kV, 200kW, 3p-2L inverter optimized for cost & efficiency under variation of package design (chip area, # chips, # substrates, heat sink) by statistical optimization approach.

- For the given converter system, SiC costs need to drop by factor ~4 to a cost/mm² ratio of SiC/Si ~13 (switch) and ~7 (diode) to reach cost parity at 20kHz (w/o any shrinked magnetics!).

- Efficiency will be 2% pts higher, heatsink volume/cost will be 3 x lower, and reliability will be similar ($T_j = 120^\circ$C).
New requirements & power module implications
SiC case study: $T_j$ varied, $f = 16$kHz

- SiC operational cost & volume benefit saturate at $T_j \sim 150$-$180^\circ$C (since SiC efficiency also drops with $T_j$)
- 3 x lower cooler volume and 2% higher efficiency pts. stay constant across the investigated $T_j$ range.
- But - reliability drops by factor 50 by changing from $T_j = 120$ to $180^\circ$C.
- **For the given converter system, high-T operation > 200$^\circ$C is not recommended for the MOSFET** (SiC bipolar devices might perform differently).
Conclusions: Packaging research needs
# Challenges and new approaches for power modules

## Research needs

<table>
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<tr>
<th>Continuous improvement</th>
<th>Si IGBT Power Module</th>
<th>Si Thyristor Press Pack</th>
<th>SiC Packages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bonding: TLP process robustness &amp; large area bonding, LTB low cost approaches &amp; further reduced p &amp; T</td>
<td>6-inch devices: Large area bonding, symmetric current distribution, low-inductance gate control</td>
<td>Resonances: technology to damp and synchronize critical resonances &amp; transients</td>
<td></td>
</tr>
<tr>
<td><strong>Topside</strong>: Planar emitter bond &amp; metallization for improved reliability, surge current &amp; cooling; improved JT passivation</td>
<td>Dry contacts: Fretting corrosion lifetime models and optimization of materials &amp; platings</td>
<td>Encapsulation materials and coatings for $T_j = 175 - 200^\circ$C</td>
<td></td>
</tr>
</tbody>
</table>

| Innovation, breakthrough | Topside SCFM: Low-cost emitter contact / IGBT module with SCFM capability | Low-cost: Plastic housings in combination with novel passivation and planar JT approaches | Hard switching: 3D integr. designs & materials for conflicting requirements on Ls, Cs, insulation, current capability, cooling, reliability and low-cost assembly. |
Challenges and new approaches for power modules

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- Samuel Hartmann
Challenges and new approaches for power modules

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