Optimized Electrical and Thermal Layout of 1700V 450A Power Module Through Virtual Prototyping

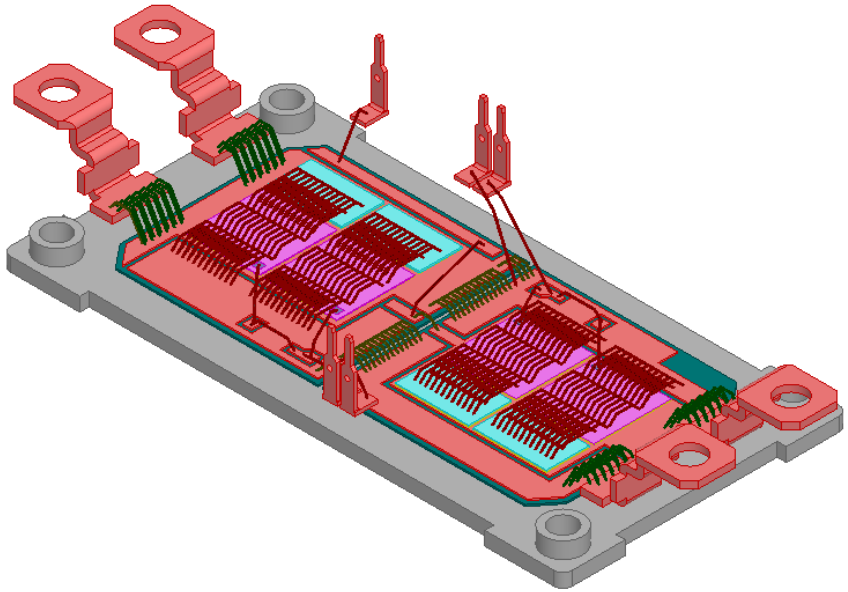
Leonel Soberano, IMI
Jean Marc Renard, IMI
Mathieu Grenier, IMI
Philippe Marquet, IMI
Cherie Sasan, IMI
Sven Matthias, ABB

<Nov. 8, 2018>

Outline

- Introduction
- Virtual Prototyping Strategy
  - Methodology
  - Design Evaluation
  - Chips and SPICE Model
- Simulation set-up & Results
  - Thermal Impact
  - Parasitics
  - Switching Behavior
- Experiment & Discussion
  - Impact on Substrate
  - Measurement
- Conclusion

Introduction: The 1700V 450A IGBT Power Module

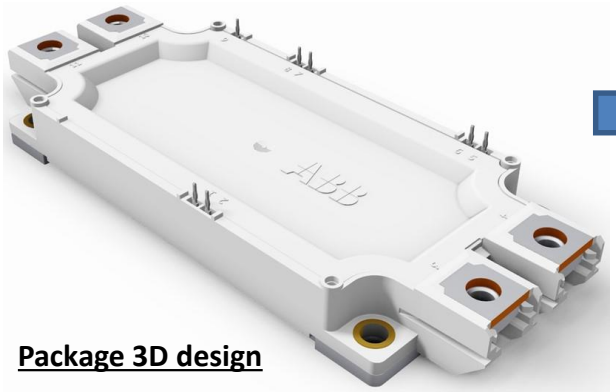


- Evaluate thermal performance
- Include package parasitics in IGBT module performance
- Find balance current distribution
- Find switching currents for power dissipation

Picture: From ABB's Lopak1

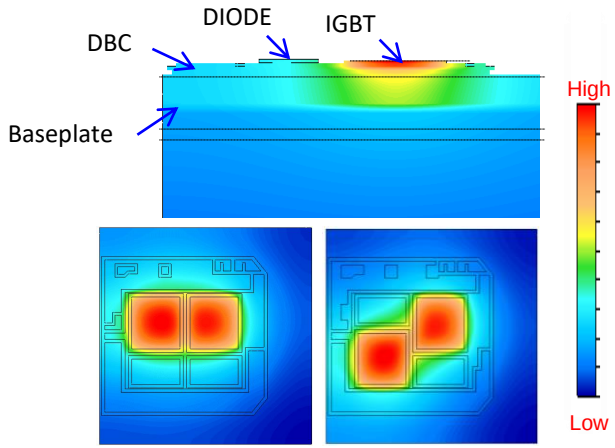
Virtual Prototyping Strategy

Virtual Prototyping Flow

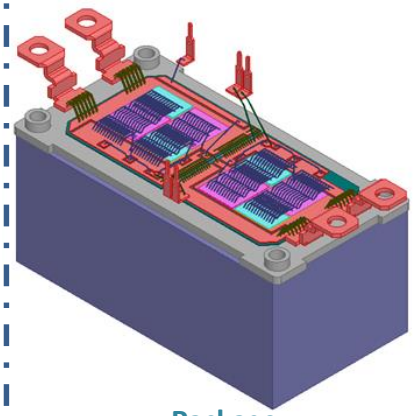


Package 3D design

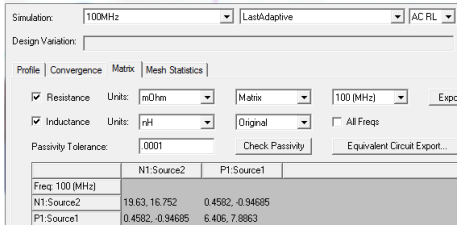
Thermal Simulation



- 3D concept
- Thermal Simulation
- Package Parasitics
- Electrical Analysis



Package Parasitic Extraction

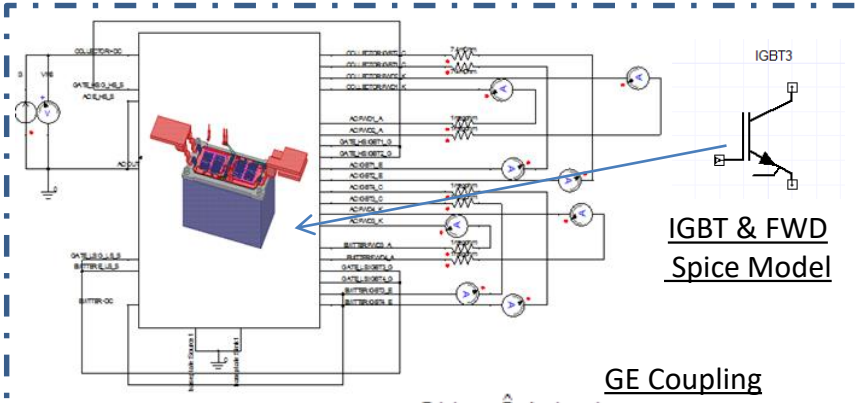


Resistance

$$R = \frac{P}{I_{rms}^2} = \frac{2P}{I_{peak}^2} \qquad \begin{bmatrix} \Delta V_1 \\ \Delta V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Inductance

$$L_{nn} = \int_V \vec{A}_n(\vec{x}) \cdot \vec{J}_n(\vec{x})\, dV$$



IGBT & FWD Spice Model

GE Coupling

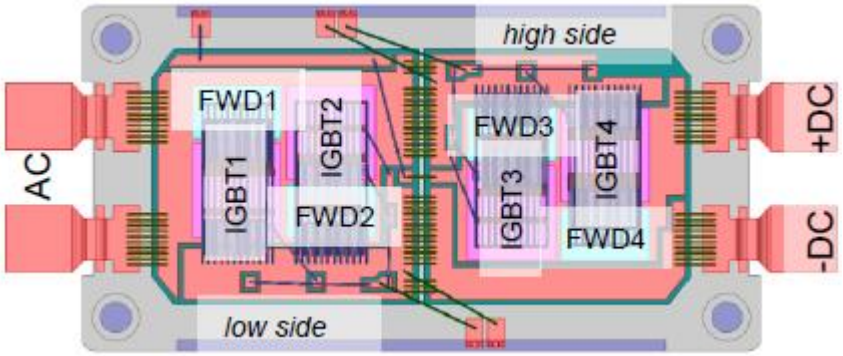
$$I(t) = \hat{I}\sin(\omega t)$$

$$V_{GE,x} = R_x \hat{I}\sin(\omega t) + K_x \omega \hat{I}\cos(\omega t)$$

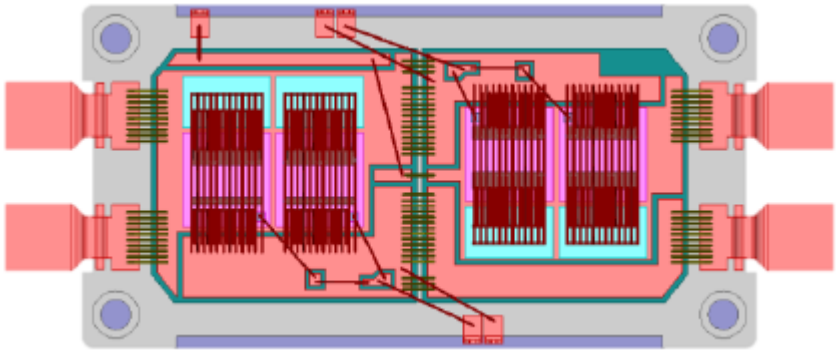
Electrical Analysis

Design Evaluation

Concept 1

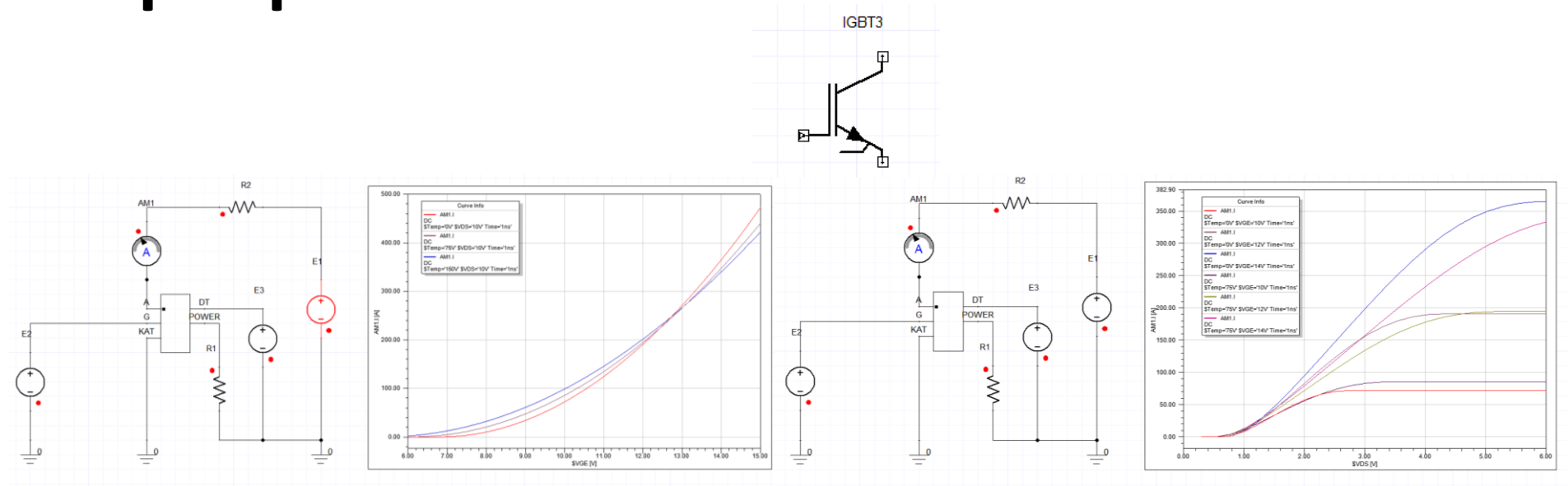


Concept 2



- The LoPak1 module was conceived
  - two possible layout configurations for the IGBTs and FWDs
    - 1st design (concept 1) features an alternating topology of the IGBT and diode
    - 2nd design (concept 2) a parallel topology was implemented

Chips Spice Model



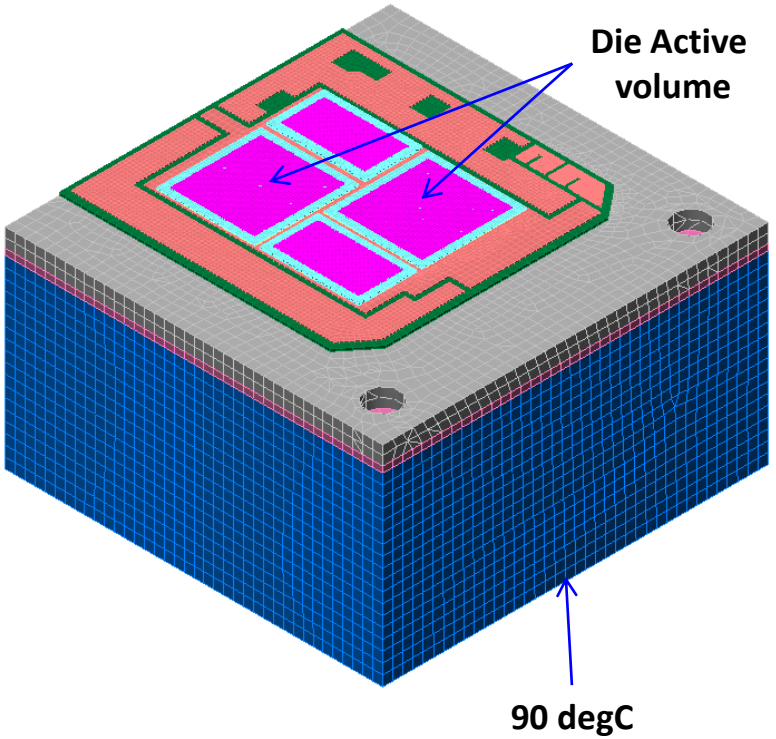
- Compact model was created and tuned to match the die characteristics
- Accurate models of the semiconductors are needed to achieve a good circuit simulation

Simulation set-up & Results

Thermal Impact

The module layout has to be checked for its thermal distribution & thermal resistance

Boundary conditions

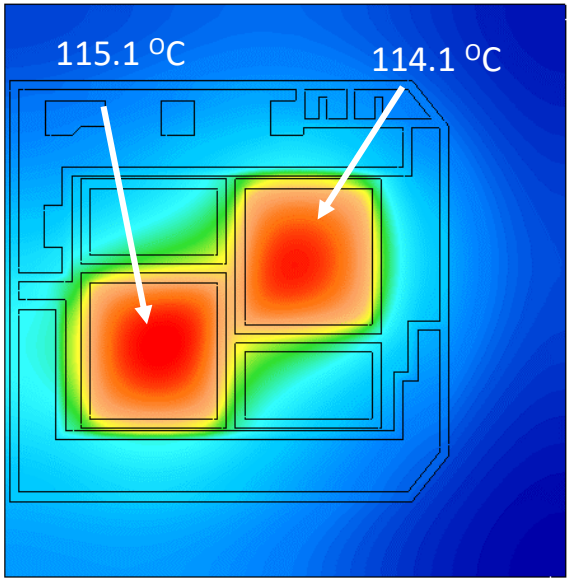


Materials Mechanical dimension

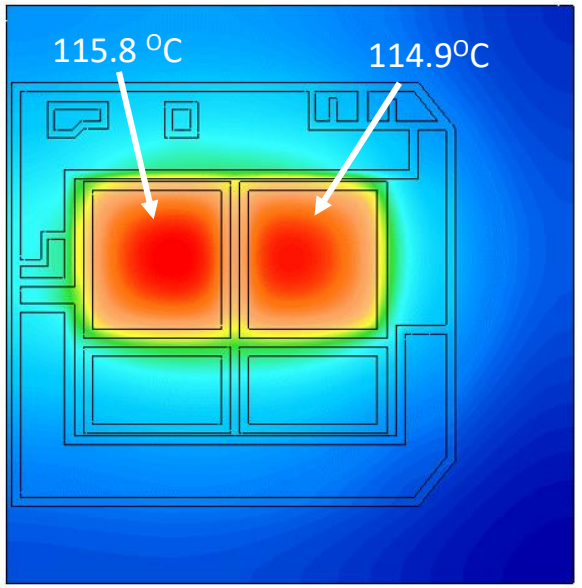
Material	Dimension (mm)	Thickness (mm)
IGBT chip	15.9X16.9	0.19
IGBT Active	13.9X14.9	0.060
FWD chip	15.9X9.30	0.390
FWD Active	13.9X7.30	0.130
Chip Solder	-	0.075
Copper Trace	-	0.300
Ceramic	-	0.380
Substrate Solder	-	0.130
Baseplate	-	3.00
TIM	-	0.100
Heatsink	-	30

Thermal Impact

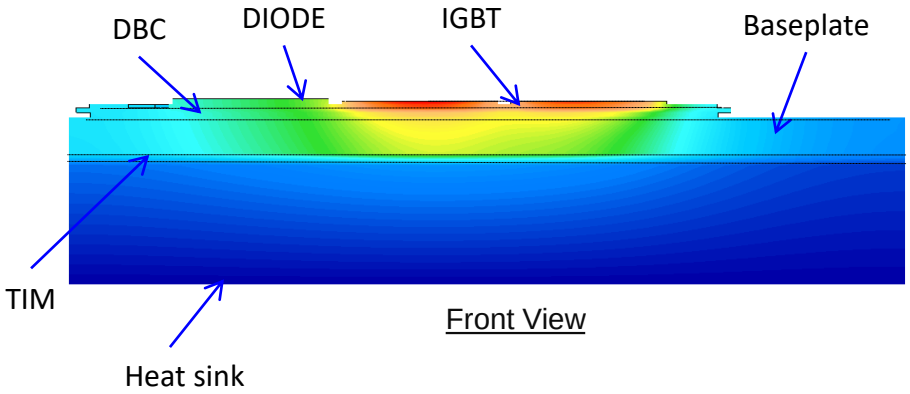
Version 1



Version 2



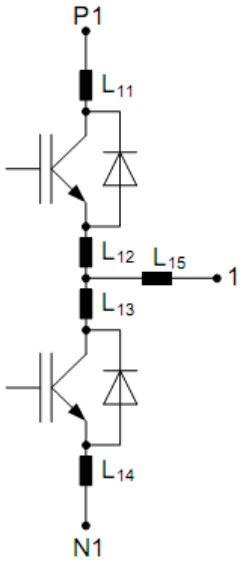
Version 1 supports a little lower junction temp and 3% lower R_{TH}



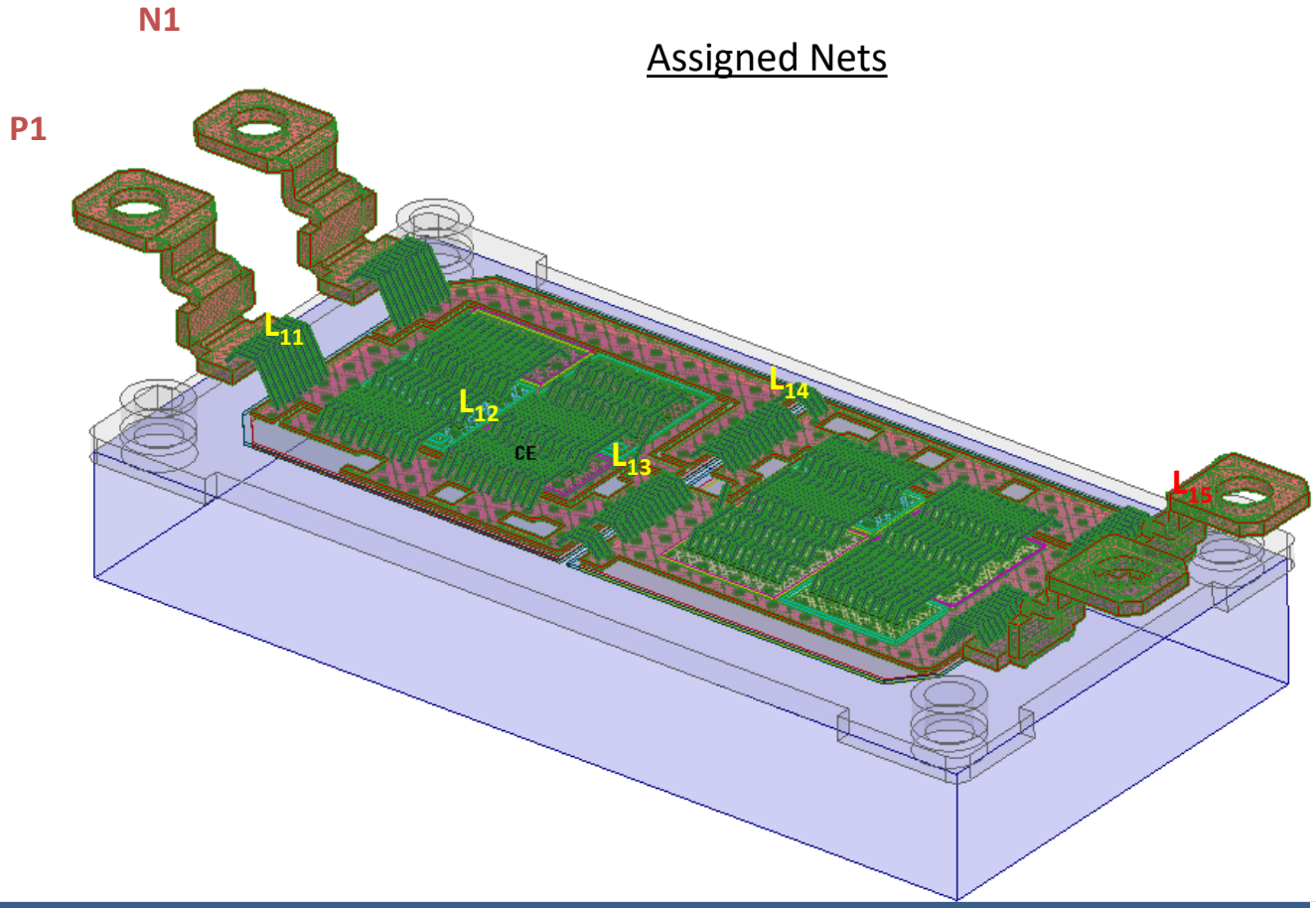
Parasitic Impact

Extracting parameters is straightforward as the nets are automatically assigned

Schematic Diagram



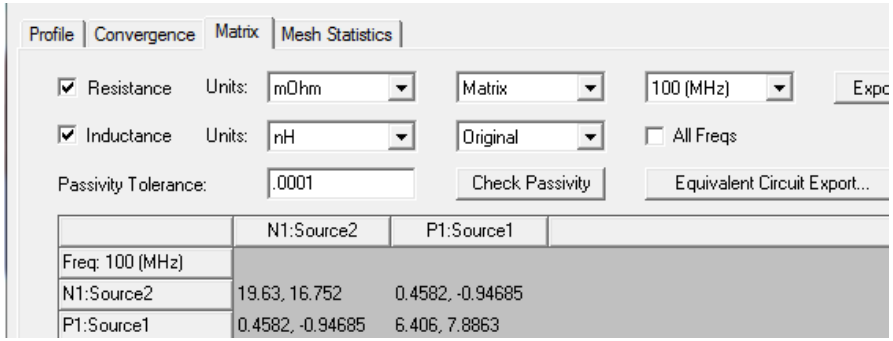
Assigned Nets

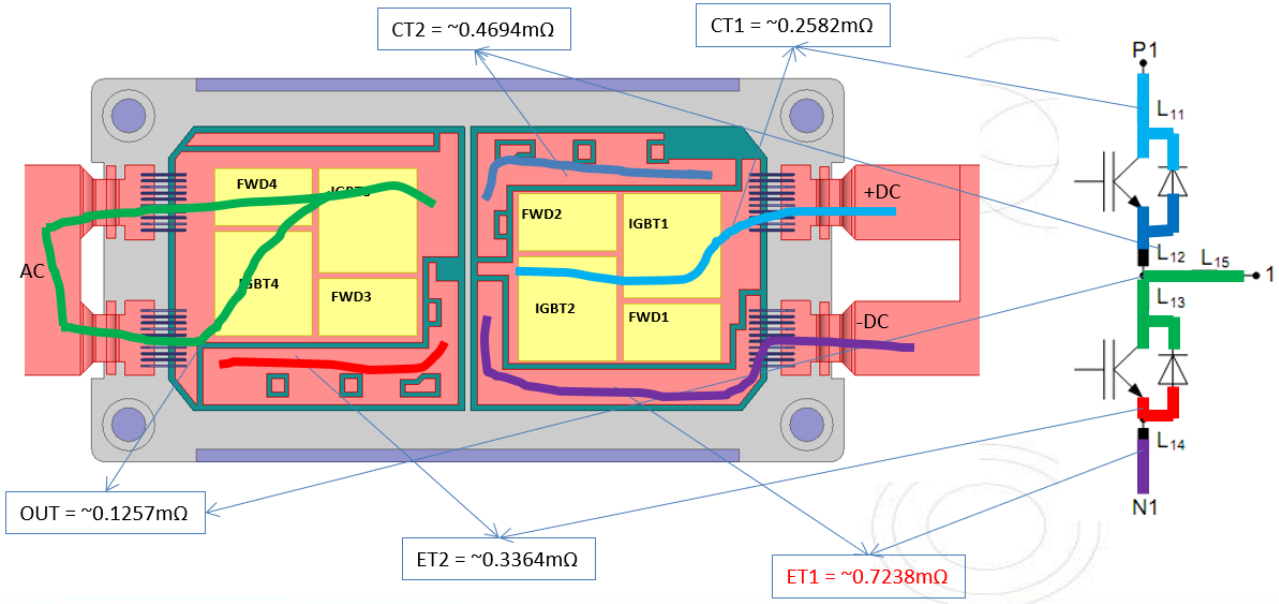


Parasitic Impact

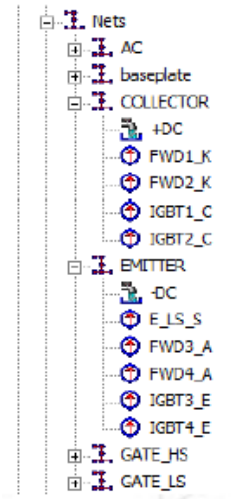
Output is composed of RLC matrices at certain frequencies

RL Matrix



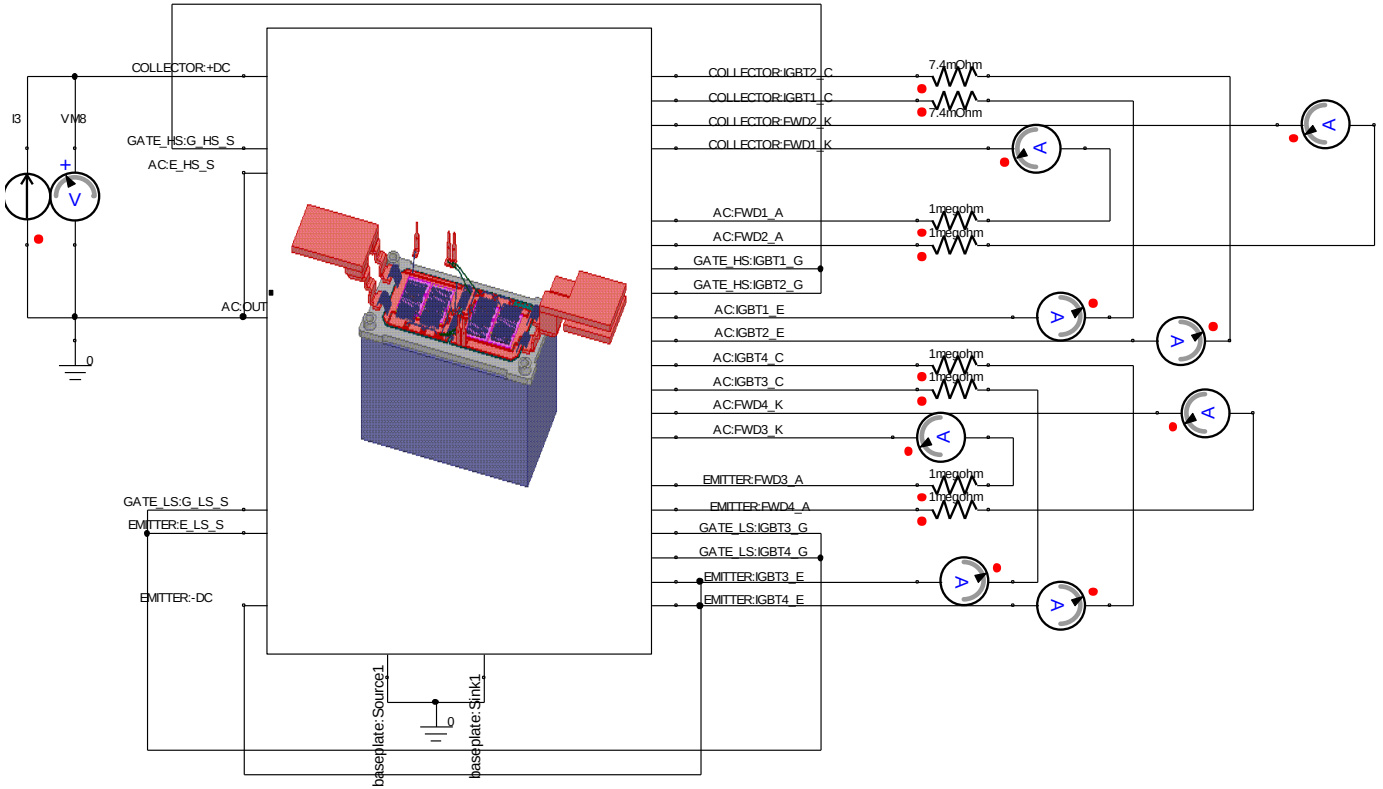


Conducting Nets



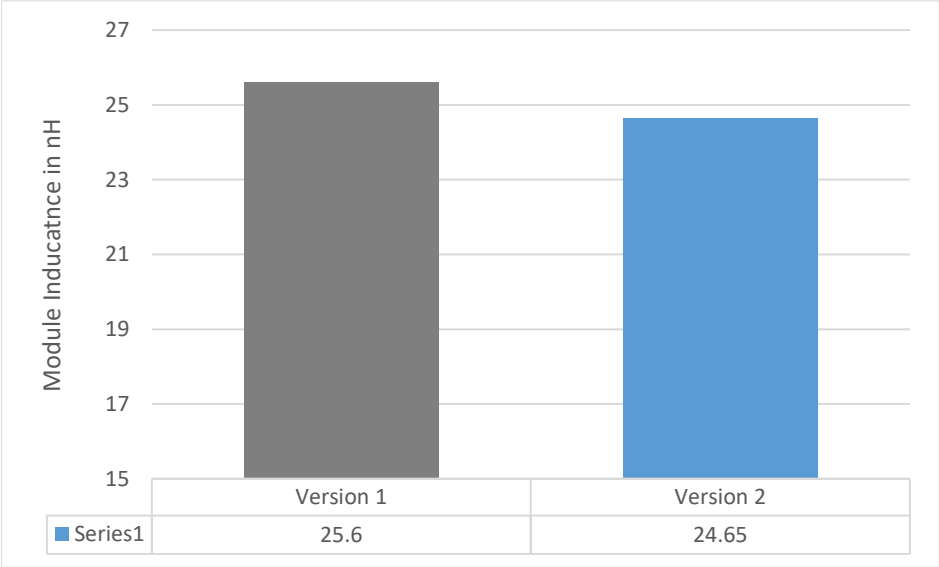
Parasitic - Integration

Using the result of lumped elements [RLC] to SPICE circuit simulator

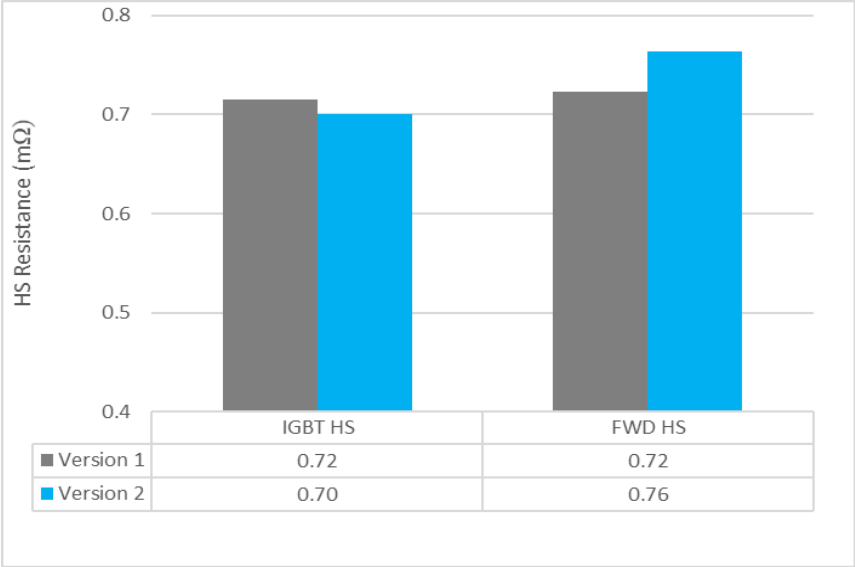


System Simulation – Module Resistance & Inductance

Module Inductance in nH



Module Resistance in mΩ

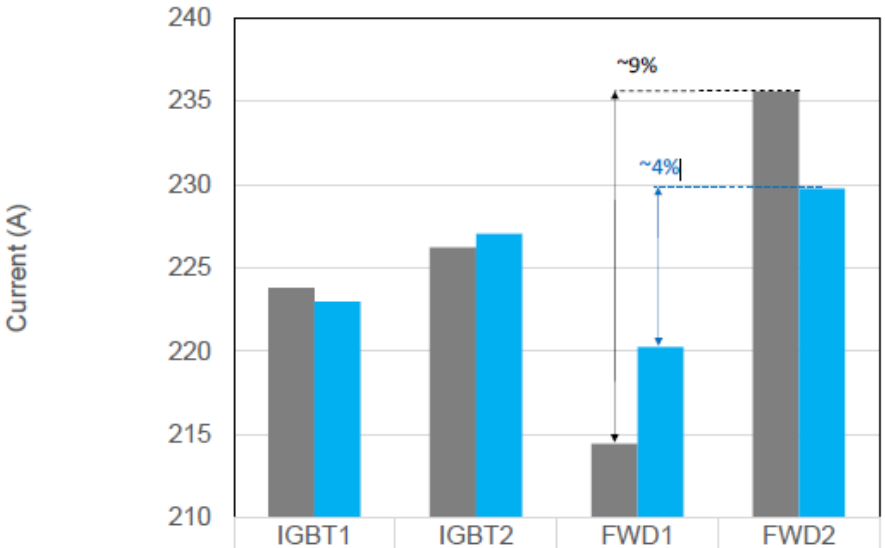


The parasitic extraction confirms:

- Both layout versions do not impact the inductance of the module of about 25nH
- the resistance of around 1mOhm

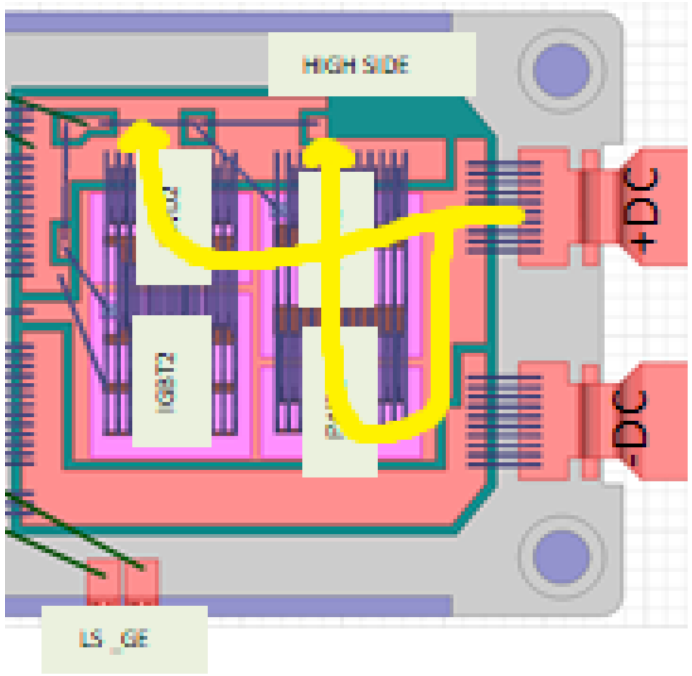
Parasitic Impact – Current Sharing

Current Sharing



	IGBT1	IGBT2	FWD1	FWD2
HS_VERSION 1	224	226	214	236
HS_VERSION 2	223	227	220	230

Current Flow

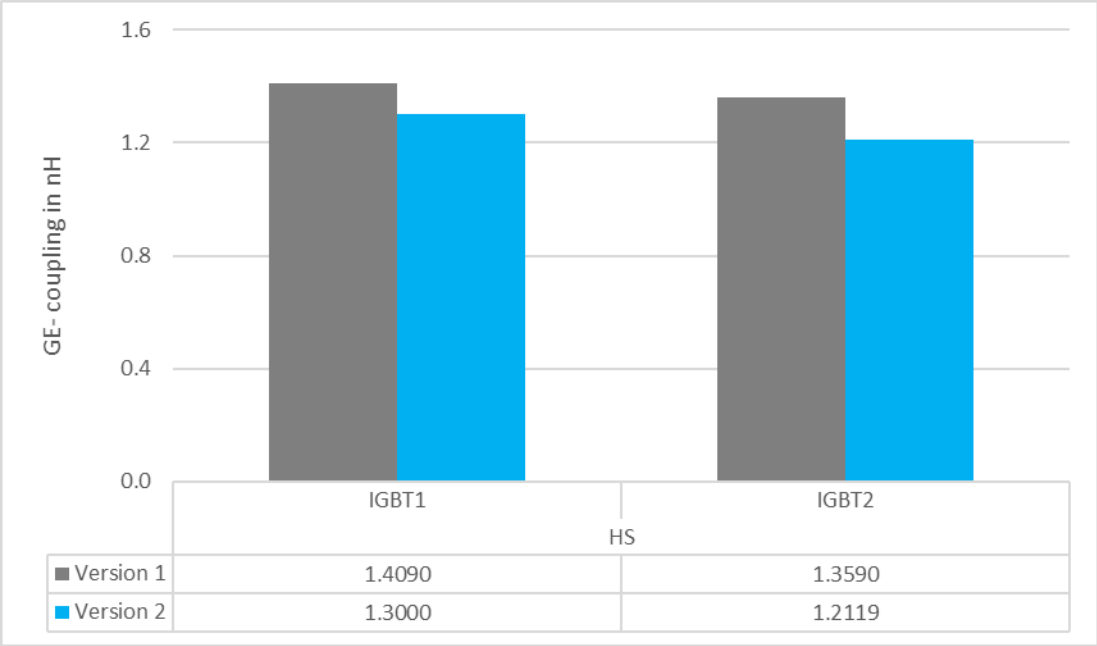


The static current sharing shows significant imbalance:

- For IGBT's are almost equal
- Free-wheeling diodes reaches 22A[version1]
- A similar result in the static current sharing for LS for both version

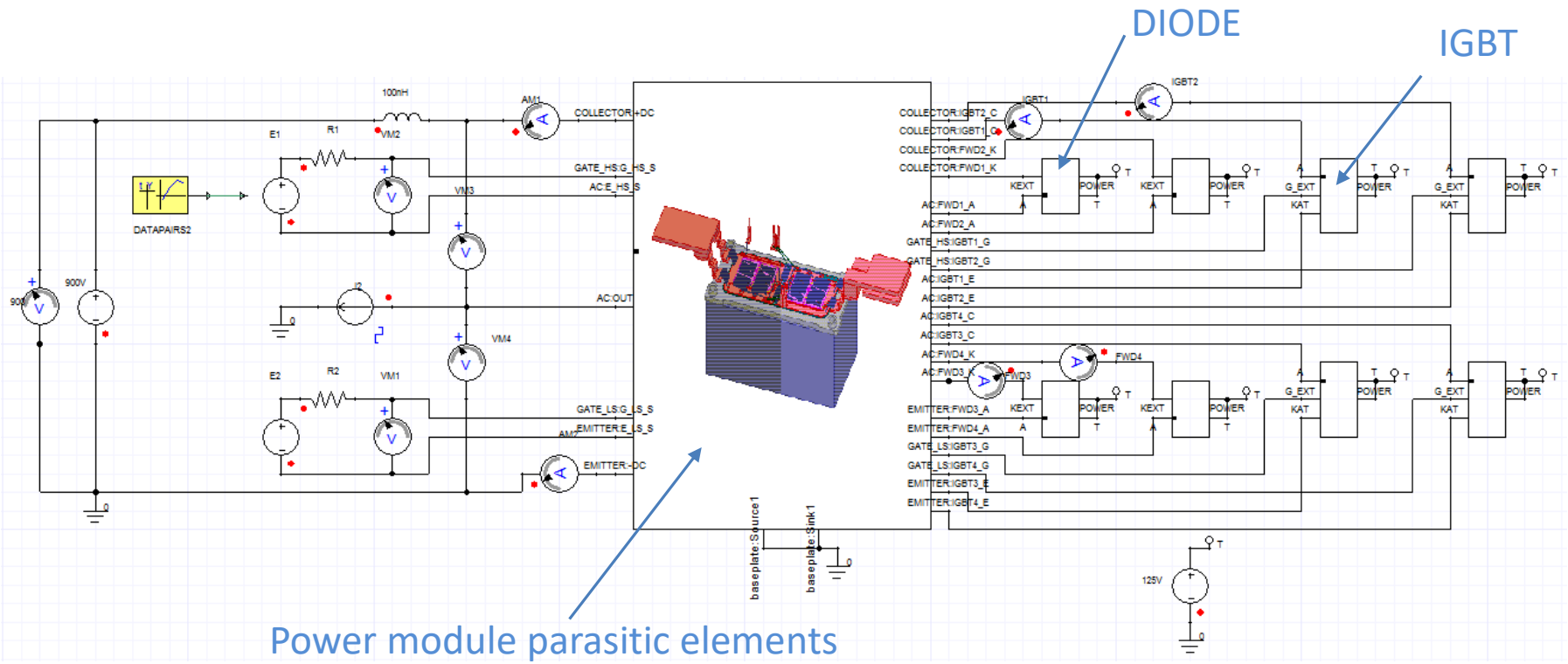
System Simulation – GE Coupling

HS Switch GE Coupling



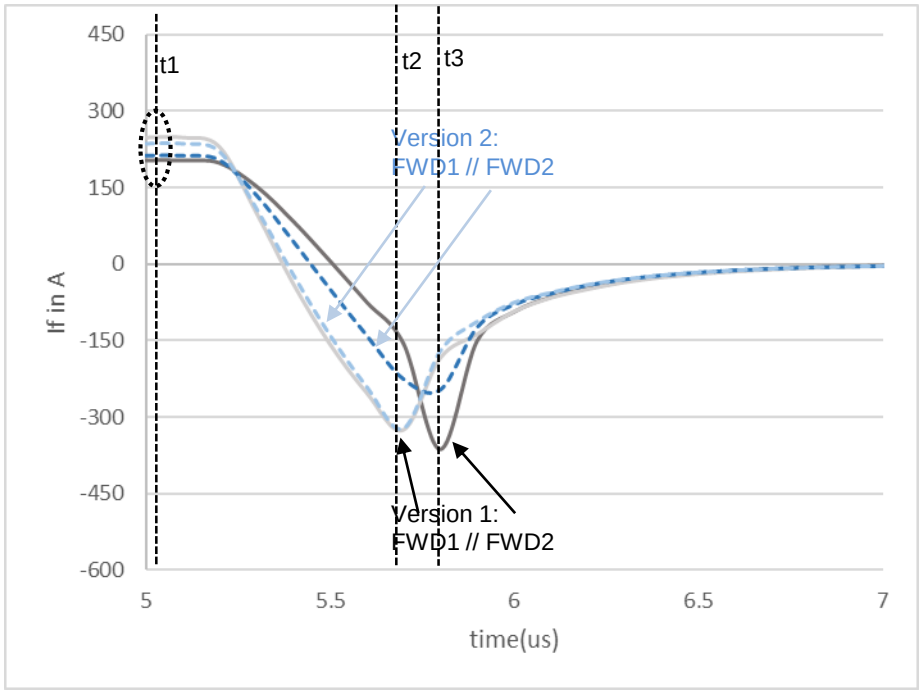
- Gate-emitter coupling of version 2 is lower – affect switching speed

System Simulation

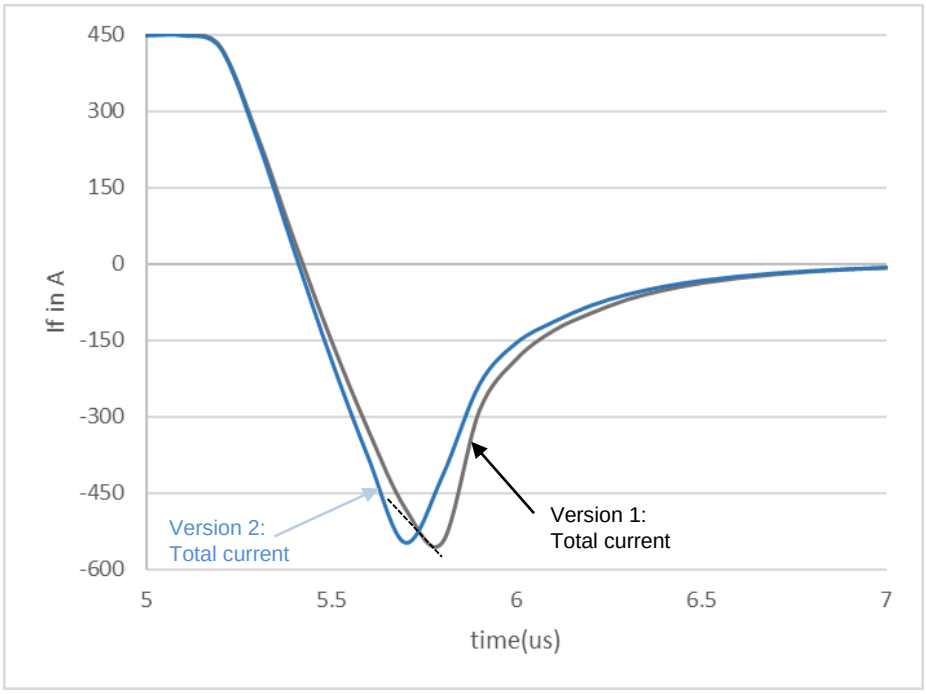


- SPICE models reflecting the chip-properties and the full simulation of a dynamic double-pulse test

System Simulation – Switching



Individual Current Though Diode

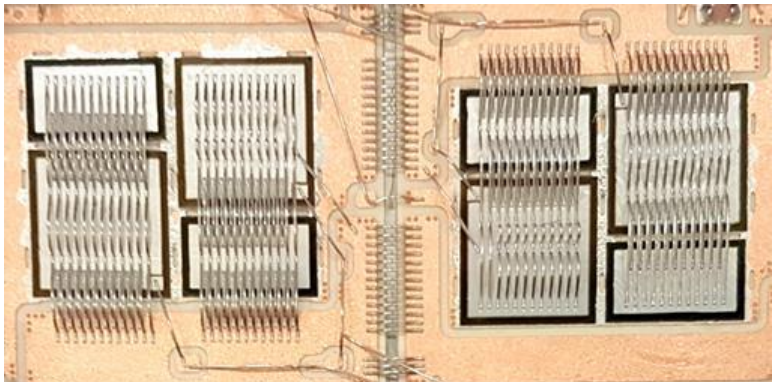


Total Current – Sum of FWD 1&2 Both Versions

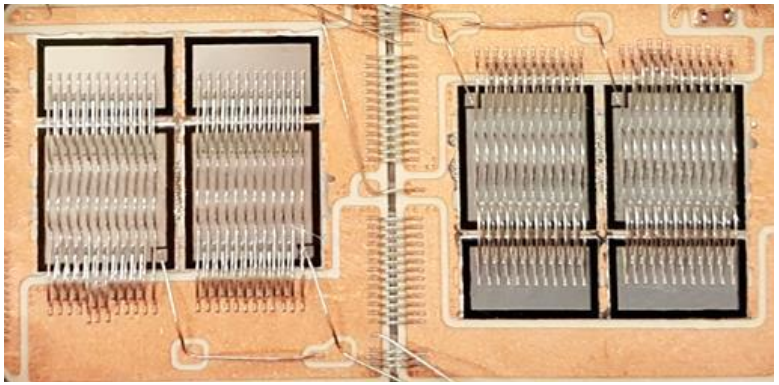
Experiment & Discussion

Impact on Substrate Layout

Version 1 - Actual



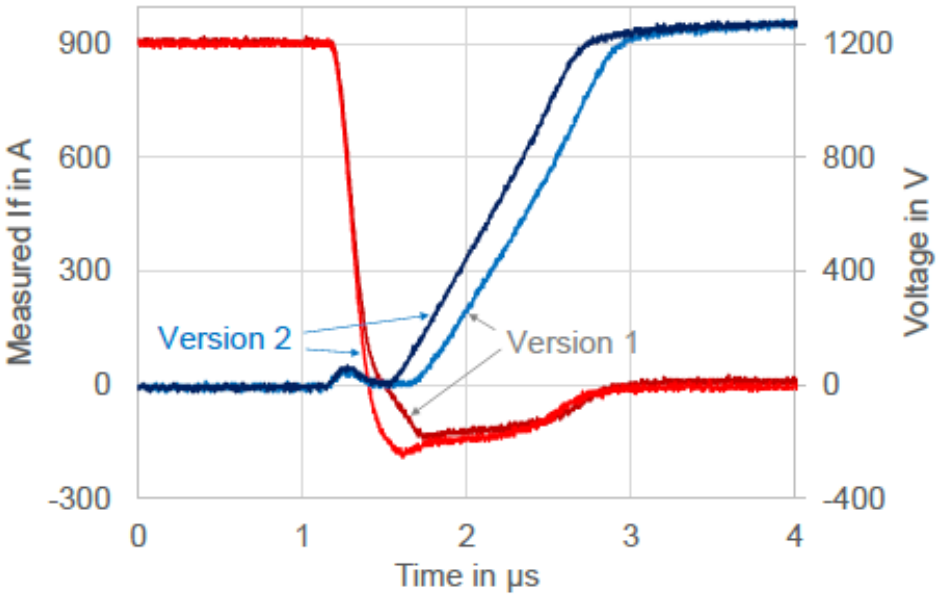
Version 2 - Actual



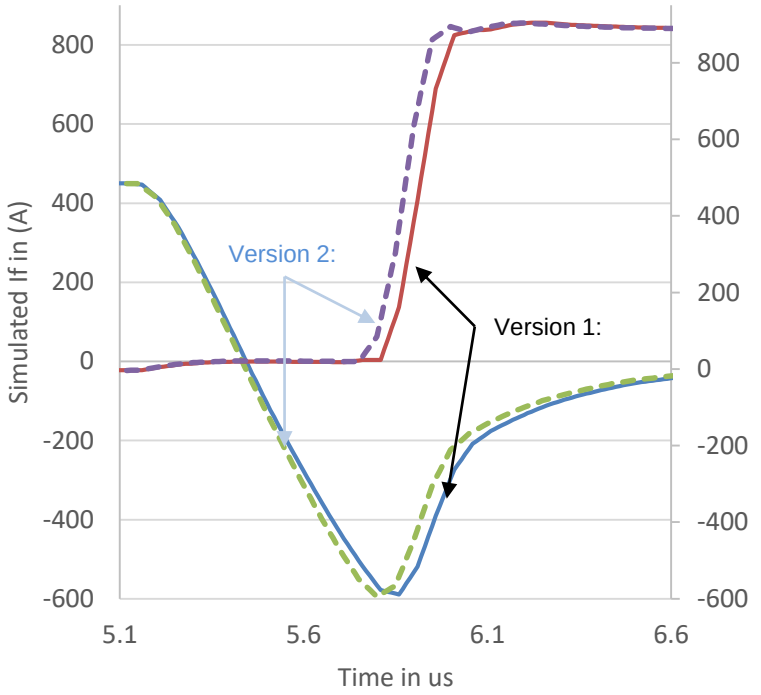
- Both layout versions were fabricated
- The electrical properties were characterized
  - Static & standard double pulse
  - Focus is on diode turn-off behavior

Electrical Measurement

Actual Testing



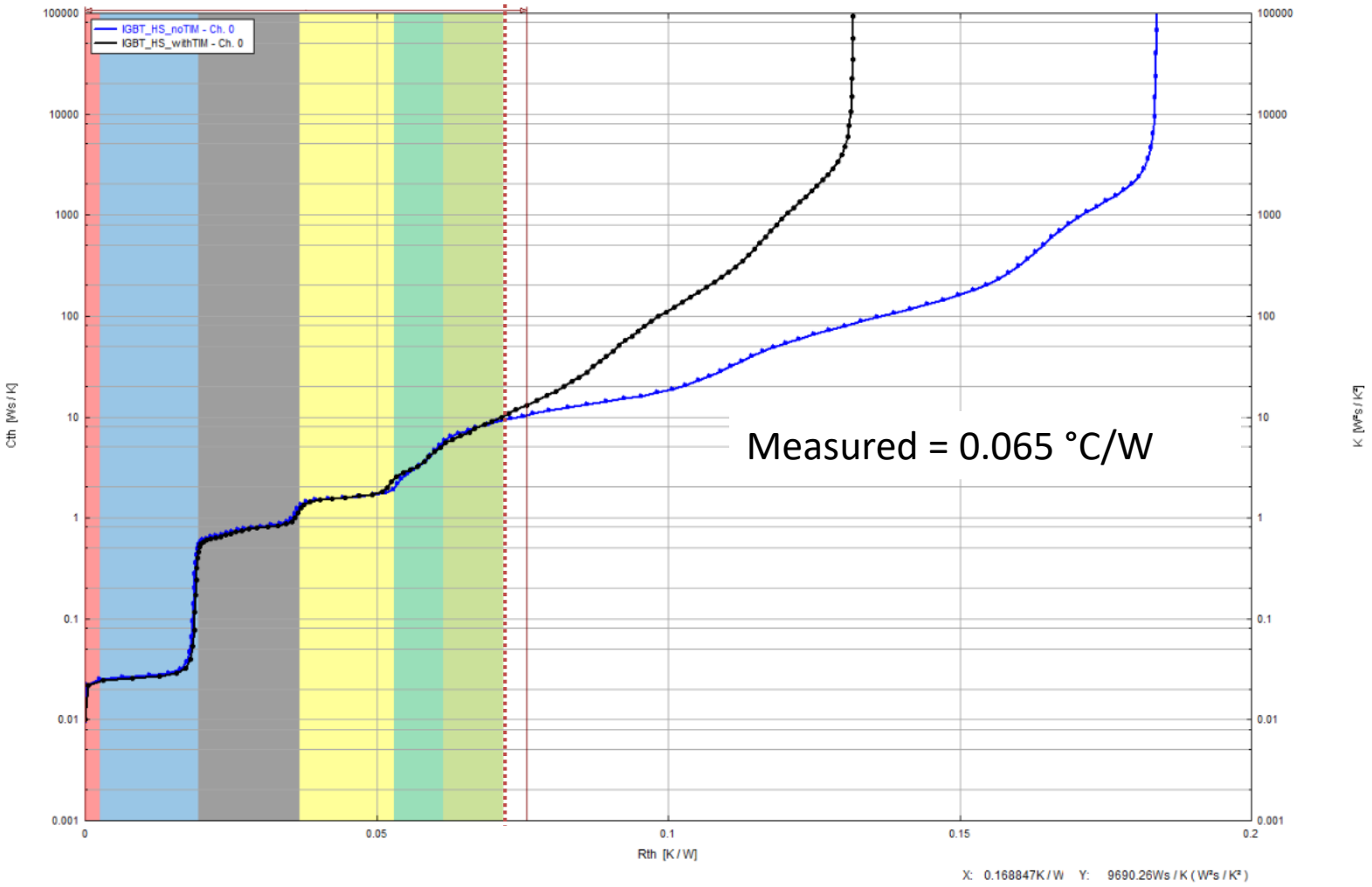
Simulated



Experimental results of the diode turn-off for the high-side switch – comparison of version 1 and 2 for safe-operating area conditions: Vdc=1300V, Ic=900A (2x Inominal), Tj=25°C, Vge=15V, Rg=0.2 Ohm).

Thermal Measurement

R_{TH} (junction to case) – IGBT [Version 2]



Conclusions

Conclusions

- Complete virtual prototyping approach
  - Concept with accurate 3D concept and geometry
  - Thermal sizing through FEM simulation
  - Parasitic extraction to perform co-simulation
  - Complete dynamic simulation

- Layout optimization
  - Designed for equilibrated current sharing
  - Temperature distribution
  - Switching behavior

Conclusions

- Actual testing
  - Confirmed the predictive power of simulations
  - Certain crucial features in the current and voltage waveforms were predicted and could be experimentally reproduced during the characterization

- Business Benefits
  - Communication is more effective, errors reduced, and more innovative product designs are delivered faster
  - Reduce cost of development and shorten time to market

Acknowledgement

- ABB & IMI

Optimized layout of 1700V LoPak1 IGBT power module by holistic design approach
Sven Matthias, Samuel Hartmann, Athanasios Mesemanolis, Raffael Schnell, Franc Dugal, Arnost Kopta, ABB Switzerland Ltd. Semiconductors, Switzerland, sven.matthias@ch.abb.com

Leonel Soberano, Dandy Jaducana, Jean-Marc Renard
IMI Philippines, North Science Avenue, Laguna Technopark, Biñan 4024 Laguna, Philippines
Andrea Irace, Michele Riccio

Università di Napoli "Federico II", Via Claudio 21, 80125 Napoli, Italy