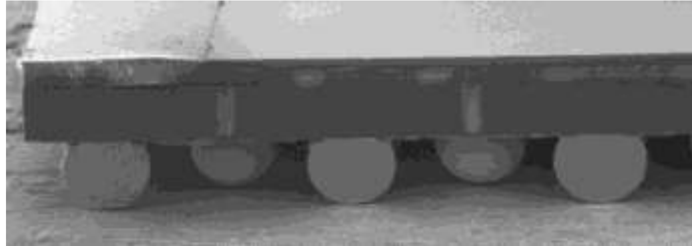

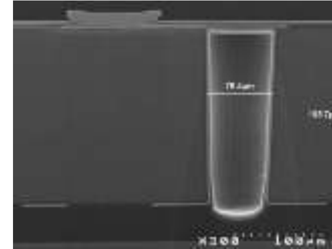

HIGH INTEGRATION OF FULL H BRIDGE ON SILICON INTERPOSER

Jean Charbonnier1, Venceslass Rat1, Hamilton de Carvalho1, Joerg Siegert2, Klaus Pressel3, Dominique Bergogne1, Gilles Simon1

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1 Introduction

2 3D stacking of power MOSFETs

3 Resistance

4 Experimental demonstration

5 Perspectives

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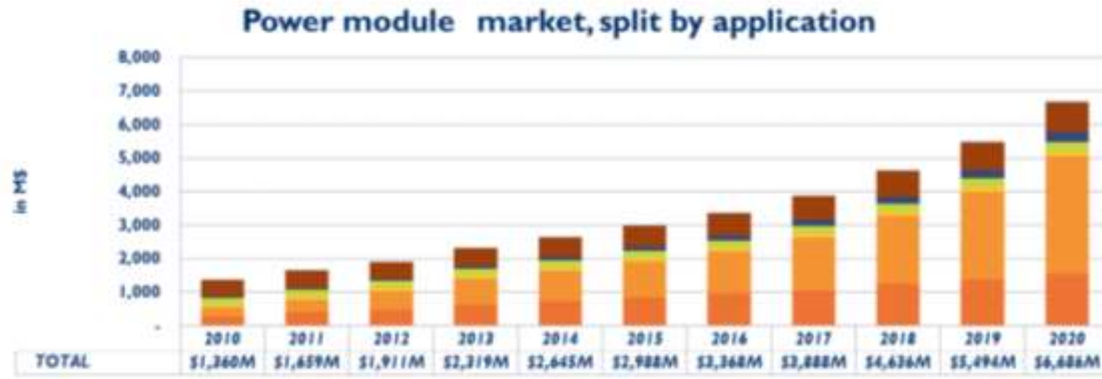
Introduction

- **Power modules and power discretes market is said to be doubled by 2020 (Yole Developpement).**



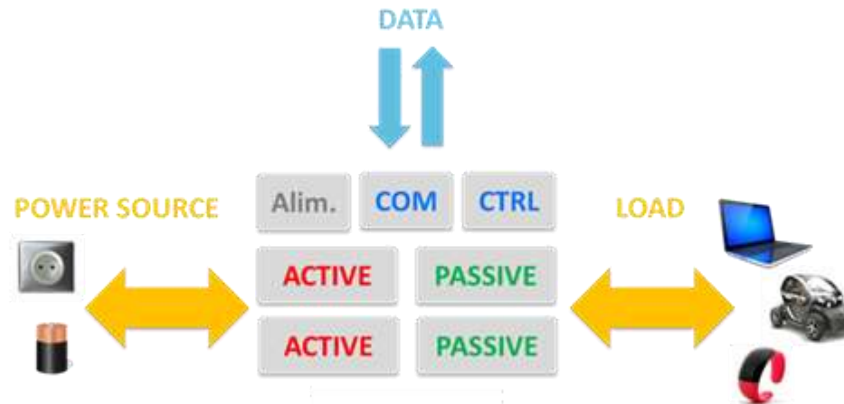
Yole Developpement – Semicon Europa 2015 – Power electronics

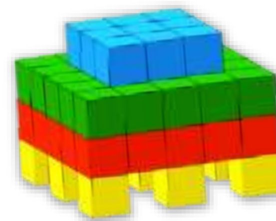
- **The need for miniaturization and for more functionality in a smaller volume is real.**
  - **Assembly and packaging involving system in package (SiP) will play a major role.**
  - **3D and Si interposer technologies provide interesting and smart alternatives for low parasitic connection and improved heat dissipation to standard laminates substrate**

- **This study introduce a power module with 5A MOSFET power chips mounted on a Si interposer to study the capability of Cu pillar technology and through silicon via (TSV) technology for power electronic applications.**

Introduction

3D integration of power modules

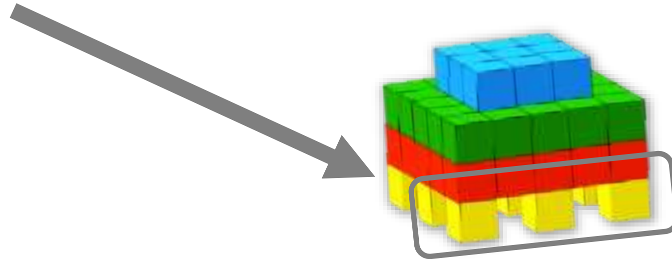




DATA Communications
Passives
Actives
Connections (Packaging)

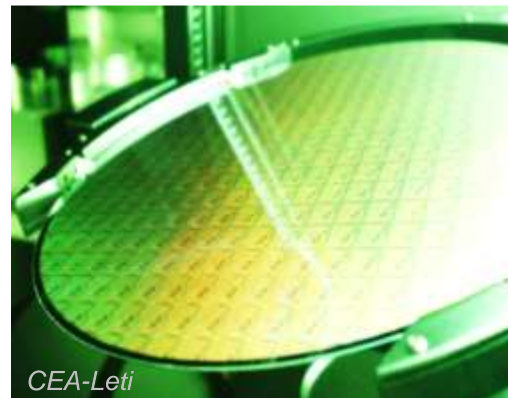
Introduction

This work



DATA Communications
Passives
Actives
Connections (Packaging)

+ Wafer Level Technology



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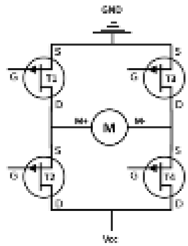
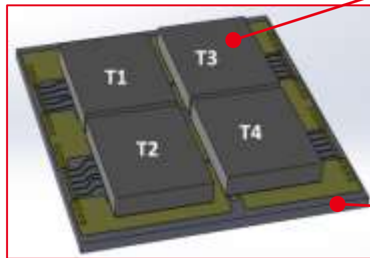
2 3D stacking of power MOSFETs

Design

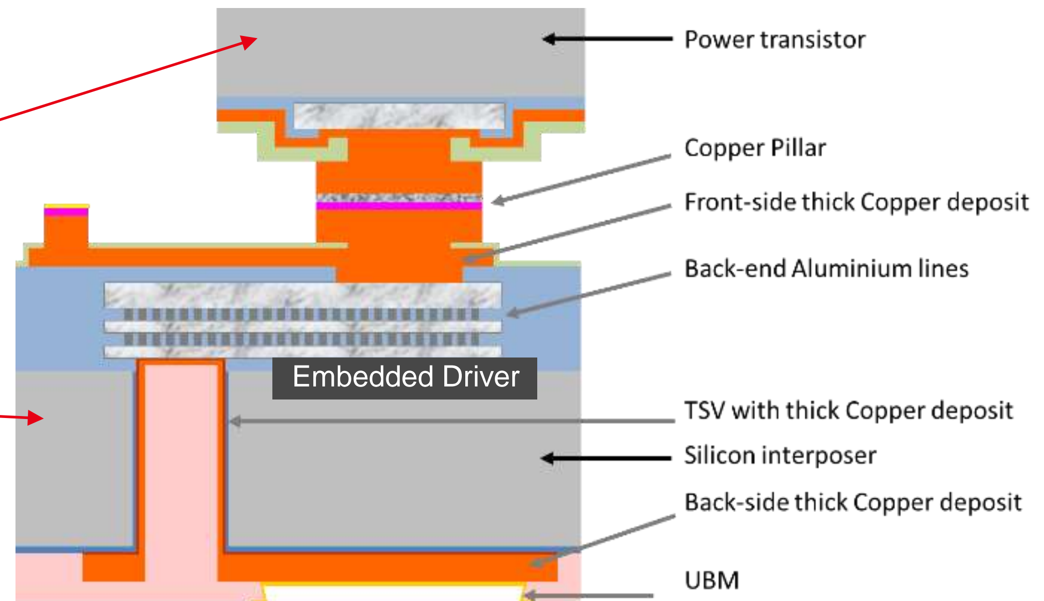
- Simple device : Full H bridge
- 4x 5A Power MOS on a passive Silicon Interposer (1st step)
- Possibility to embedded the Driver inside the interposer
- Short interconnection length: ➔ low consumption
  ➔ low parasite for high switching rate capability



Electrical H bridge electronic circuit



H bridge prototype with Silicon Interposer

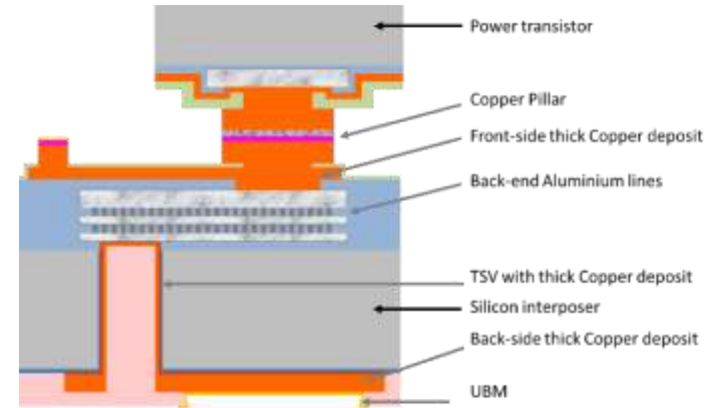


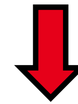
Cross Section of Technology schematic

Design

The demonstrator features:

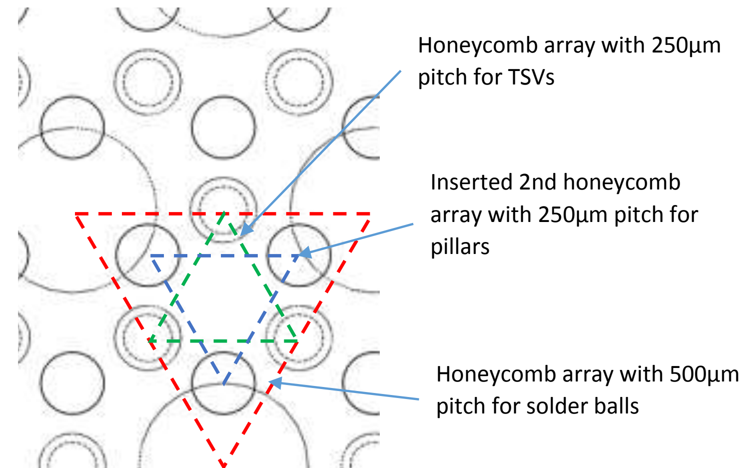
- Cu Redistribution layer (RDL) on Power MOS
- Copper Pillar Matrix
- Front side Cu RDL on Si Interposer
- 3x Al lines for driver integration simulation
- TSV Matrix
- Backside Cu RDL
- Under Bump Metallization (UBM) Matrix





In order to minimize the overall resistance and to optimize heat dissipation each matrix has been designed as a honeycomb array.

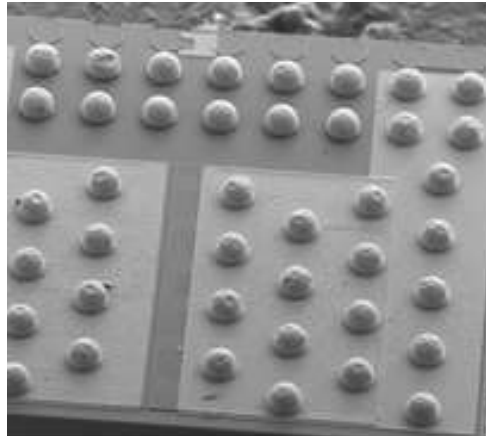
Moreover, each array is inserted in the other with respect to the minimum critical dimensions of the design rules.



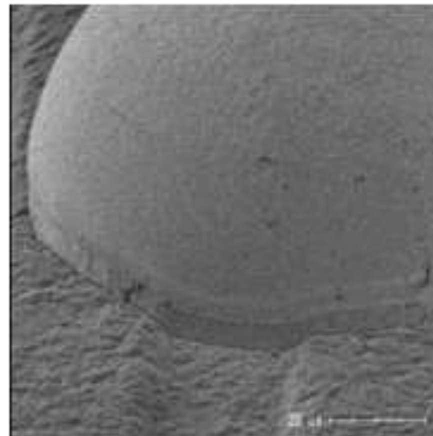
Compact integration of TSVs, pillars and solder balls.

Power Mos Process

- **Power MOS interconnection**
  - Cu Redistribution layer (RDL) on Power MOS to spread the current from the pads
  - Copper/Nickel/SnAg bump 105µm diameter matrix



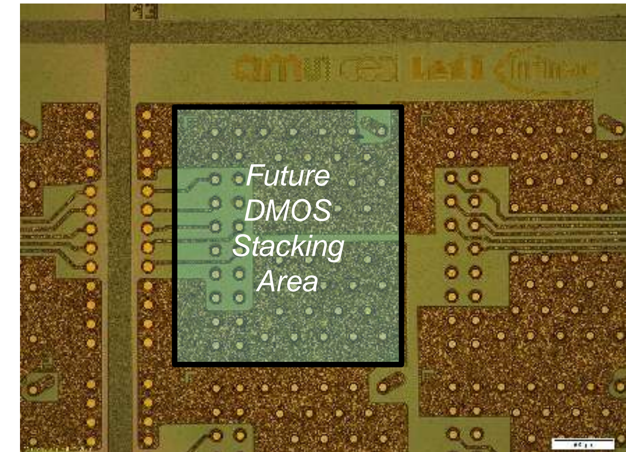
Diced DMOS chip before stacking



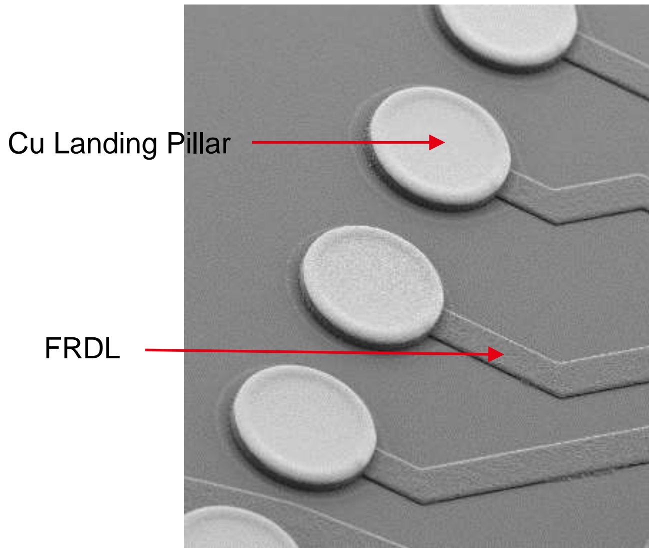
Cu Ni SnAg power bump

Silicon interposer Process: Front side interconnections

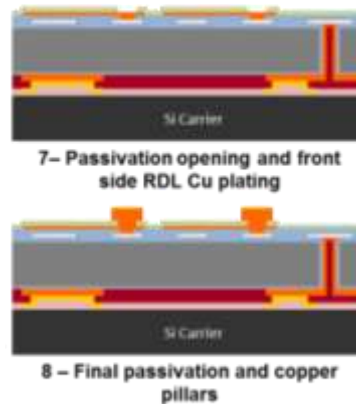
- **Front side interconnections: RDL and Pillar**



Back side processing TSV, BRDL metallization

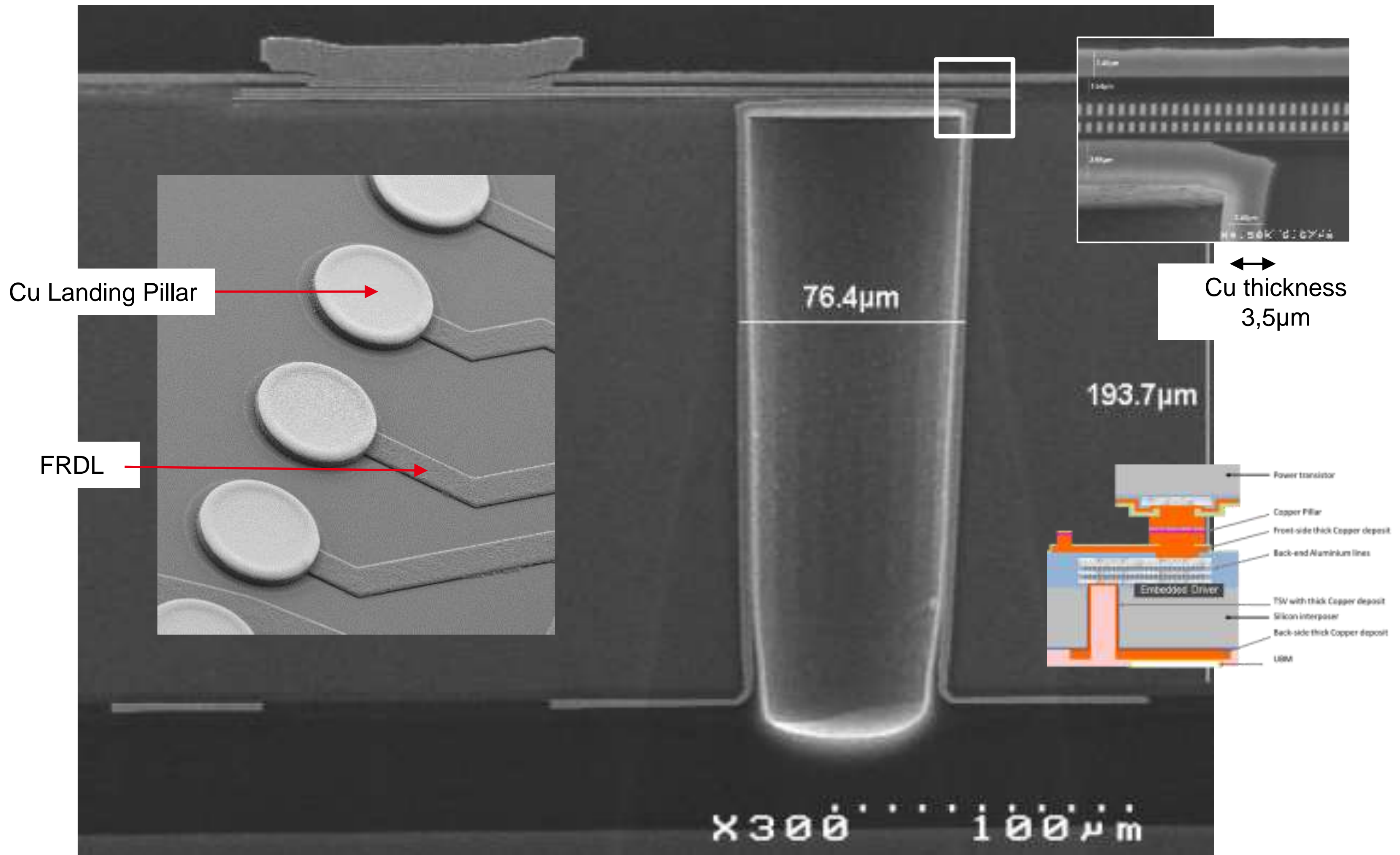


Front side processing FRDL, passivation and copper pillars SEM observation



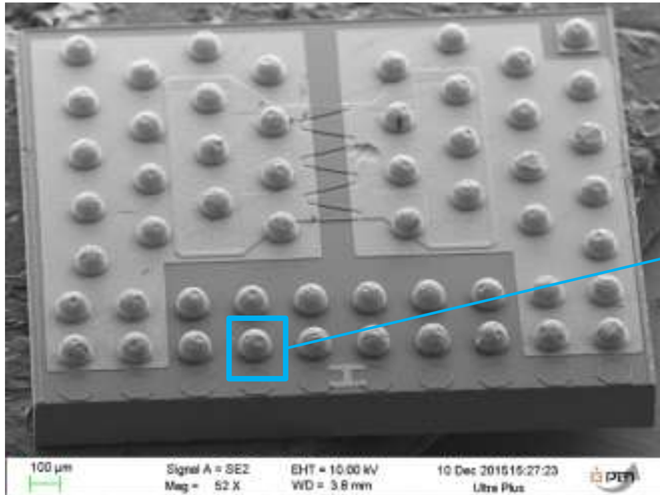
- **Front side rerouting**
  - Front side Cu RDL lithography
  - 3µm thick Cu RDL ECD
  - Mineral passivation
  - Passivation opening
  - Landing pillar lithography
  - Cu Ni Au pillar ECD

Silicon interposer – general cross section

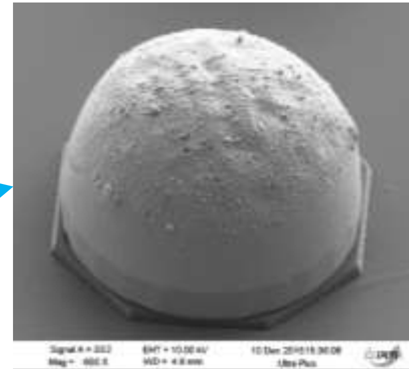


Technology global cross section Ams/Leti mixed process

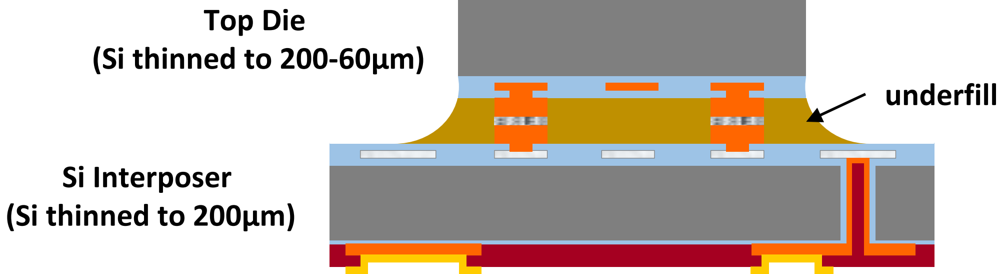
Prototyping: Assembly

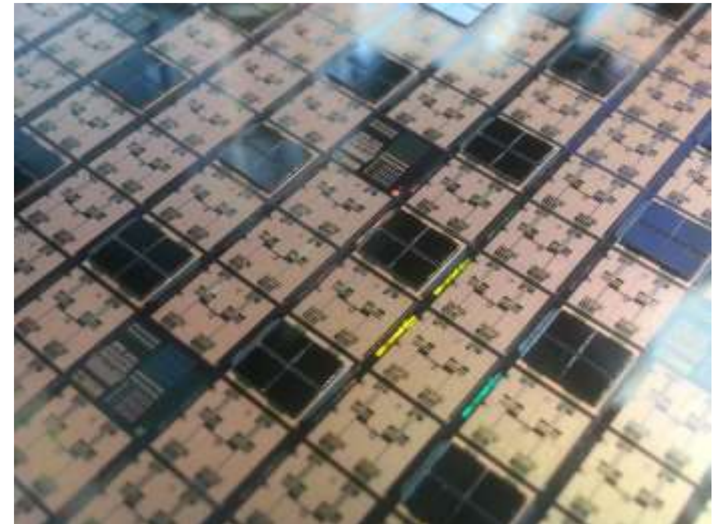


Infineon DMOS top die

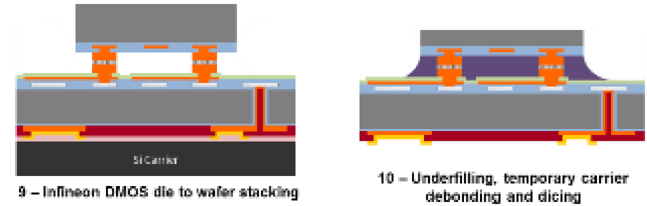


Power copper bumps (Ø105µm)

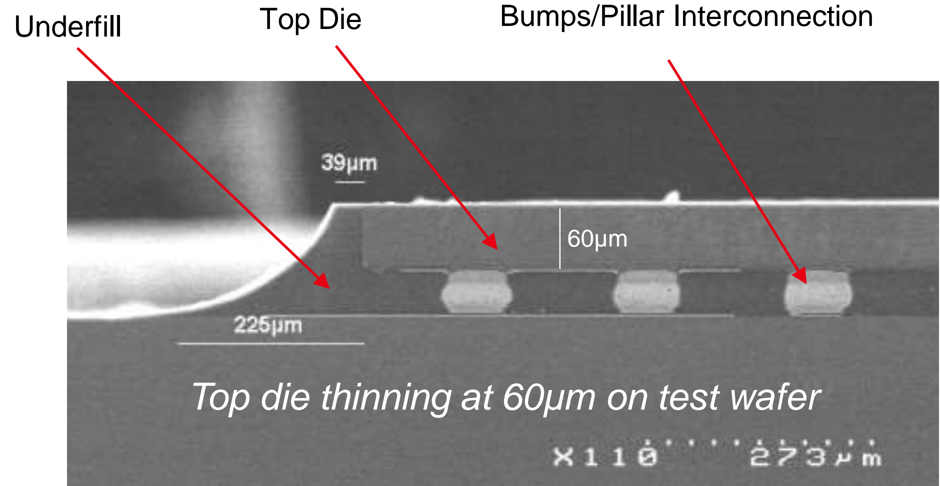


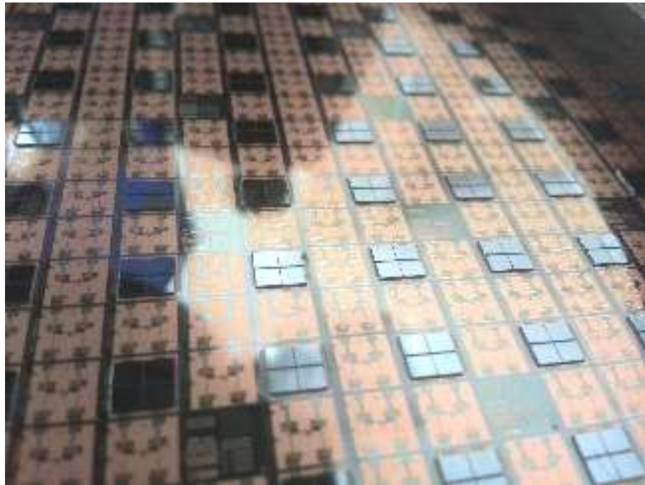


Prototyping: Assembly



- Die to Wafer Stacking
- Capillary Underfilling
- Top die Thinning until 60µm
- Debonding
- Dicing



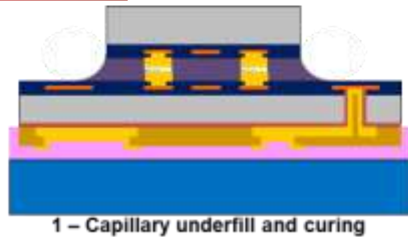


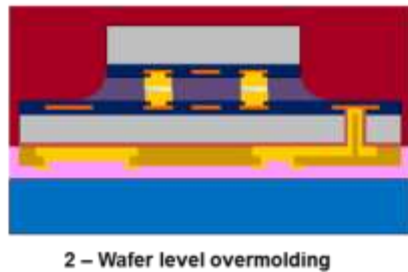
Infineon DMOS chips after stacking on ams/Leti Si interposer after reflow and underfilling wafer level

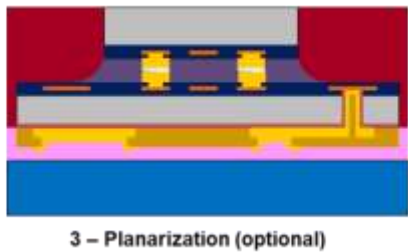
Optical top view the power MOS H-Bridge after Top die Thinning

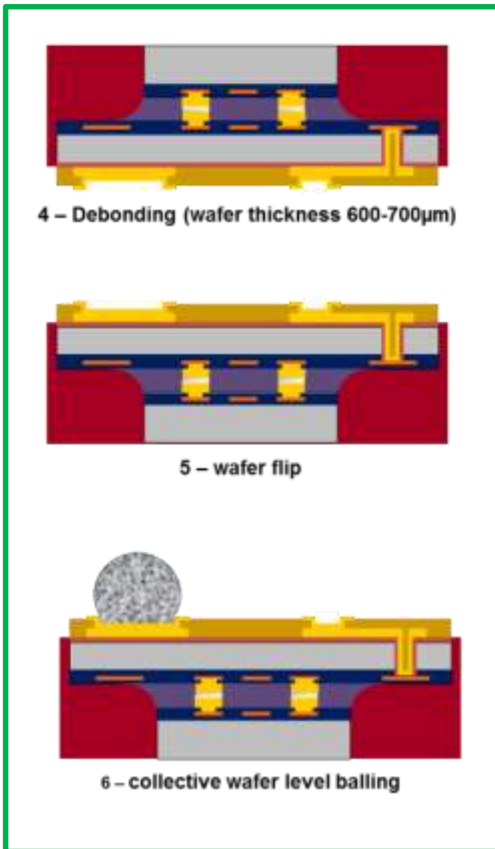
➔ Promising integration for efficient cooling of DMOS backside after thinning

ALTERNATIVE FULL "WAFER LEVEL" PROCESS FLOW


1 – Capillary underfill and curing


2 – Wafer level overmolding

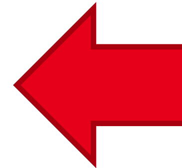

3 – Planarization (optional)


4 – Debonding (wafer thickness 600-700µm)

5 – wafer flip

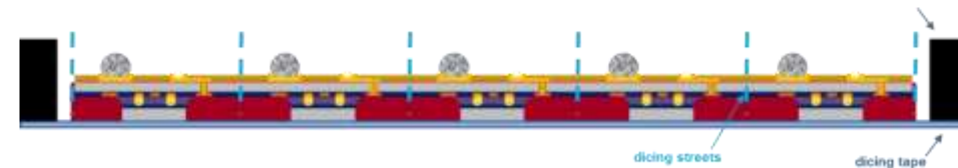
6 – collective wafer level balling

Simplification of the process flow for handling



Usually complex process steps due to thin wafer handling (warp, detection, silicon breakage)

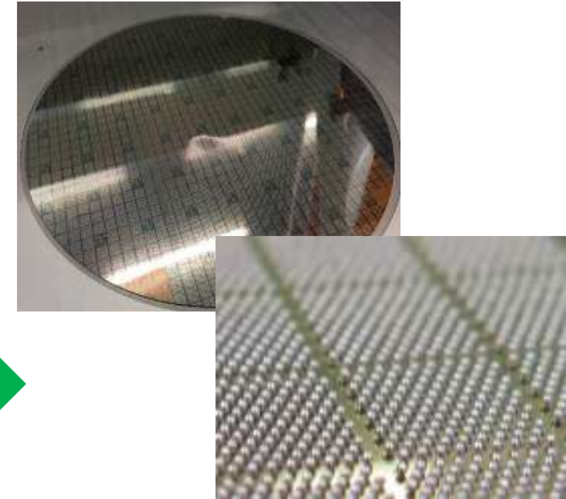
From debonding to dicing process (step 4 to 7), a 600µm to 700µm thick wafer is easier to handle thanks to molding !



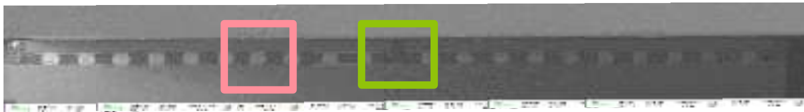
7 - Mounting on dicing frame, dicing and final delivery

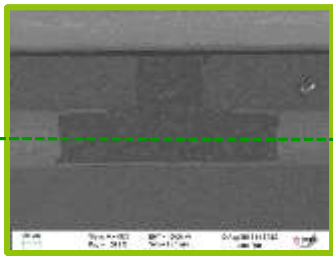
APPLICATION TO STACKED MODULE

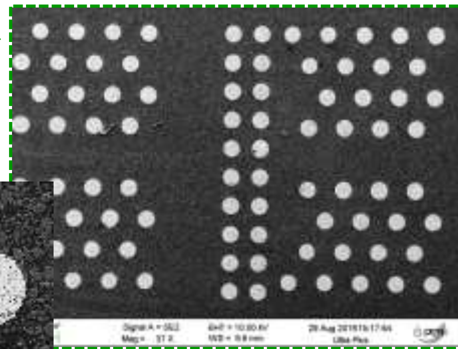
Wafer Level Balling

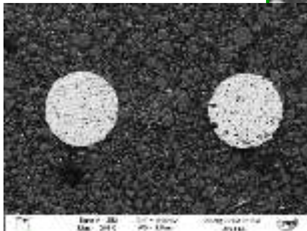


UF and Molding in 1 step: Dry film lamination







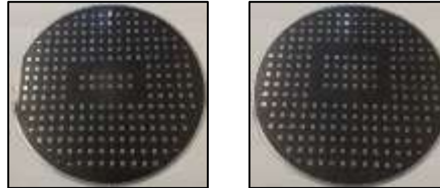


Parallel polishing characterisation reveal no voids or defect at interconnections interface

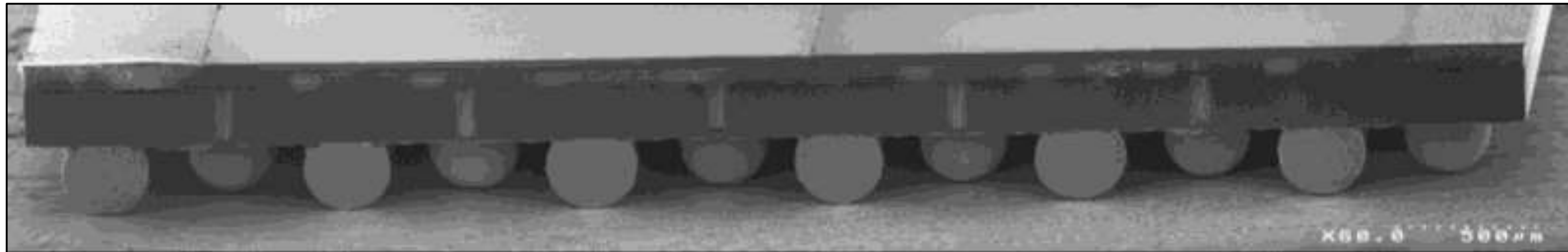
Wafer level Balling by Screen printing
Ø 300µm pitch 500µm
on 300µm thin wafers
thanks to porous segment

FUNCTIONAL POWER MODULES

Application to Full module

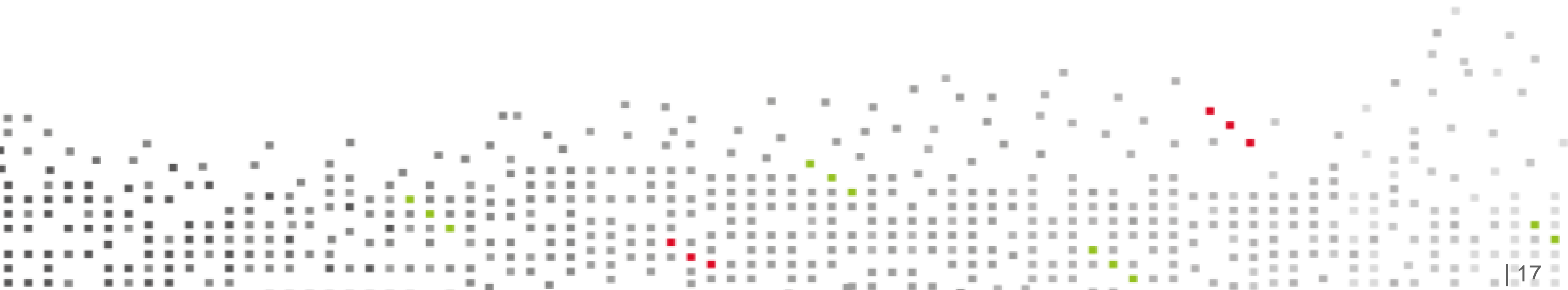


Full wafers of H bridge Modules after WLOM and WLB



- **Power modules have been successfully produced at wafer level**
- **Process cost and time optimized thanks to new WLOM and WLB collectives approaches**
- **Combined molding underfiling process has been developed and applied to the demonstrator**

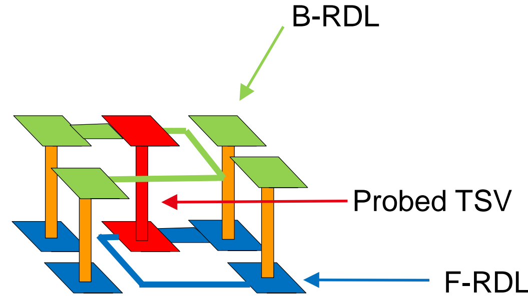
3 Resistance

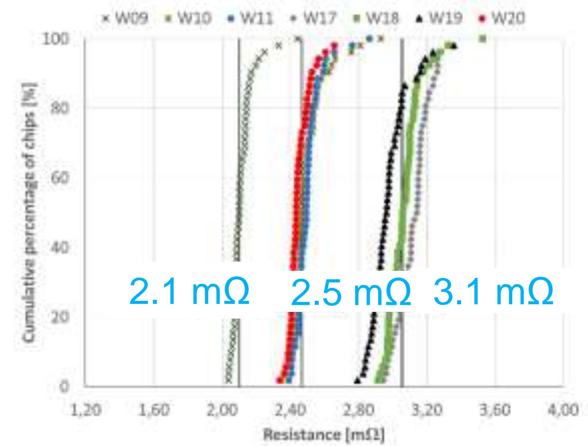


Si interposer Electrical characterisation

- **Kelvin TSV 80x200µm for 3 technological splits of TSV sidewall copper thickness:**
  - 4.7µm
  - 3.6µm
  - 2.7µm

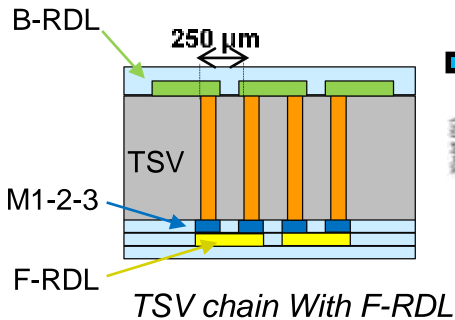
➔ **Very low resistance for Power application**



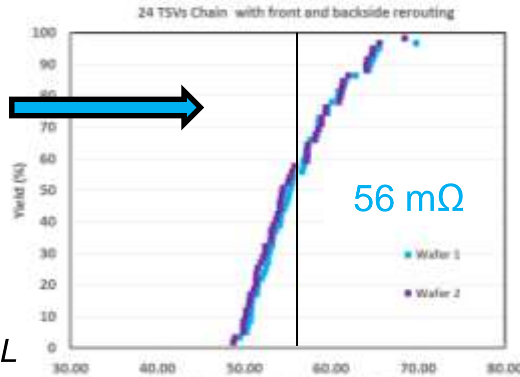


Contact resistance Kelvin TSV

- **Added resistance due to 3D integration:**



TSV chain With F-RDL



Resistance of a Single TSV including FS and Back side 40µm width connections

- **Single TSV resistance:**
  - Front side access: 21mΩ
  - Back side access: 17mΩ
  - 56 - (21+17) = **19mΩ** for a Single TSV

Si interposer Electrical characterisation

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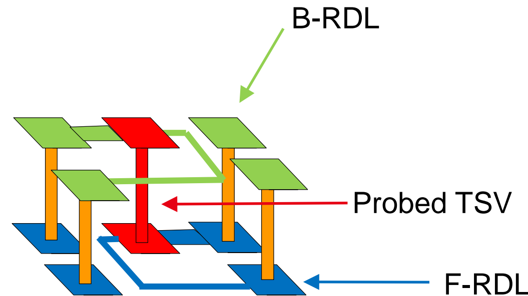
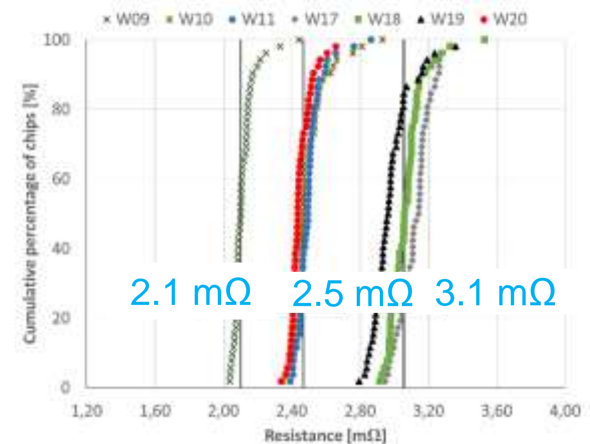


➔ Very low resistance for Power application



Contact resistance Kelvin TSV

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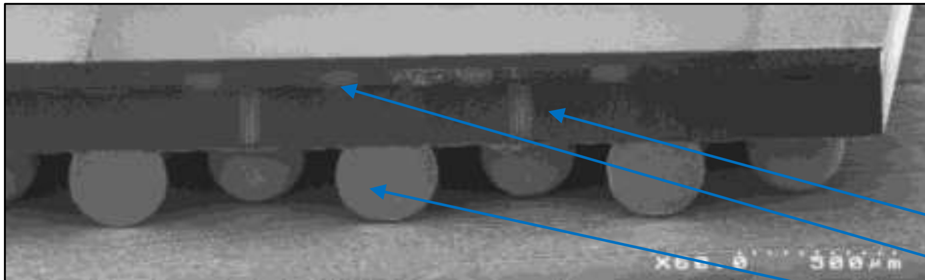


- **Single TSV resistance:**
  - Front side access: 21mΩ
  - Back side access: 17mΩ
  - 56 - (21+17) = **19mΩ** for a Single TSV

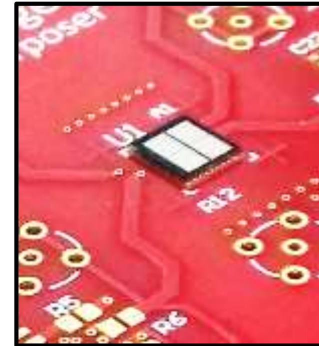
- **Added resistance per mm²:**
  - TSV density = 18.5 TSV/mm2
  - TSV resistance: 1.0 mΩ/mm2
  - Bumps resistance: 3.60×10^{-2} mΩ/mm2
  - Balls resistance: 1.17 mΩ/mm2

Rtot = RTSV + Rinterco = 1.0 + 1.2 = 2.2 mΩ/mm² added to Ron

Measured resistance on test board

Die only	Wire bonded	Balled brazed
125 [mΩ]	204 [mΩ]	127 [mΩ]

Measured On-resistance for one power switch



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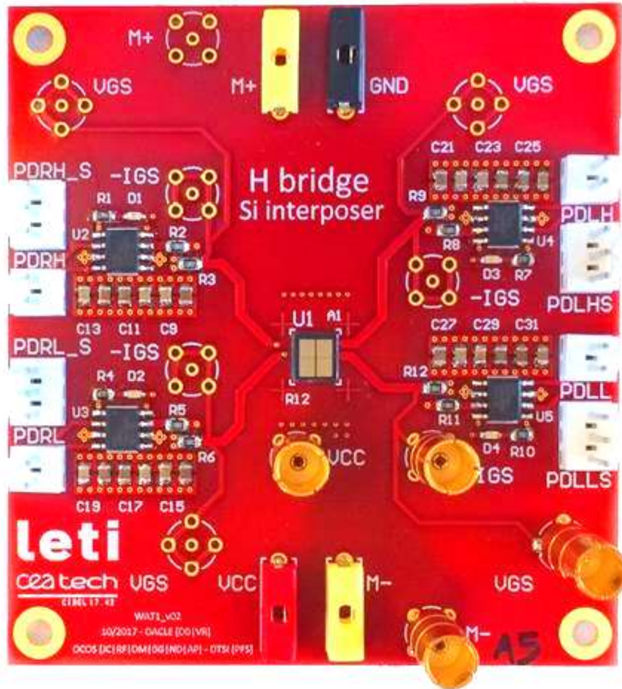
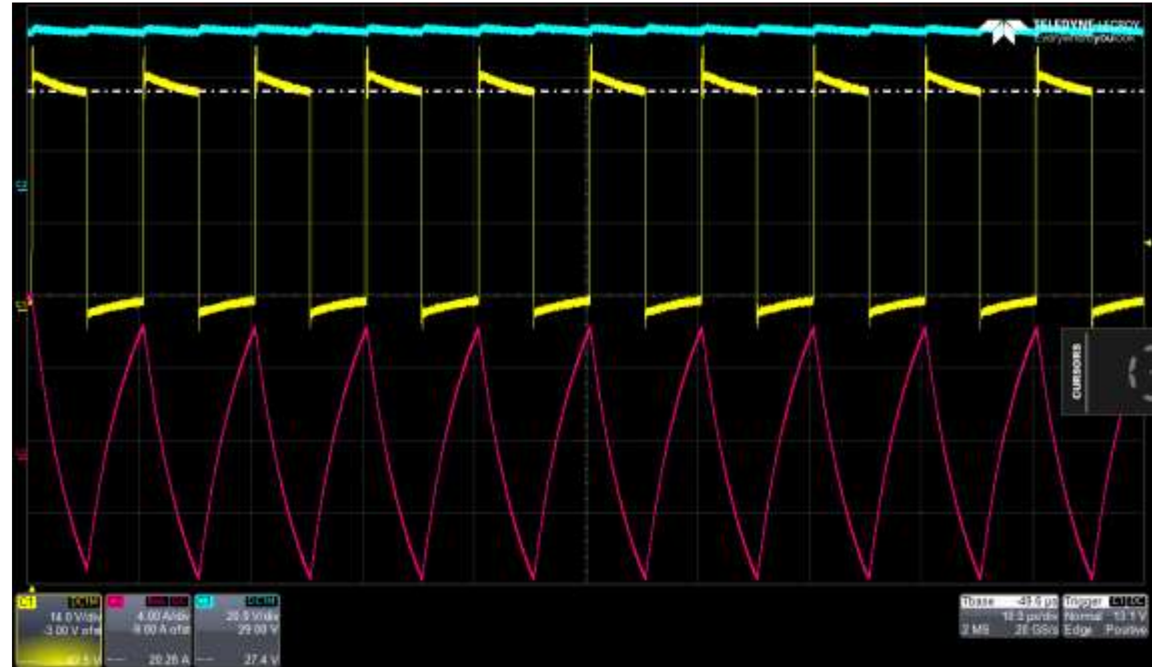
4 Experimental demonstration

Experimental demonstration

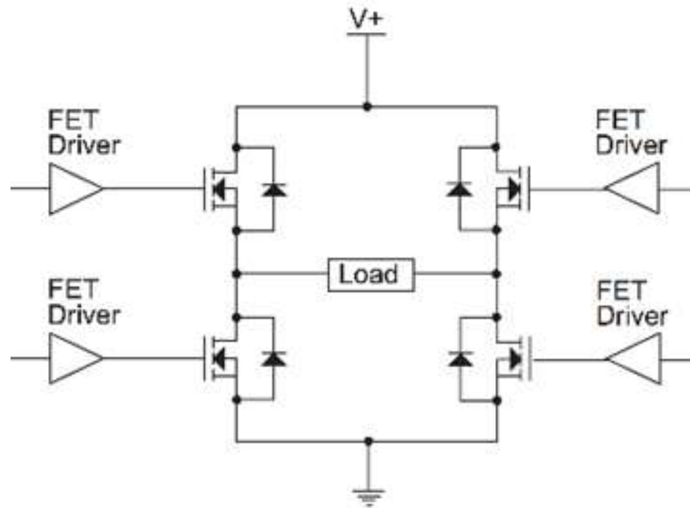
- 100kHz switching frequency
- 48VDC supply
- 15A pic (for testing only) 5A rated



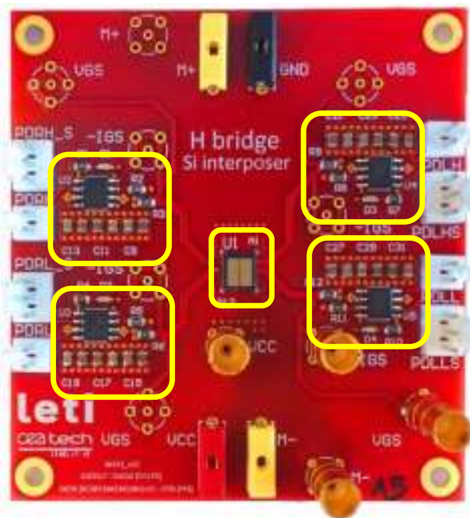


15A pic without heatsinking with 5A devices (no heatsink = easier to test)
=> High temperature rise => Ron increases => Von increases

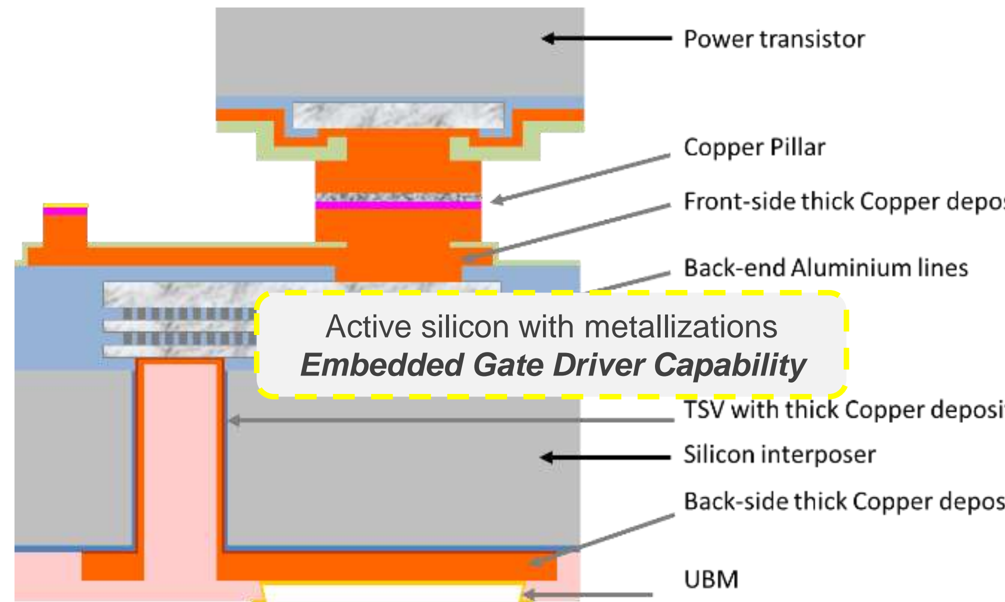
Experimental circuit and technology



H Bridge with Gate Drivers

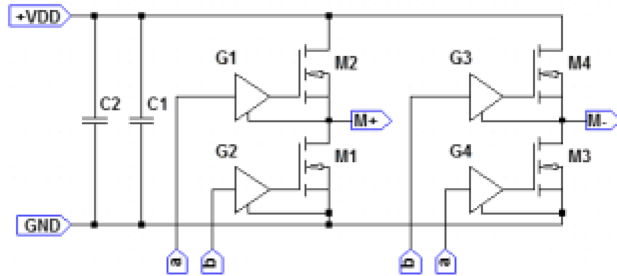


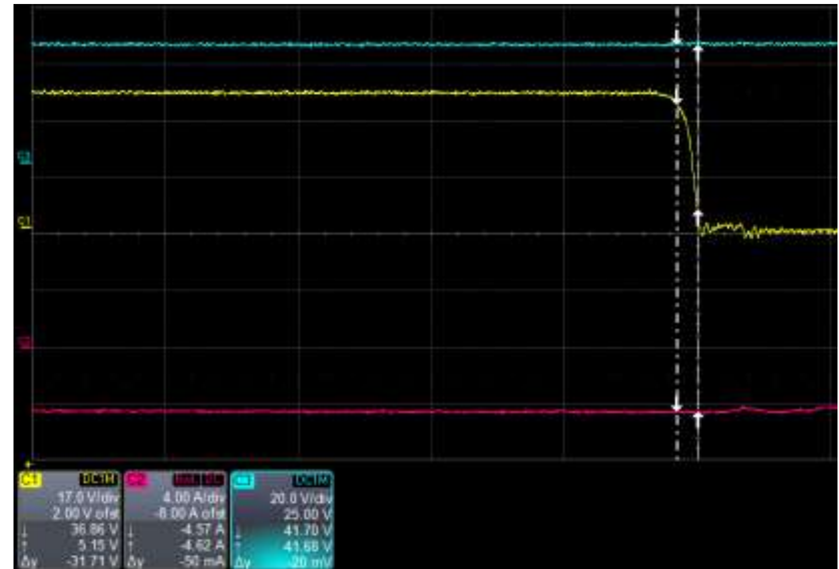
The silicon interposer is capable of hosting the gate driver

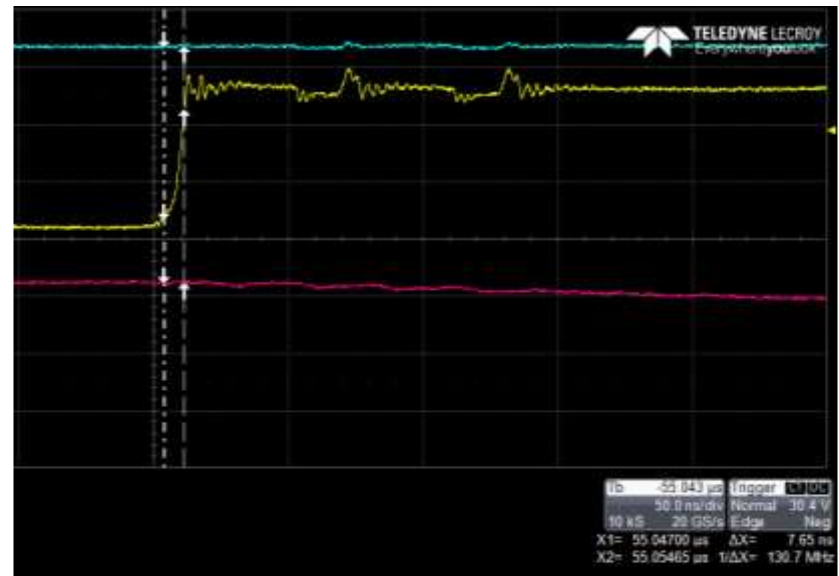


3D technological stack at wafer level

Experimental demonstration, switching







- **Yellow : M+ Bridge Output voltage**
  - Rise/Fall time : 7.6 ns
- **Red : Load Current**
  - 4.6 A
- **Blue : DC Bus voltage**
  - 41 V
- **Approximated switching losses**
  - 1.2 uJ per switch
  - Less than 500 mW for the H-Bridge @100 kHz)

- **Approximated conduction losses**
  - 5 W for the H-Bridge (180 W Output Power)

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Conclusions & perspectives

Conclusions:

- A new complete 3D integrated H bridge device has been proposed, designed and processed through the collaboration of Infineon, ams and Leti.
- Dedicated process modules, design and design rules have been developed and applied for this power application in the 1 hundred to kilowatt range, including thick copper rerouting.
- The good electrical performance of the setup is reflected for example in the very low Kelvin TSV contact resistance of 2.1mΩ as well as by fully functional DMOS devices.
- Measured switching performance is satisfactory

➔ These results confirm the path for new types of 3D applications in the field of medium power devices.

➔ Relatives dimensions between active interposer (drivers + passives) could be overpassed by using Leti CIWIS technology or switching to FO-WLP.

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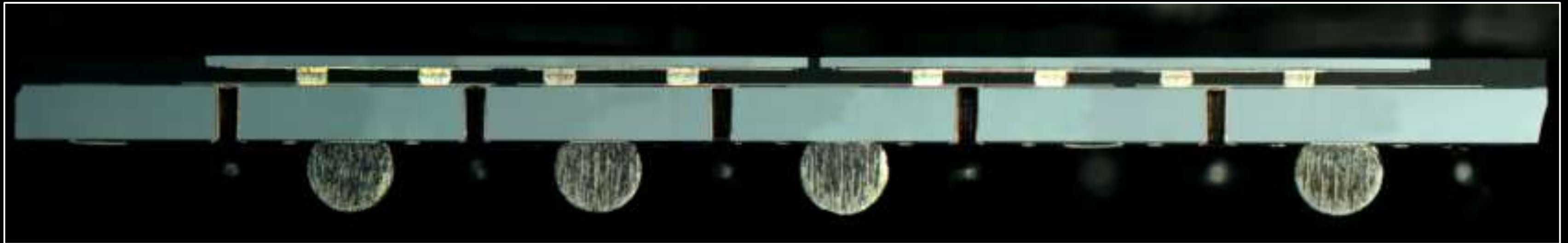
Thanks for your attention!
Any questions?



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