Methodology of signal and power integrity for multilayer embedded PCB

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Outline

1. **Objective of EDDEMA Project**
2. **SI/PI analyses for EDDEMA**
   - SI/PI Simulation methodology
   - Impedance extraction technique
3. **IC-EMC model establishment**
4. **Future works**

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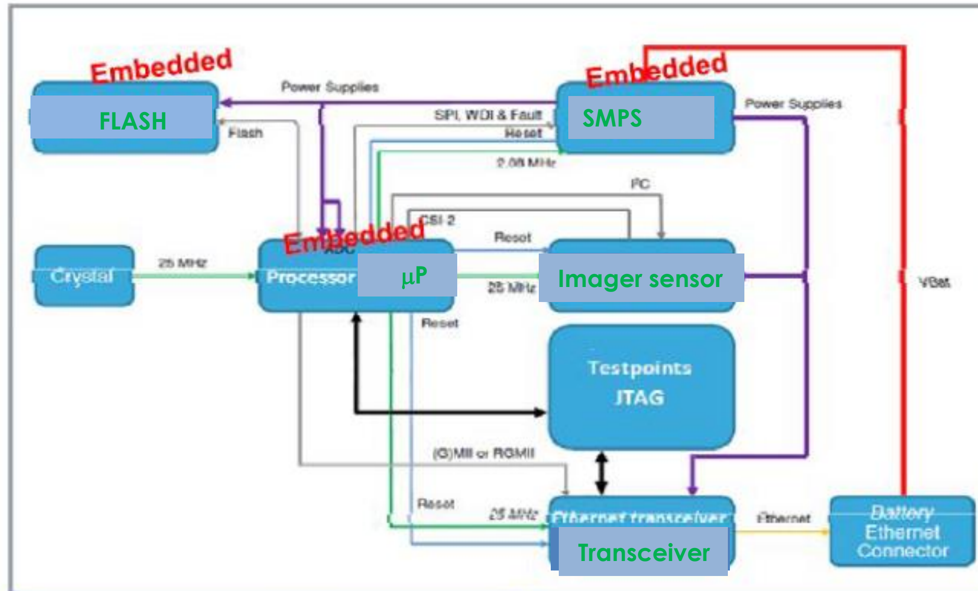
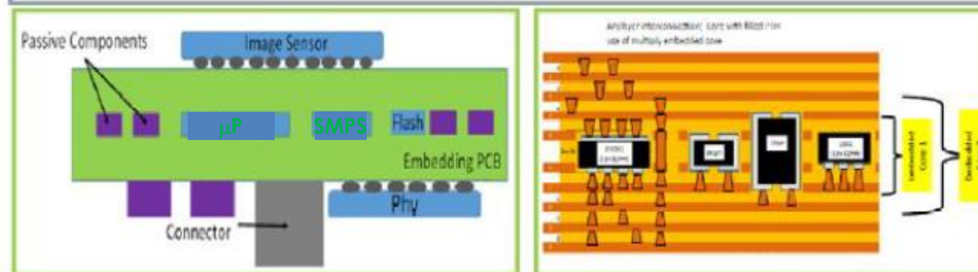
Objective of EDDEMA Project

DESIGN FOR MANUFACTURING - TEST VEHICULE
PROTOTYPE N°1: DUMMY MOCK-UP WITH DAISY CHAIN DICES



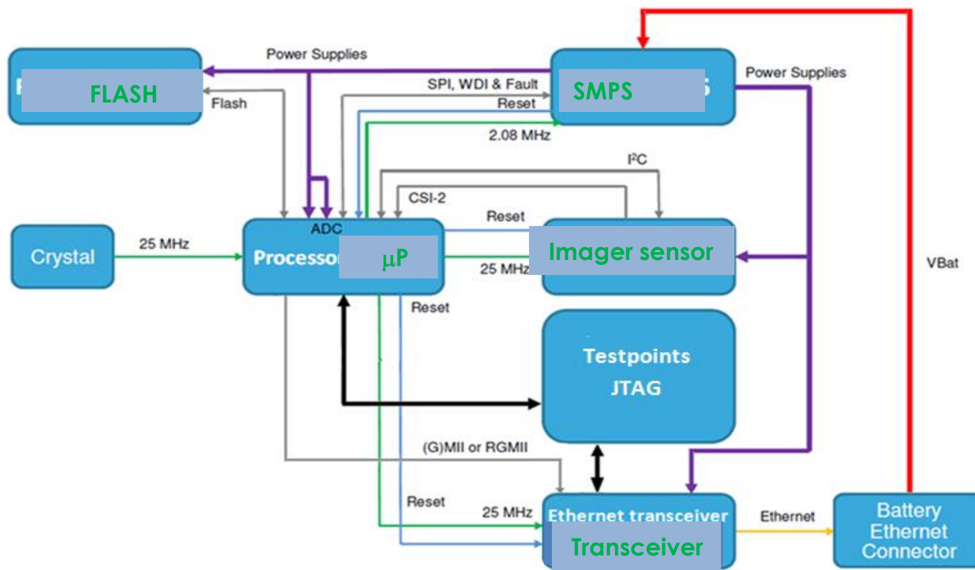


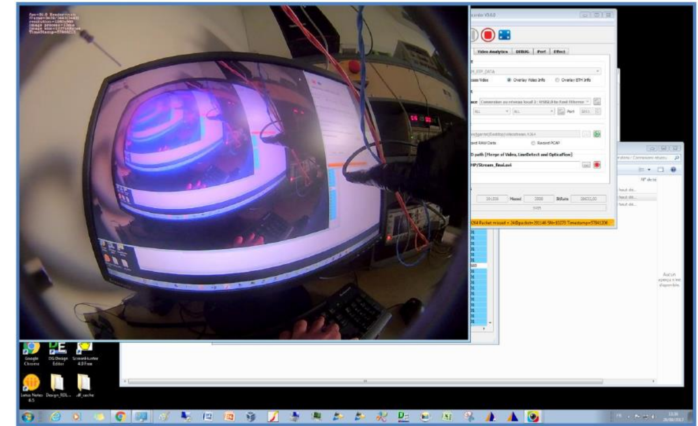
The Camera is the product that needs the most integration at Valeo,

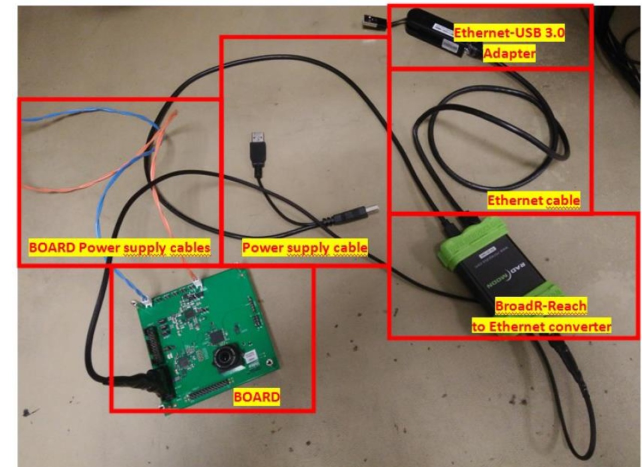
PWB size: 24.2 x 23.3mm; thickness: 1mm
Housing (AlSi12, Plastic) -
28 x 28mm; 3 screw holes diameter 2.7mm

Prototype1 stackup: 12 layers, 2 embedded components cores
(E C thicknesses: 150um & 330um)

Objective of EDDEMA Project







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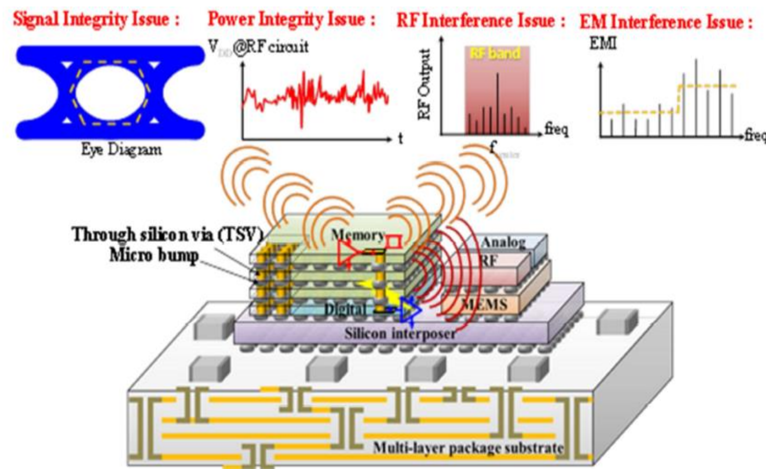
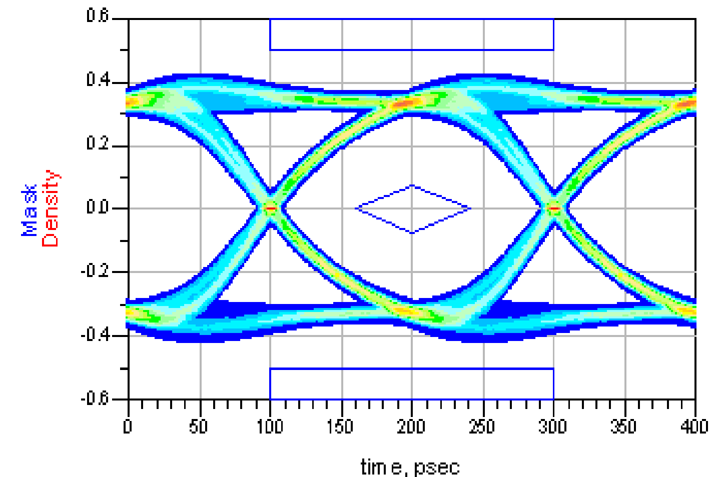
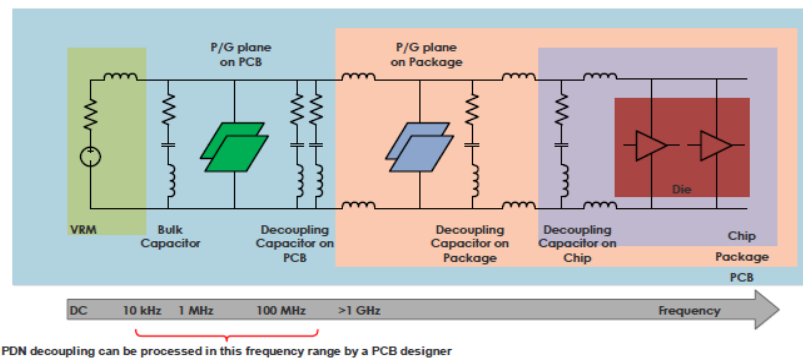
SI/PI analyses for EDDEMA

General observations on the camera board







SI/PI analyses for EDDEMA

Zuken® | SIwave® | CST®

We start with 2D simulations (CST® PCB studio and SIwave®). Here we have done some SI/PI results for Prototype 1 by using SIwave®, since CST® PCB studio is not able to do these analyses. When the results need to be more accurate, the 3D simulations will be applied, however, the time consumption will be longer depending on the complexity of the board.

Import ZUKEN® EDDEMA prototype to SIwave®.

Tools	Method	Speed	Memory	Nets	Components	Pins
SIwave®	MoM (traces), FEM (Plane)	SI and PI: High (<5min)	Low	32 unknow nets (E-nets ZUKEN®)	No lost	No lost

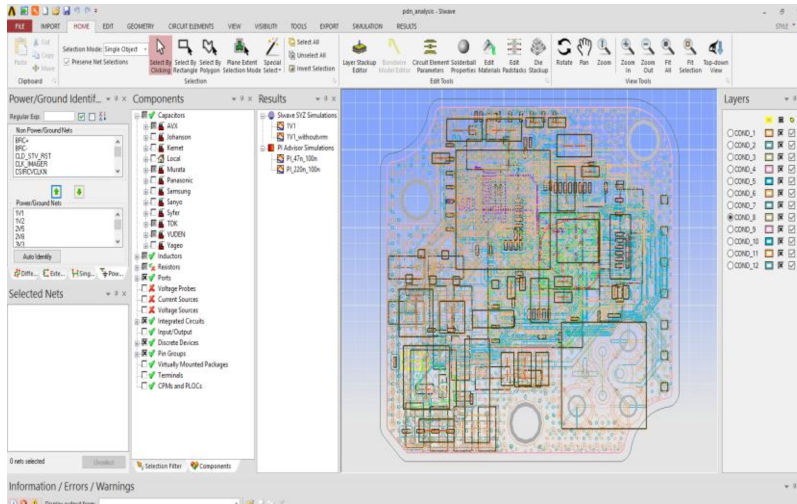
Import EDDEMA prototype to CST® PCB studio.

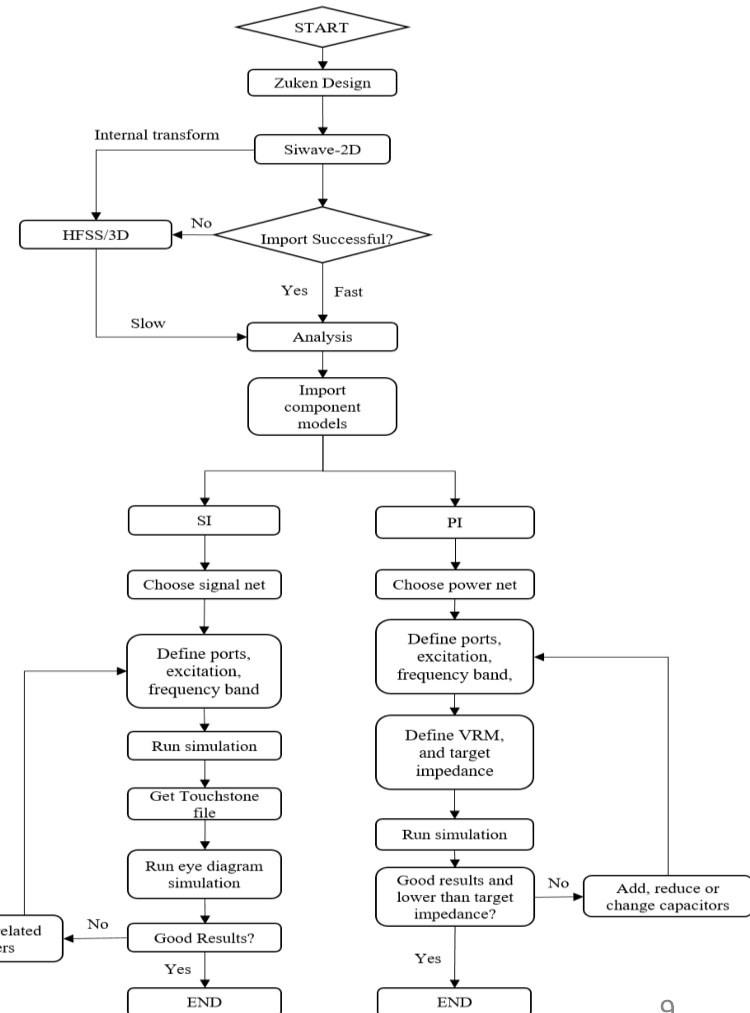
Tools	Solvers	Speed	Memory	Nets	Components	Pins
CST® PCB studio	TLM(SI), FEM(PI)	SI(<5mins) PI(cannot do)	SI(low)	32 unknow nets	No lose	All pins of embedded components lose

SI/PI analyses for EDDEMA

Simulation methodology

EDDEMA Project dedicated to develop a camera with embedded active components inside the PCB, after checking and comparing with CST, Siwave is more compatible to the data generated by Zuken for multi-boards analysis.

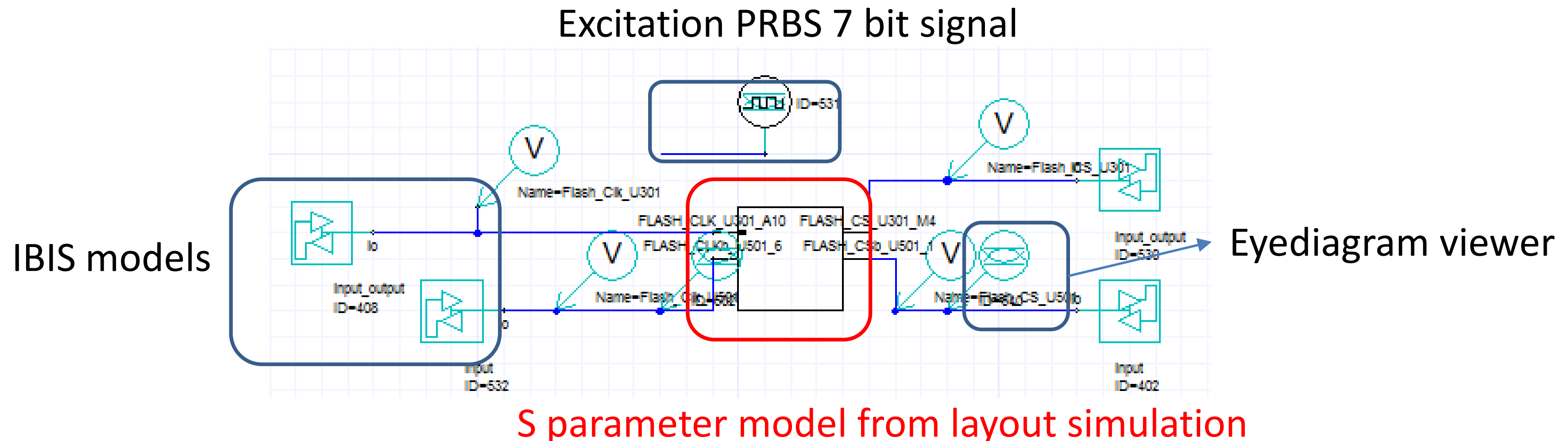




SI/PI analyses for EDDEMA

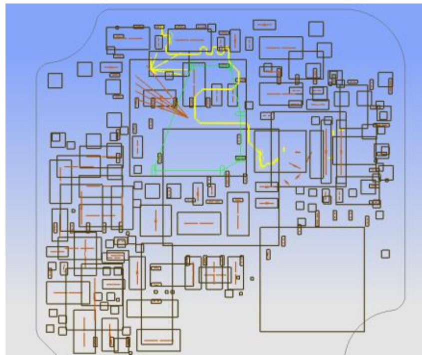
General Signal integrity analysis methodology

The S parameter model of the signals are obtained through Siwave simulation based on the layout of Prototype, the rise and fall time are already defined inside the IBIS model, the PRBS signal definitions (frequency, amplitude….) are based on the measurement from Application board



SI/PI analyses for EDDEMA

Example of Signal Integrity analysis



Layout of **FLASH - CLK** network in Prototype2

Vhigh	Vlow	Bit per second	Pseudo random bits
3.3 V	0	7.5ns	7 bits

Stimulus
From AP measurement

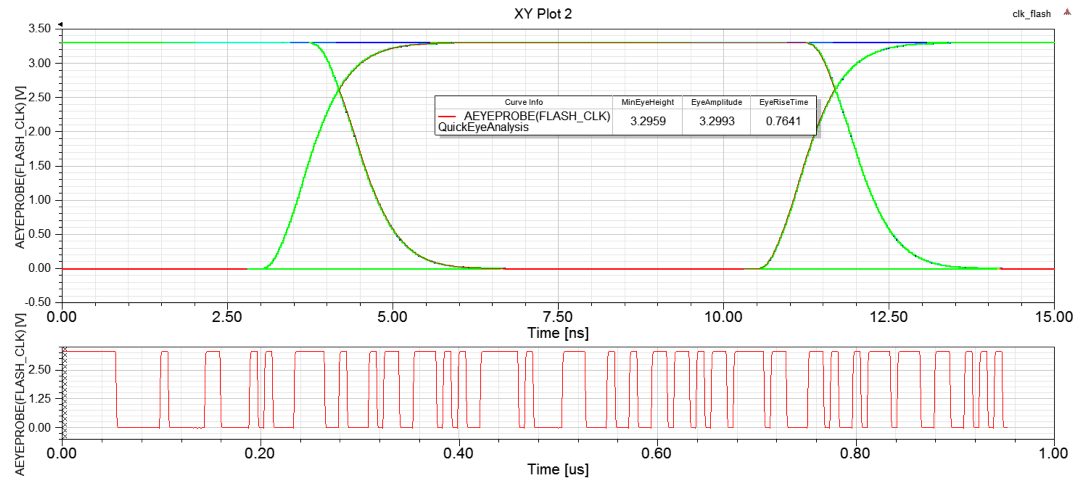
Signals are perfect concerning the over/undershoot

Good!

Requirements for the signal

BD4X_HF

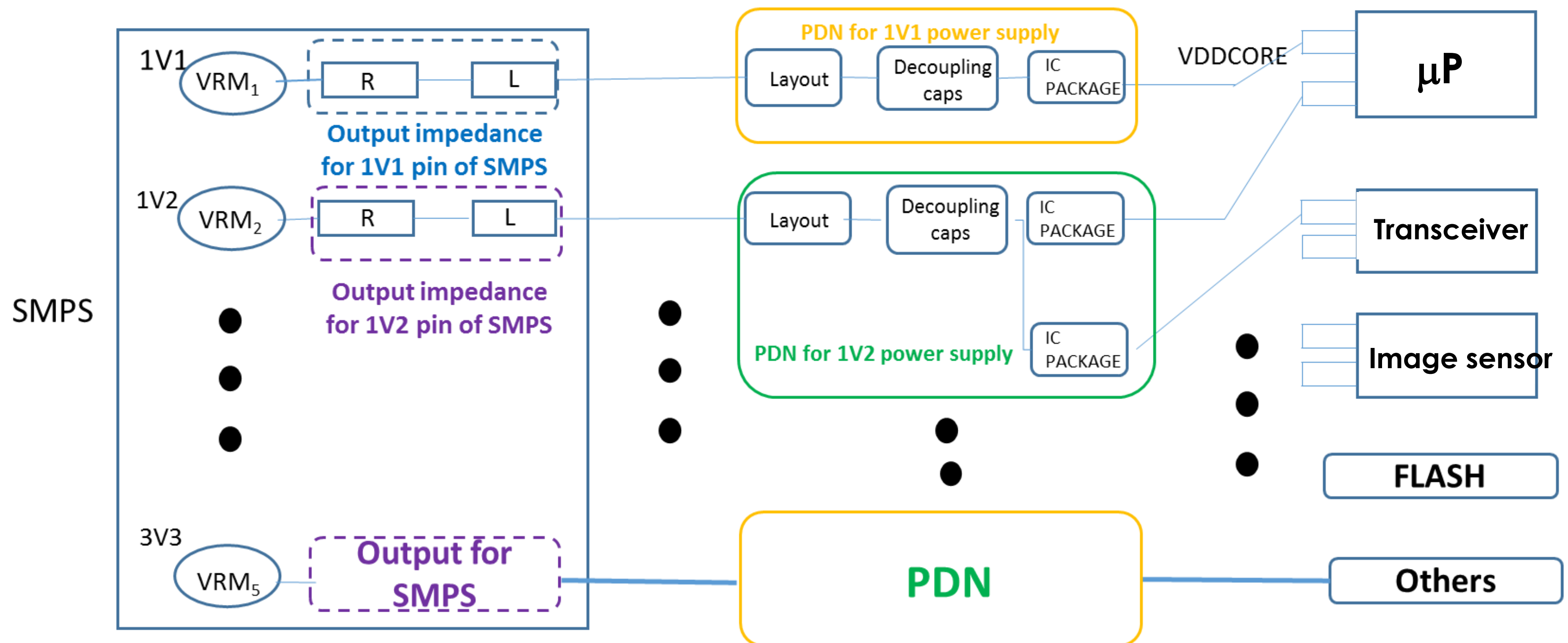
3.3V I/O operation						
V_{IH}	High level input voltage	-	2.0	-	VDD_IO + 0.3	V
V_{IL}	Low level input voltage	-	-0.3	-	0.8	V
V_{HYST}	Schmitt trigger hysteresis	-	250	-	-	mV



$V_{Max} = V_{IH} = 3.3V+0.3V=3,6V$
$V_{Min} = V_{IL} = -0.3V$

SI/PI analyses for EDDEMA

Power Integrity analysis

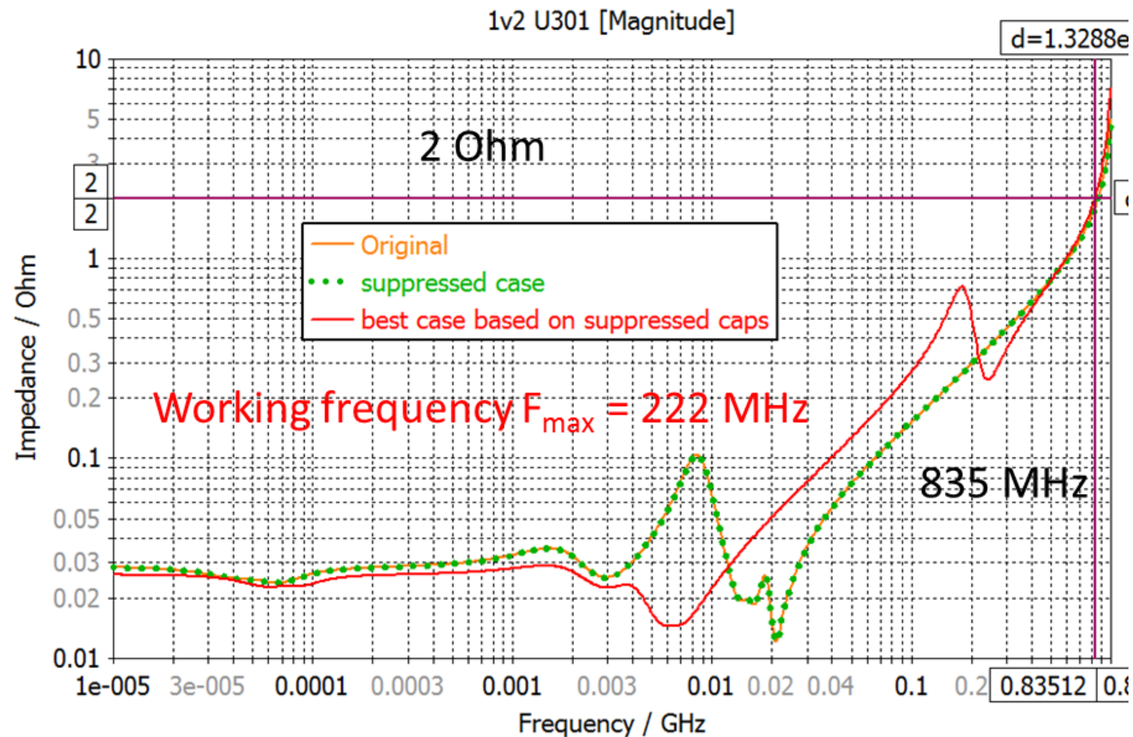


SI/PI analyses for EDDEMA

Example of Power Integrity analysis

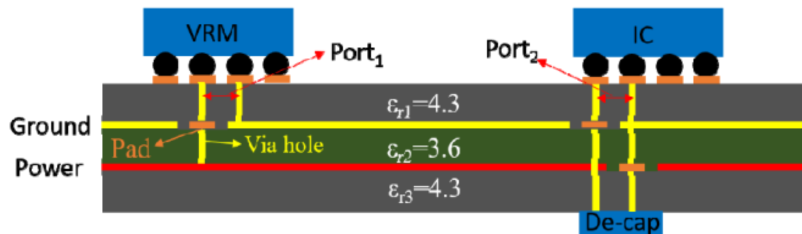
1.2 V power supply of μP

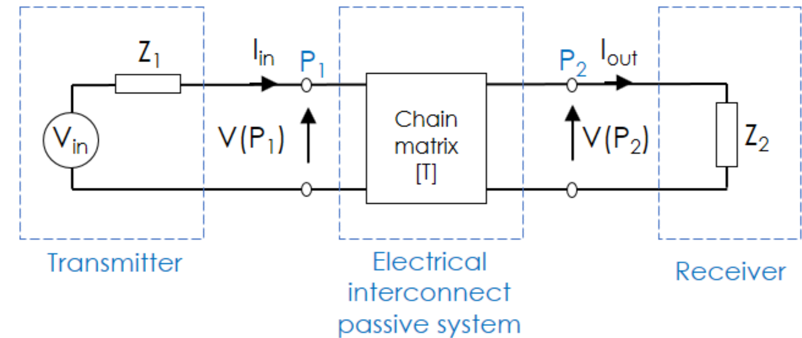
- Voltage range : 1.14 V-1.26 V
- Ripple: 5%
- I_{max}= 30 mA in datasheet
- Z_{target}= 2 Ohm

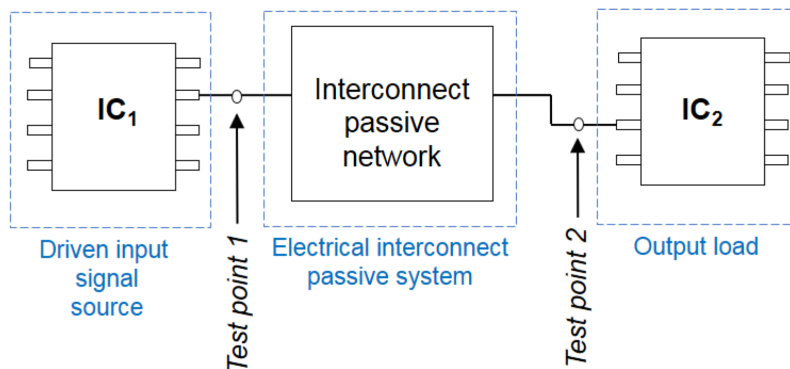


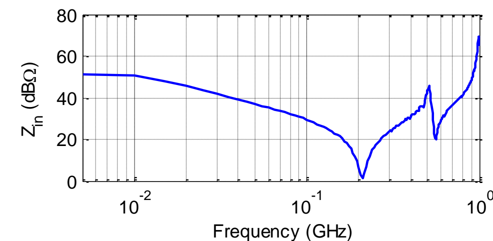
SI/PI analyses for EDDEMA

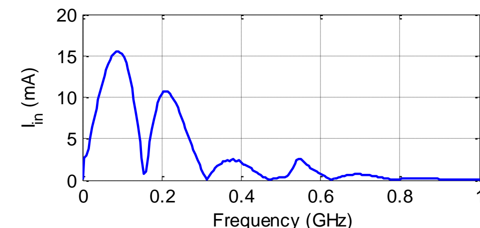
PCB extraction technique development







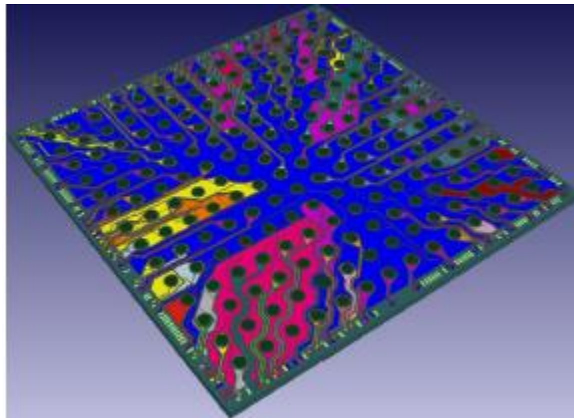


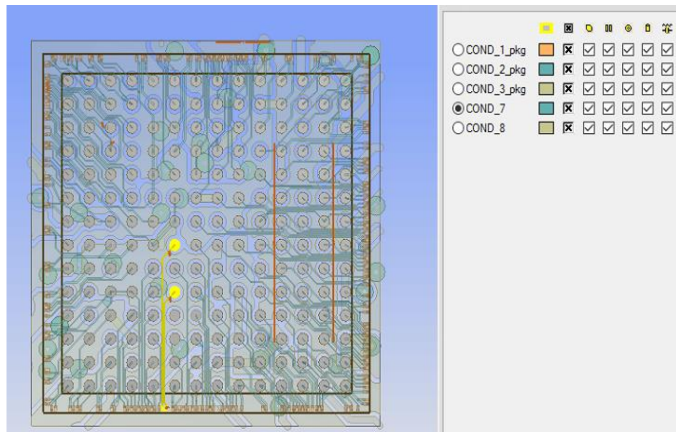


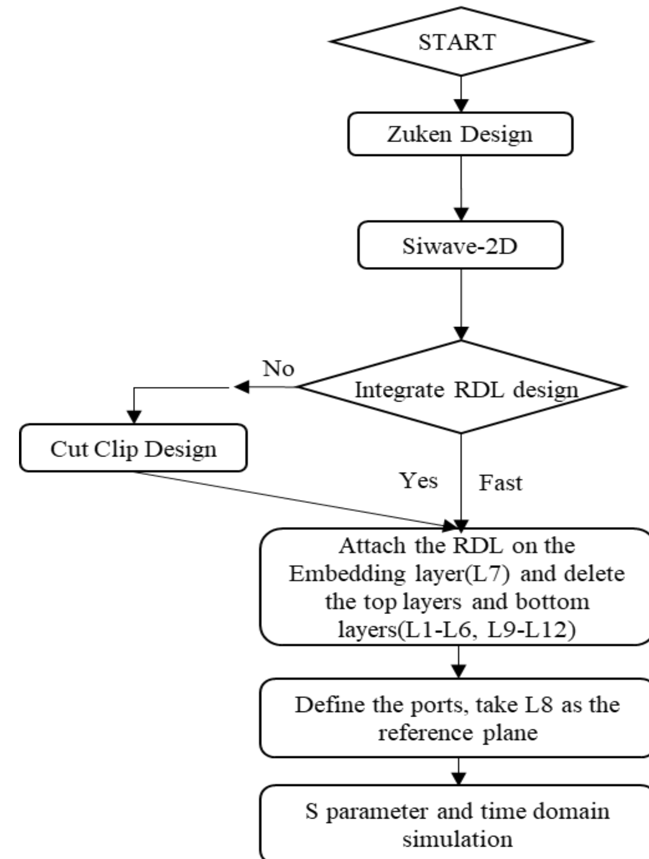
Xu, Z., Ravelo, B., Gantet, J., & Marier, N. (2018, August 19). PCB access impedances extraction method of in-situ integrated circuit. Advanced Electromagnetics, 7(3), 108-116.

SI/PI analyses for EDDEMA

RDL and analyses methodology



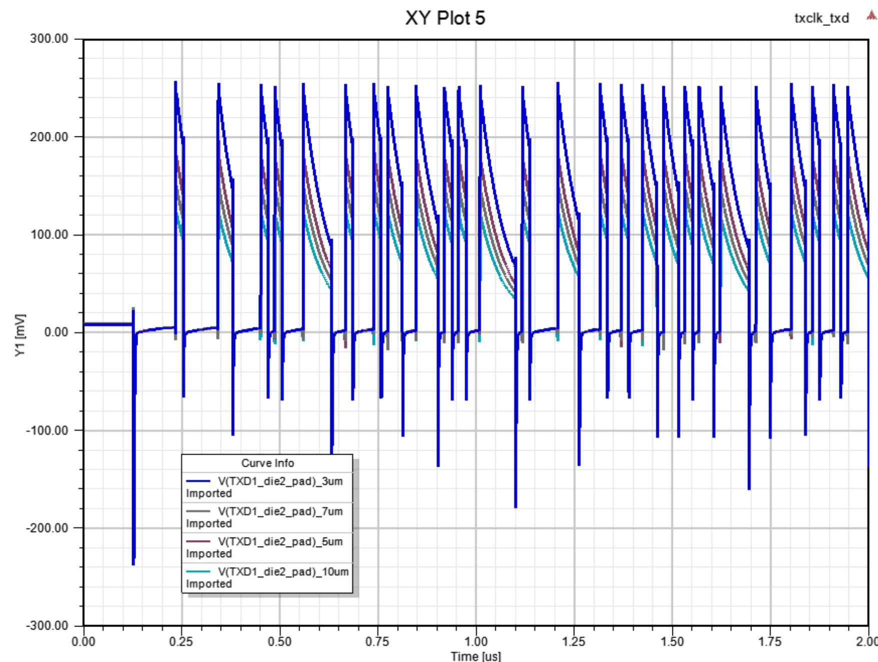




SI/PI analyses for EDDEMA

Crosstalk on the RDL

Here is the crosstalk results when RXCLK active and TXD2 deactive load with deactived IBIS models. The results presented maximum 130mV, this value may have risk in the future test, however, it is still under the design limit (0.3V). The different gap distances smaller than 15 μm(10 μm, 7 μm, 5 μm, 3 μm) have been simulated.



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IC-EMC model establishment

Input data

Technology	Year	Supply	Density of cells /mm^2	Clock frequency (MHz)	Typ. current per gate	Typ. switching delay in typ. loading conditions
0.8µm	1990	5 V	15 K	4-90	0.9 mA	0.5ns
0.5µm	1993	5 V	28 K	8-120	0.7 mA	0.3ns
0.35µm	1995	5-3.3 V	50 K	16-300	0.6 mA	0.2ns
0.25µm	1997	5-2.5 V	90 K	40-450	0.4 mA	0.12ns
0.18µm	1999	3.3-2.0 V	160 K	100-900	0.3 mA	0.1ns
0.12µm	2001	2.5-1.2 V	240 K	150-1200	0.2 mA	70 ps
90 nm	2004	2.5-1.0 V	480 K	300-2000	0.15mA	40 ps
65 nm	2007	2.5-1.0 V	900 K	500-3000	0.1 mA	25 ps
45 nm	2009	2.5-0.7 V	1500 K	800-5000	0.08 mA	15 ps
32 nm	2011	1.8-0.7 V	2500 K	1000-7000	0.06 mA	10 ps
22 nm	2014	1.0-0.6 V	4000 K	1000-10000	0.05 mA	7 ps

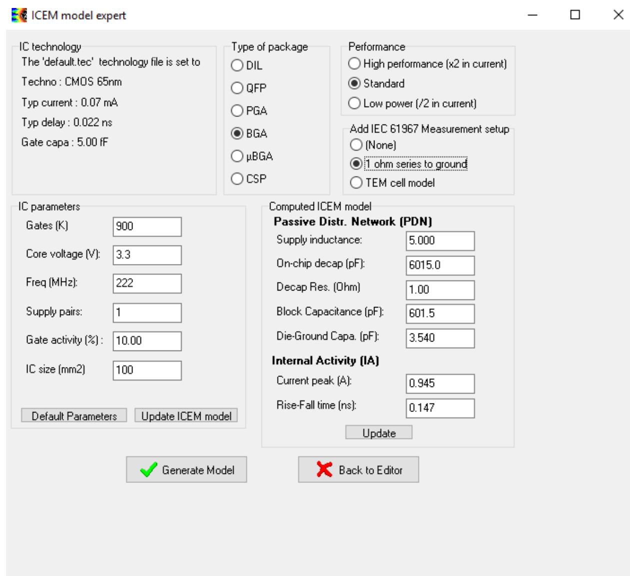
“Cookbook for Integrated Circuit model ICEM , project number 62014-3.”

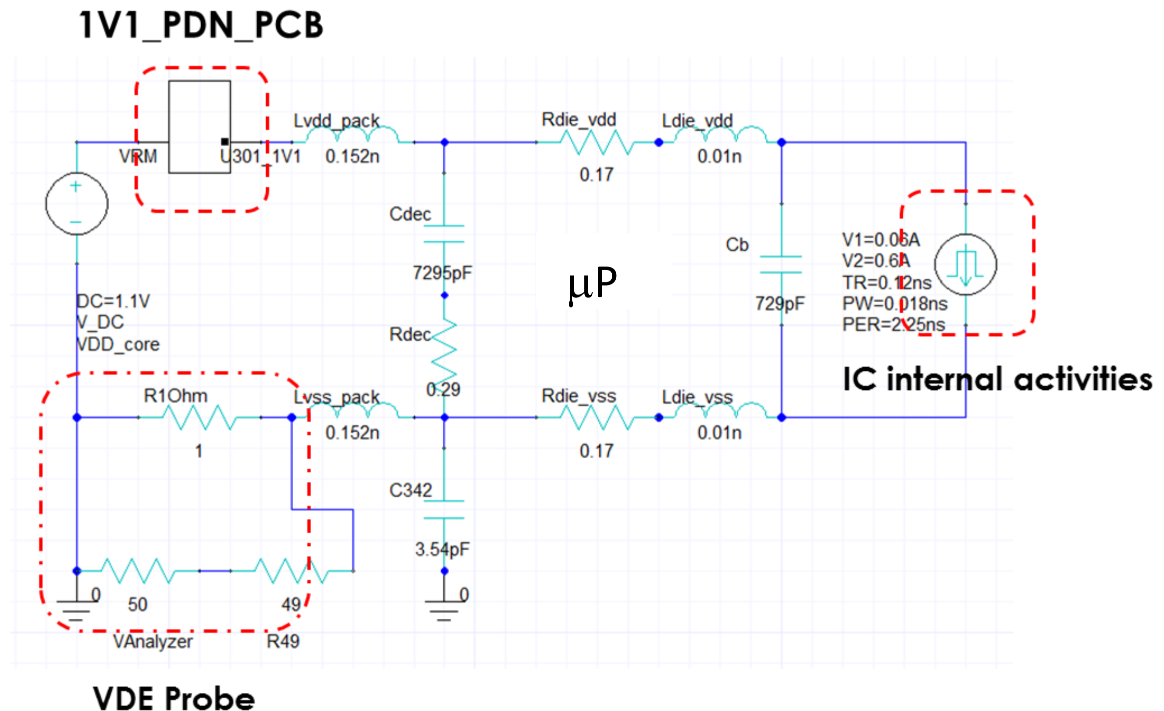
Package	TFBGA201	
Overall dimensions (mm)	10 x 10	
Height (mm)	A max	
Pitch (mm)	0.65	
Power and ground pins	66	
Signal pins	135	
Total pins	201	

	µP	Imager	Transceiver	FLASH
Technology	45 nm	65 nm	65 nm	65 nm

IC-EMC model establishment

Singal IC's IC EMC model

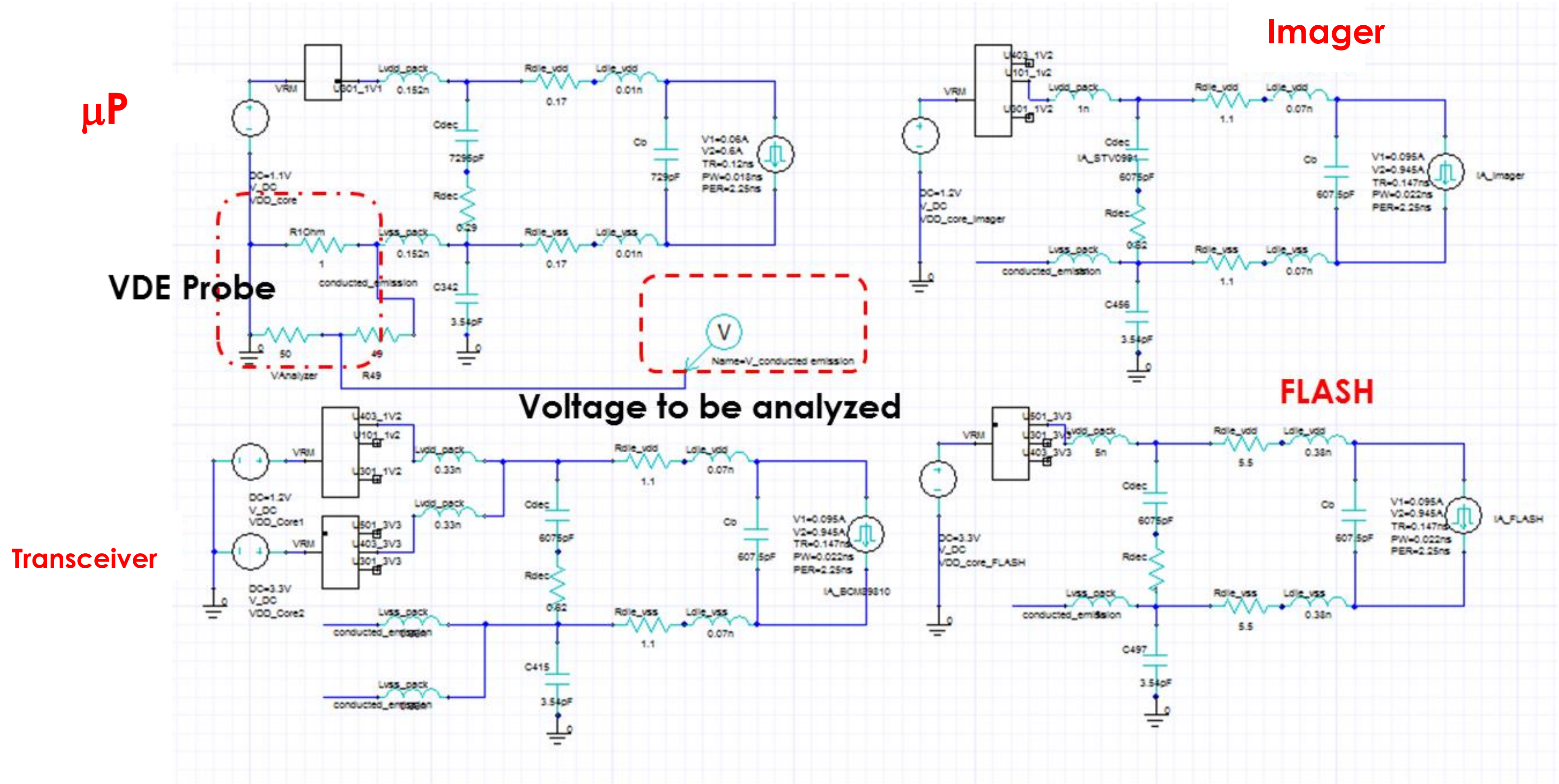




Boyer A, Sicard E, Dhia S B. IC-EMC, a demonstration freeware for predicting Electromagnetic Compatibility of integrated circuits[C]//Electromagnetic Compatibility and 19th International Zurich Symposium on Electromagnetic Compatibility, 2008. APEMC 2008. Asia-Pacific Symposium on. IEEE, 2008: 16-19.

IC-EMC model establishment

Conducted Emission simulation schema



Future works

Measurement on the product and compare to the surface mounted case on EMC performance

EMC measurements	Conducted susceptibility	Radiated Susceptibility	Conducted Emission	Radiated Emission	Electrostatic Discharge
Standards	ISO 7637-3, ISO 11452-4	ISO 11452-2	CISPR 25	CISPR 25	ISO 10605
Objectives	Check the immunity of EUT to transient and inducted common mode disturbances coupling on the signal line and harness	Check the immunity of EUT to EM field in the dedicated frequency band	To evaluate the RF disturbances conducted by EUT and its power supply wiring.	To evaluate the RF disturbances radiated by EUT and its power supply wiring.	Check the resistance of EUT to ESD produced directly by operators
Embedded case	***	***	***	***	***
Surface mounted case	*** -	_***	***	***	***

Acknowledgement

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Thanks for your attention