Molding materials performances experimental study for the 3D interposer scheme

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Abstract

Wafer level encapsulation is necessary in 3D technologies to ensure good chip stability and no material degradation during chips post-processing. It has been proven as one of the most challenging steps. Specifically to 2.5D, the use of silicon passive interposer leads to dedicated process sequence because of warp management on large and thin die. In this paper stacking first approach is presented to propose a solution for those challenges. We focus on molding materials evaluation: experimental results are presented with test wafers that simulate chips on interposers and on which both epoxy and silicone based molding materials are applied. A study of the vacuum lamination quality, the induced bow and its process stability for these technology steps is reported in this paper.

Key words: Wafer level molding, Encapsulation, Vacuum lamination, 3D integration, Silicon interposer, Epoxy, Silicone

Introduction

In the current move from standard CMOS to 3D ICs, the 2.5D technology approach using passive silicon interposer has many advantages [1]. Design and mask costs are reduced as a mix of mature and advanced nodes can be integrated. Interposer leads to high connectivity density between chips, performances are optimized thanks to shorter interconnection lengths, CTE mismatch is reduced between chip and substrate (BGA for example), and lateral heat dissipation can ease thermal management. For these reasons many developments to reduce cost of manufacturing, which is a key challenge [2], are on the way. Even full volume production of first heterogeneous 28nm 3DIC FPGA has been recently announced by Xilinx with TSMC’s CoWoS technology inside [3].

In the first part of the paper advantages of Chip on Wafer approach used for 2.5D technology will be exposed. Usual process includes an encapsulation step. Various integration routes can be used, among others: wafer reconstruction [4], molding achieved simultaneously to underfilling thanks to additional compression step [5, 6], carrier-less wafer handling with molding polymer acting itself as a carrier [2], stacking last and stacking first [1]. For the experiments, the stacking first approach was chosen. Different molding materials were laminated on test wafers by vacuum lamination, then planarized by grinding, and integrated with temporary bonding, backside grinding, oxide thin film deposition, up to the debonding step. The quality of the lamination, the wafer bow analysis throughout the process will be presented.

Chip on wafer

Realizing a chip-interposer assembly can be made by choosing various integration schemes described in [1]. To realize the 2.5D assembly, Chip on Chip (CoC) approach is the common but Chip on Wafer (CoW) can also bring advantages. As the trend for interposer size is to be increased, bow is a major concern and CoW tends helping to reduce it. Higher thermo-compression quality bonding is achieved and electrical testing of bumps at wafer level is also possible.

The 2.5D desired assembly consists in bonded chips on a thin diced interposer, with molding protecting material in-between chips, and the interposer with its backside processes including bumps. The whole is then ready to be stacked on substrate. Achieving this CoW process can be done with two main schemes, depending on the moment when chips are bonded or when back side processing of interposer is realized [1]: “stacking last” when the chips are stacked after the thinning of the interposer and its backside processing and “stacking first” when chips are stacked to the interposer before the temporary bonding for interposer thinning and backside processing.
A first common step is to obtain frontside interposer wafer (figures 1 and 2), including Back End Of Line (BEOL), TSVs and frontside copper pillars. Then the processes differ.

In stacking last approach (figure 1) the wafer is bonded to temporary carrier to allow backside processing and bumping. Then after having realized a double-temporary bonding sequence with planarity and thermal handle as key parameters, chips are stacked by thermo-compression (TC) onto the interposer, with underfilling at the end. Limiting topology thanks to wafer encapsulation and planarization can reduce taping and debonding issues. Other possibility to avoid double temporary bond is stacking on thin interposer using specific chuck.

Stacking first approach (figure 2) begins with chips stacking on wafer by TC, without thermal concerns or stack difficulty as no temporary bonding layer is present yet. This leads to better interconnection. Chips encapsulation is made with the vacuum lamination of the molding polymer. The molding is planarized by mechanical grinding, landing on top of the dies. This gives better heat dissipation properties to the assembly, as exposed chips could enable direct contact between silicon and a post-applied heat spreader to boost cooling performances. Then temporary bonding to a carrier is made with bonding capability to handle back-side and bumping processing. At the end the interposer wafer is debonded and taped to allow its dicing. Here the key parameter is molding and taping materials compatibility in term of adhesion.

Stacking first flow is preferred. Indeed one major drawback of stacking last approach is to process stacking by TC on thinned wafer. This is more complex to solve than the need with stacking first to have a temporary bonding that can handle backside processing.

The advantages and drawbacks of each approach are summarized below (Table 1)

### Table 1: Stacking first and stacking last advantages and drawbacks

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Stacking last</th>
<th>Stacking first</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advantages</td>
<td>Standard interposer 3D integration process flow</td>
<td>TC on thick wafer</td>
</tr>
<tr>
<td>Interposer can be tested before stacking (KGD)</td>
<td>Max 1 temporary bonding</td>
<td></td>
</tr>
<tr>
<td>Top chip assembly (TC) on thin wafer</td>
<td>C2W without interposer testing</td>
<td></td>
</tr>
<tr>
<td>Complexity : Si interposer flip &amp; up to 2 temporary bonding</td>
<td>Temporary polymer compliance with full processflow</td>
<td></td>
</tr>
</tbody>
</table>

Molding materials

Encapsulation functionality is to allow chip mechanical stability and that no material degradation occurs over time. The standard epoxy-based molding materials used in packaging technology ensure high mechanical protection thanks to high Tg, Young modulus and bending strength. To limit bowing of final package, a high filler content rate gives a CTE to material in the range of substrate’s one. But in
CoW process molding material also needs to induce as low as possible bow at wafer level and to show good behavior under planarization. This means it has to have low Young modulus, CTE, tensile strength and elaboration temperature. We clearly see here that molding compound for CoW technology will be a compromise between many parameters. Adapted epoxy-based can be used, as well as silicone-based material that can have lower \( T_g \) and modulus but higher CTE.

In our experiments one adapted epoxy-based and two silicone-based compounds have been tested. Their main material parameters are presented below (Table 2) and compared to standard packaging material. Dry film sheets are used instead of liquid compounds to allow the use of standard 300mm lamination tool.

<table>
<thead>
<tr>
<th></th>
<th>Standard Epoxy based</th>
<th>Adapted Epoxy based</th>
<th>Silicone based 1</th>
<th>Silicone based 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulus (GPa)</td>
<td></td>
<td>~10</td>
<td>1.7</td>
<td>2.4</td>
</tr>
<tr>
<td>DMA@RT</td>
<td>15-25</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTE ( \alpha ) (ppm/K)</td>
<td>~10/-30</td>
<td>1675</td>
<td>76/107</td>
<td>14/64</td>
</tr>
<tr>
<td>( T_g ) (°C)</td>
<td>-150</td>
<td>140</td>
<td>139</td>
<td>151</td>
</tr>
<tr>
<td>( T_{	ext{elab}} ) (°C)</td>
<td>-150</td>
<td>150</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Tensile strength (Mpa)</td>
<td>high &gt;100MPa</td>
<td>high</td>
<td>19</td>
<td>2.0</td>
</tr>
</tbody>
</table>
| Filler dia (µm) | > 10                | Ave 10              | Ave 5            | Ave 2

* \( \alpha \) is CTE for \( T<T_g \), \( \alpha \) for \( T>T_g \)

Table 2: Molding materials parameters

Simulation and experimental studies can be done to select the best molding material. Simulations on full-sheet allowed comparing materials by giving tendencies on induced bow and stressing [1]. Introducing asymmetric design to simulation led to be closer to real wafers with embedded chips. Bow calculation shown high values with thinned interposers but didn’t take into account the fact that interposer is bonded to carrier when being thinned. An experimental comparison only full-sheet was made and shown the limitation of this approach. Indeed data from simulations and experiment deviated strongly, which was assumed to be due to thermoplastic and viscoelastic deformations that had not been included into the model.

An experimental study monitoring the material stability and wafer bow on wafer with topologies appeared necessary and is being explained in next part of this paper.

Experiment

A) Test wafer design and manufacturing

To study the molding performance for chip encapsulation, before using complex interposer with real stacked chips we designed some 300mm all-silicon-made test vehicles wafers (TV). The design fits the requirements for real interposers: chips of various lateral sizes in the range of 5mm to 30 mm with height around 100µm, stacked on wafer interposer with 30µm interconnection height material and an interchip separation width of 0.5mm to 1.5mm (figure 3).

![Figure 3: Layout of chips on interposer](image)

Below (figure 4) are pictures of our 300mm TVs. Two designs were defined: trenches widths that represent interchip spacings of 0.5mm and 1.5mm. Lateral sizes of respectively 12x24.5/7x7/7x17mm² and 12x23.5/7x8/7x14mm² are simulated, with a common total height of 130µm representing a 100µm height chip with its 30µm height interconnections. These TVs have been obtained through standard microelectronic processing steps.

![Figure 4: 300mm test vehicles (sizes in mm)](image)
B) Experimental process flow

Hereafter is described the applied process flow to TVs to study molding material performances (figure 5).

Firstly lamination of a 200µm thick dry film has been done with Takatori TEAM300 vacuum laminator tool. Then the wafer has been annealed at temperature and time recommended for a total polymerization ratio. Planarization by grinding of molding material down to the chip top-side has been achieved to reveal chip, while trenches remain filled with this material. Molding material performance is then submitted to stacking first typical processes: temporary bonding on the chip side either with 3M Wafer Support System (WSS) or Brewer Science ZoneBond (ZB) processes, back-side silicon thinning from 775µm to typical interposer thicknesses of 100 to 200µm, silicon oxide deposition at 150°C which is the critical thermal step of back-side processing, and at the end debonding on a temporary tape (taping). During the process we characterized wafers in terms of bow (standard SEMI specification), and bonding quality has been verified with scanning acoustic microscopy (SAM).

C) Results

Top views of laminated molding films after annealing are shown on figure 6. For both TV types, adapted epoxy-based material has filled the trenches contrary to silicone-based ones. SEM pictures on trenches confirmed a total unfilling (figure 7) for silicon-based polymer versions, making not relevant further testing of stacking first steps. The present study then focused on the adapted epoxy-based material performances. After lamination and annealing, high bow values (concave shape): ~1.5mm were measured on VTs, and will be discussed later.

The planarization of molding films was done by material grinding (figure 8, a1, a2, a3). The grinding process was optimized to land on top of the silicon dies. For both TVs types, after grinding the polymer fills completely the trenches (figure 9). However, for the two first wafers we noticed that some areas at the wafer edge presented no polymer in the trenches. This could be due to the bad wafer clamping on the grinding chuck, due to the high wafer bow. Then three TVs have been bonded to temporary carriers with varying process to gain information on material performance: on 0.5mm-width trenches TV we tried both ZB and WSS processes and on 1.5mm TV we tried WSS only. Then silicon back grinding has been processed to decrease silicon thickness from 775µm to around 200µm. We see on scanning acoustic microscopy (SAM) pictures that polymer filling inhomogeneity directly impacted bonding quality at the edges (figure 8, b1, b2). At the end a 2µm-thick SiO2 layer has been deposited in plasma chamber at 150°C. If cracks and delaminations occurred on the edges, nevertheless good behavior is shown in center. The best results were obtained with TV3 that benefited of optimized polymer grinding parameters then better further bonding.

The outputs information of this step are then: 1) the laminated wafer bow need to be decreased, in order to improve the wafer clamping on process chuck and 2) epoxy-based molding material are compatible with both WSS and ZB bonding processes.
Debonding the temporary carrier and taping the interposer wafer have been achieved successfully over large areas (figure 8, d_2, d_3) which ends successfully the integration test of epoxy-based material. The effect of unfilling at the edge is again seen as temporary glue remains where trenches were unfilled.

A focus on wafer bow monitoring during process is presented (figure 10). It shows bow evolution for the three TVs encapsulated with adapted epoxy-based material, and bows of laminated silicone-based materials. As mentioned earlier, after lamination and hard bake steps, a high bow is observed with epoxy-based. Thinning the molding material by grinding leads to an almost total release of induced bow. The whole process doesn’t induce bow out of a range of +/-300µm. This good result shows that apart lamination + hard baking step this molding material is suitable for automatic tool handling in term of wafer bow.

Silicone-based induced bows after lamination + hard baking are significantly lower, in the range of 400µm.
Conclusion

Two types of molding materials have been tested in stacking first integration process flow. Concerning silicone-based films the lamination doesn’t fill the trenches for the test vehicle design and lamination temperature we used. Then we could not go through testing process flow. Nevertheless as this kind of material shows very low young modulus it still presents high advantages. We are continuing work with new material to improve filling, as an example by tuning its viscosity that seems the relevant parameter.

Adapted epoxy-based material has succeeded the integration process flow and seems to be a good encapsulating candidate for stacking first approach. But while bow is maintained in the range of +/-300µm during process flow which is acceptable for automation tools handling, the high initial bow of 1.5mm after lamination is detrimental to this technique as such laminated wafer cannot be handled by grinding automatic tool. Furthermore, such a bow probably induces some killer defects into the interconnection between chip and wafer, or into CMOS. A way to reduce this bow could be to tune hard baking.

Once optimized, both materials should be integrated on real structures, for instance to encapsulate DRAM chips on passive interposers.

References


