Application of WDoD™ technology for the manufacturing of a leadless pacemaker

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Abstract

3D PLUS has patented an innovative 3D technology based on the stacking of Know Good Rebuilt Wafers with only Know Good Dies, named WDoD™. This technology is compared with Wafer-to-Wafer technology based on TSV and with Embedded IC in PCB technology. An innovative application of leadless pacemaker module developed with SORIN and manufactured by 3D PLUS is described.

Key words: WDoD™, leadless pacemaker, 3D IC, RDL, yield, SIP

1. Introduction

More and more applications are requiring electronics shrinkage in order to integrate high performance devices in a limited volume. Consumer market is driving 3D technology as smartphones, tablets and many handheld devices require advanced features in light and thin products.

Those requirements are being fulfilled by fan-in or package on package (PoP) technologies but real 3D low profile components are just being introduced for specific applications. Through silicon vias (TSV) is the main driving technology even if several drawbacks are still slowing-down its introduction such as:

- Highly specific design making any multi-sourcing difficult to achieve
- Final 3D component yield drastically decreased as wafer level yield is good enough
- TSV yield
- TSV cost

Alternative technologies are being developed to get through those issues mainly for highly heterogeneous systems in package for which multi-sourcing is a must. 3D PLUS proposes a unique solution that overcomes many TSV issues:

- High yield as known good rebuilt wafers are stacked
- Multi-sourcing is very much compatible with this technology

Wafer level package manufacturers include double-face redistribution layer (RDL) in their roadmaps as a first step for 3D integration with PoP solutions. 3D PLUS is a step ahead with stacking several rebuilt wafers with its patented bus metal interconnect.

2. WDoD™ technology description

A trade mark: Wirefree Die on Die “WDoD™” has been registered by 3D PLUS. This technology avoids these disadvantages of TSV technology and is very well adapted to the Systems In Package as well as too small and large volumes for the following reasons:

- Use of standard wafers without TSV (Multi-sourcing).
- Each layer testing prior to stacking; only “Known Good Reconstructed Wafer” is stacked.
- Possibility to stack Known Good Burn-In Wafers among Known Good Rebuilt Wafers.
- Thermal management between logic IC and memory can be adapted, thanks to the epoxy resin in between them.
- Very small form factor, - Several dice/level are possible
- Thickness of each layer: 250 to 100µm (10 levels/mm).
- Technology can be applied to 300 or 200 mm wafer or panel form
WDoD™ resulted in the registration of more than 25 patents worldwide. The flowchart is shown on figure 4.

The steps 1 to 6 are used by the manufacturers of the Rebuilt Wafers with well-known eWLB or RCP technology:
- Pick-Flip and Place of KGD from the die wafer on an thermal-release tape on a silicon carrier (300 or 200 mm diameter)
- Compression molding with epoxy resin with silica fillers
- Know Good Rebuilt Wafer grinding in order to decrease total thickness to 250 µm or less
- Fan-out built-up with Redistribution layer process (see figures 1 and 2)

The next steps 7 to 13 concern the WDoD™ process with edge connection. (see figures 4)

Figure 3: Example of Quad-Die DDR3 RDL fan-out

Figure 4: WDoD™ stacking process

- Step 7: gluing of first Know Good Rebuilt Wafer
- Step 8: sequential staking and gluing of Know Good Rebuilt Wafers
- Step 9: dicing of rebuilt and stacked wafers
- Step 10: plating of dicing streets with electroless process
All these steps are collective at the wafer level. Final laser patterning on the plated edges of each module is the final step before electrical test.

3. Leadless pacemaker built with WDoD™

More than 1 000 000 pacemakers and more than 200 000 defibrillators are implanted in the world each year. All these devices need 3D heterogeneous integration to reduce the size of the electronics.

Global market revenue for pacemakers in 2012 was $4.3bn

Leadless pacemakers are expected to be revolutionary to the CRM (Cardiac Rhythm Management) industry, especially in the US and EU by eliminating the need for lead replacement.

The state of the art for the volume of a subcutaneous pacemaker is 8 cm$^3$ and for a leadless pacemaker is 1 cm$^3$.

3D PLUS has designed with SORIN GROUP and manufactured a module in the frame of
a feasibility study of a leadless pacemaker directly implanted inside the heart. This is only feasible thanks to a 16 times shrinkage of the volume versus conventional pacemaker.

This challenge was fulfilled thanks to the heterogeneous advantage of 3D PLUS stacking technology, allowing the stack of WDoD™ rebuilt wafers (only for components available in bare dies) and PCB levels on which can be soldered SMD components.

![16x shrinkage](image)

**Figure 5: 3D concept (a) and real picture of the leadless pacemaker (b)**

The module has 5 layers stacked using 3D PLUS WDoD™ process. The layers are stacked on wafer level. 2 layers have known good passive (30) and active components (3) and are reconstituted wafers using fan out WLP technology eWLB. RDL pitch is 50µm. The 3 other layers are PCB based.

External sides of this module can be also populated by additional components and allow the interconnexion with other sub-modules (see figure 6).

![Module integration](image)

**Figure 6: 3D module integration in the leadless pacemaker**

Dimensions of the module are: 2.3 x 5.2 x 7.3 mm (figure 5) - volume is less than 1 cm³. Bus metal laser pitch is 250 µm. Bare dice are ASICs and silicon capacitors. SMD components are mainly capacitors.

4. **Yield aspect of WDoD™ versus alternative technologies**

3D IC TSV wafer level stacking raises the issue of yield and consequently cost.

For example, if 4 levels of wafers are stacked and if the yield (percentage of KGD) of each level is 95%, the global yield is expected to be 81%.

The wafer level stacking with TSV could be a nightmare regarding the yield. It was the main reason in developing the stacking of known good rebuilt wafers.

A lot of works and papers have been made for more than 10 years, with the stacking of the wafers with the use of Thru Silicon Via (TSV). The TSV are mainly used with the MEMS and imagers which have the need of a small quantity of TSV per chip (around 10 or less).

Unfortunately, the stacking of wafers with memory, Asic, processor did not work in production for the following reasons:

- The yield (Y1) of the wafer could be from 80 to 95% and the stacking of them leads to a global low yield,
- The yield of each TSV (Y2), generally the redundancy by 3 even by 6 are used in order to increase the yield, but the global yield of this step stays relatively low,
- The yield of the bonding of all the TSV of the wafer level “n” to the wafer level “n - 1” (Y3) has to be considered too,
- The multiplication of Y2, Y3 and “n” times Y1 leads to a very low global yield.

The comparison between Embedded IC in the PCB versus WDoD™ allows showing the main differences between these two technologies. The Embedded IC in the PCB presents some distinctive characteristics:

- The small die are used,
- The moving of the die during the curing of the PCB is more important than with the Fan-out technology,
- If several dice are embedded, the accuracy of their location could be critical (one of the advantage of the Fan-out is the use of an isotropic epoxy resin with silica filler),
- A full system with different die and passive components will have a large area due to the fact that it is 2D technique.
WDoD™ technology yield is directly linked to R.D.L technology yield. A tight cooperation must exit with our partner in order to define design rules in order to reach a very good yield.

3D staking process yield must be also considered. Results obtained during the leadless pacemaker modules manufacturing are promising and must be improved in order to take in consideration the relatively high cost of ASICs dies of this module.

5. Conclusions

Finally, we proved the feasibility of realizing prototypes of 3D IC heterogeneous integrated modules for all the electronics of a leadless pacemaker in a very small volume compared of the state of the art electronics for pacemakers which use 2D integration.

WDoD™ allowed a 16 times shrinkage of the volume versus conventional pacemaker where hybrid technology is used.

TSV wafer to wafer technology would not have permitted to stack all the components embedded in this module.

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References

