ASE GROUP

Fine Pitch Substrate for Cost Effective Flip Chip Package using Embedded Trace Substrate Technology

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ASE Europe

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ASE GROUP

EPP Substrates

- ASE Substrate Manufacturing
- Substrate manufacturing
  - Subtractive
  - MSAP/ SAP
  - EPP
- Cu pillar FlipChip fine pitch
  - Peripheral, Array, Pitches on Substrate
  - Reliability Results
- Wire Bond Finger Pitch (Hybrids)
- Conclusion

Substrate Manufacturing Sites

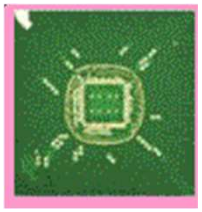
ASE GROUP

ASEMTL Shanghai outlook

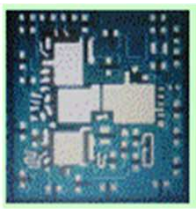
- Operation began from 2003
- Capital: $140M USD
- Revenue : 2010: $205M 2011: $185M 2012: $200M
- Capacity: 48kk pcs /Month based on PKG(27x27mm)
- Manpower : 1,750
  - Manufacture: 1300
  - PE, RD & QA: 280

ASEMTL Shanghai, China

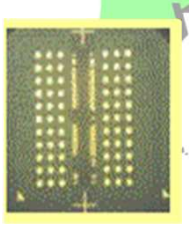
ASEMTL Kaohsiung, Taiwan



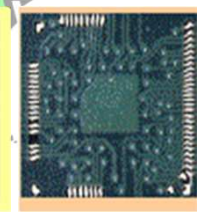
PBGA



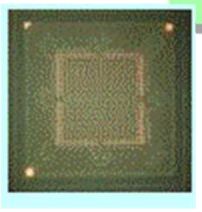
Module



BOC



TFBGA



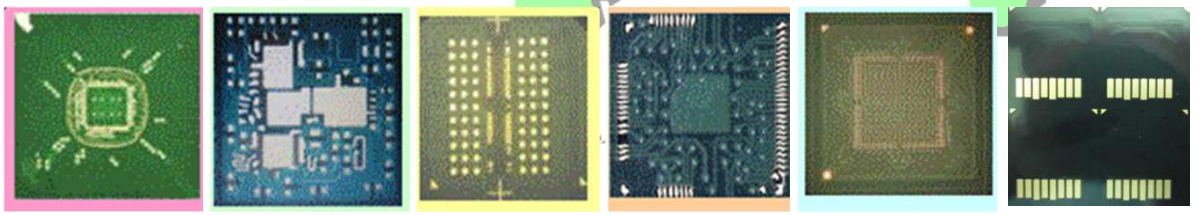
FCCSP

Substrate Manufacturing Sites

ASE GROUP

ASEMTL Kaohsiung outlook

- Operation began from 1995
- Capital: $135M USD
- Revenue : 2010: $110M 2011: $125M 2012: $140M
- Capacity: 22kk pcs /Month based on PKG(27x27mm)
  (future expansion to 36kk pcs/Month)
- Manpower : 1,000
  - Manufacture: 650
  - PE, RD & QA: 250



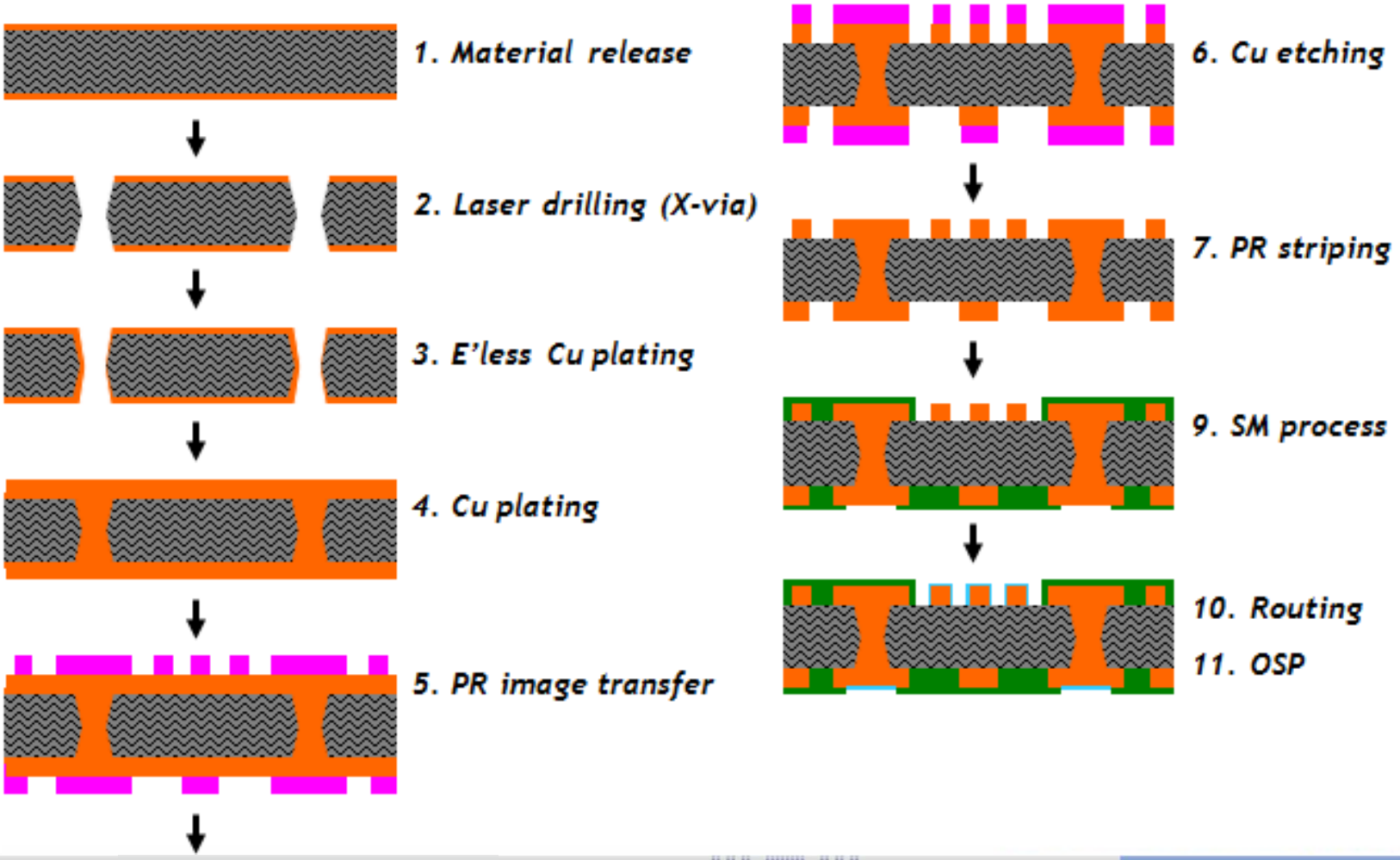
PBGA Module BOC TFBGA FCCSP HG

ASEMTL Shanghai, China

ASEMTL Kaohsiung, Taiwan

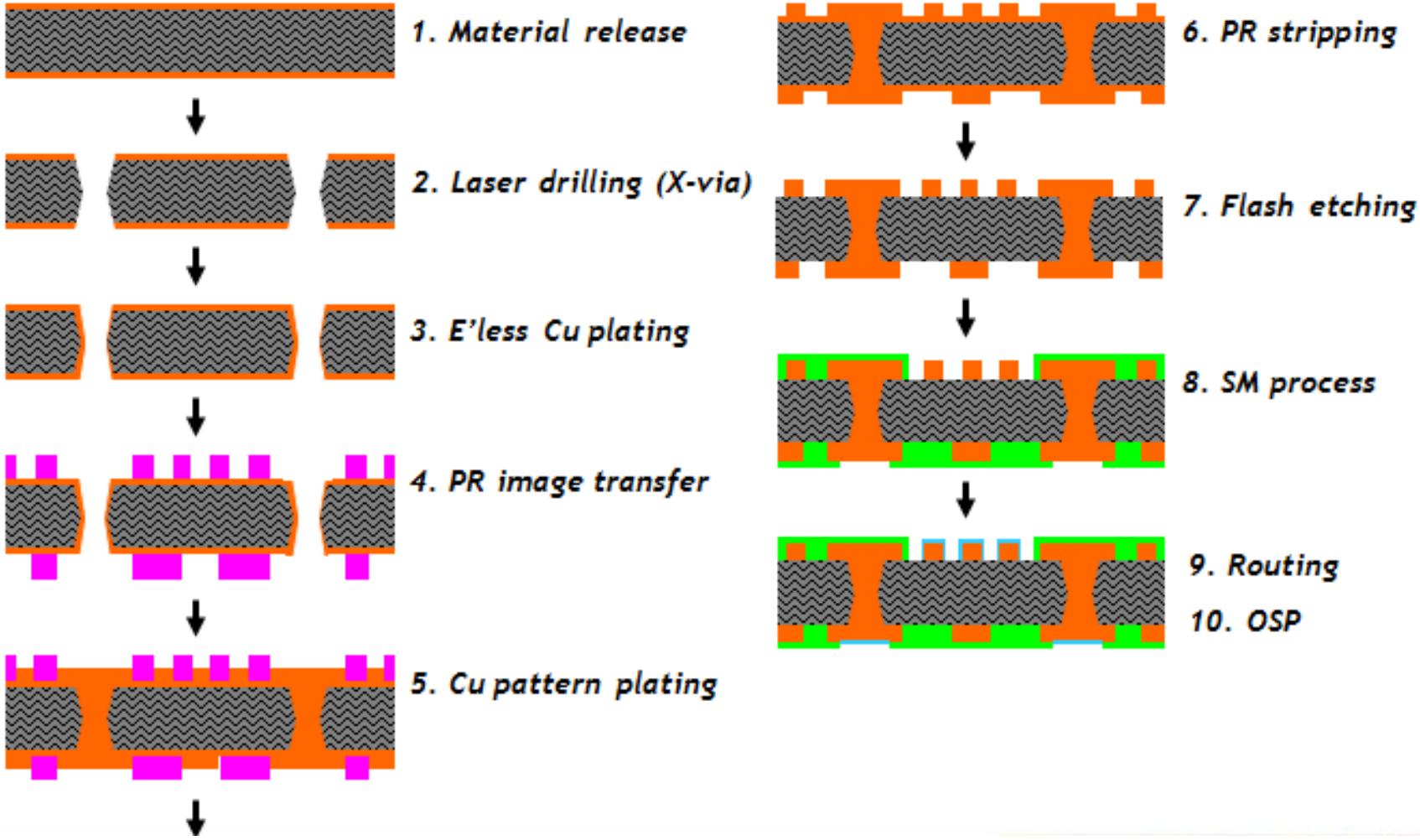
Substrate manufacturing

- Subtractive
  - Via drill, E'less Cu, Panel Plating, Tent'n'Etch



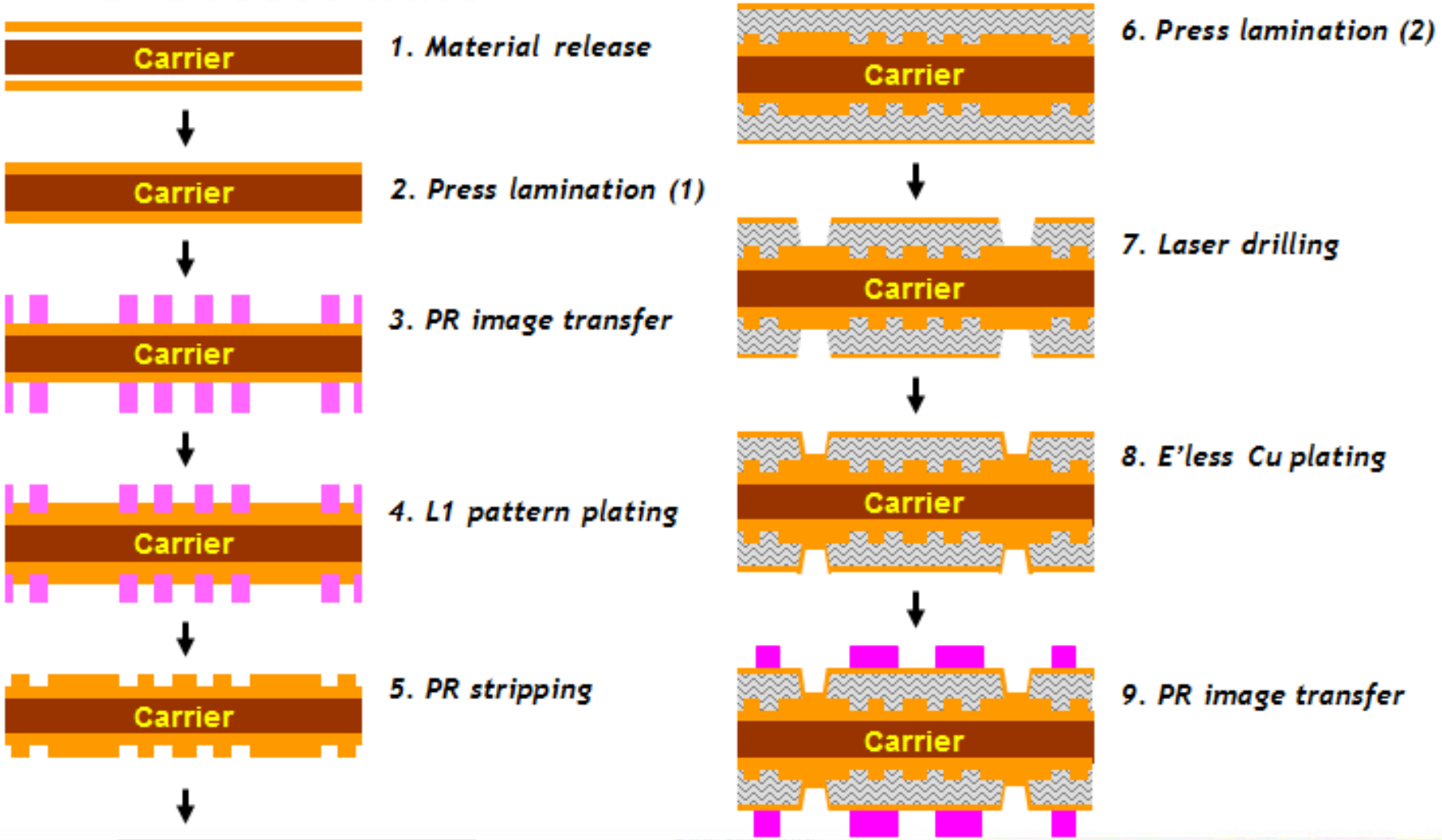
Substrate manufacturing

- MSAP (Modified Semi Additive Process), SAP
  - Via drill, E'less Cu, Pattern Plating, Flash Etch



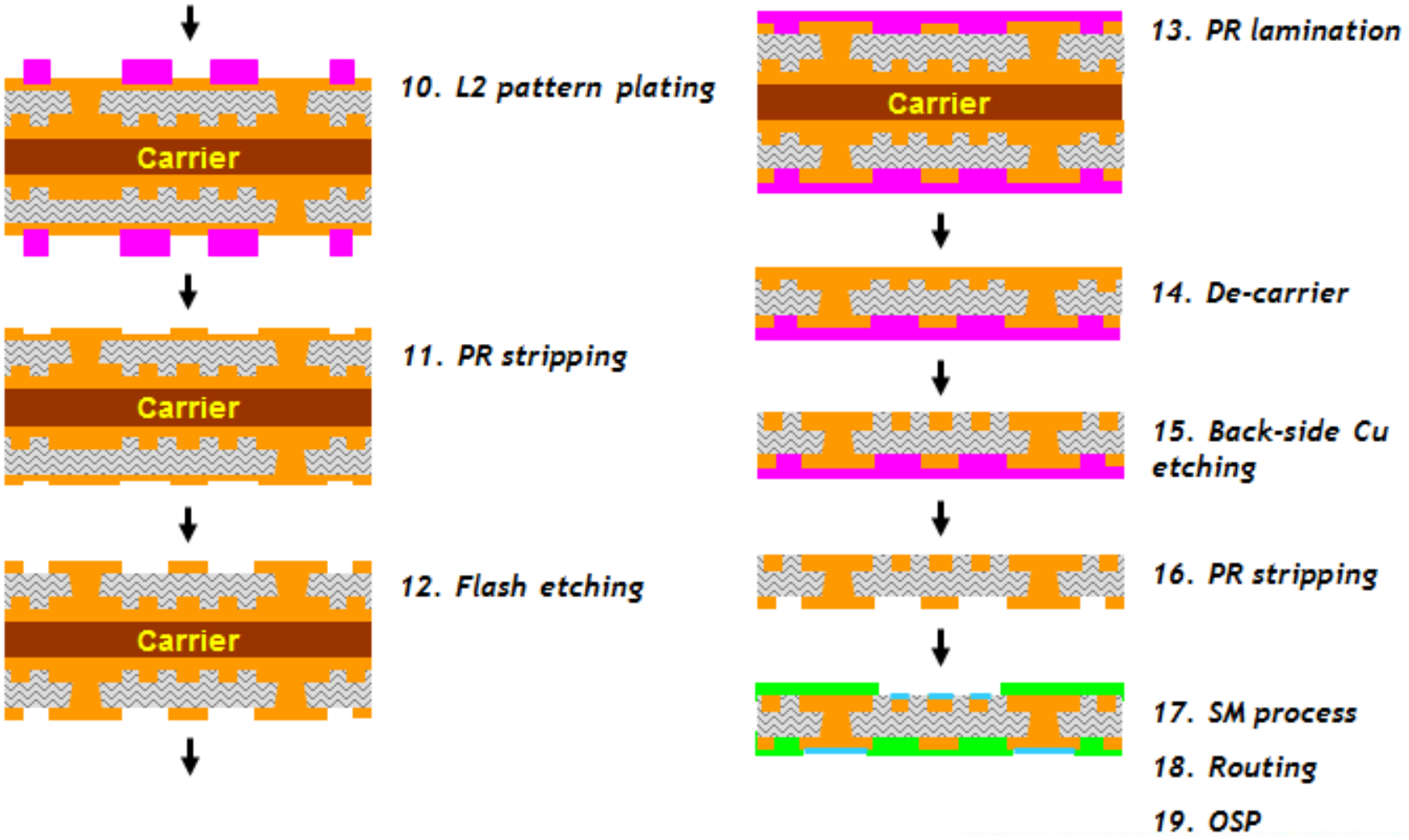
Substrate manufacturing

- EPP (Embedded Pattern Process) I
  - Pattern plating, Lamination, Via Drill, E'less Cu



Substrate manufacturing

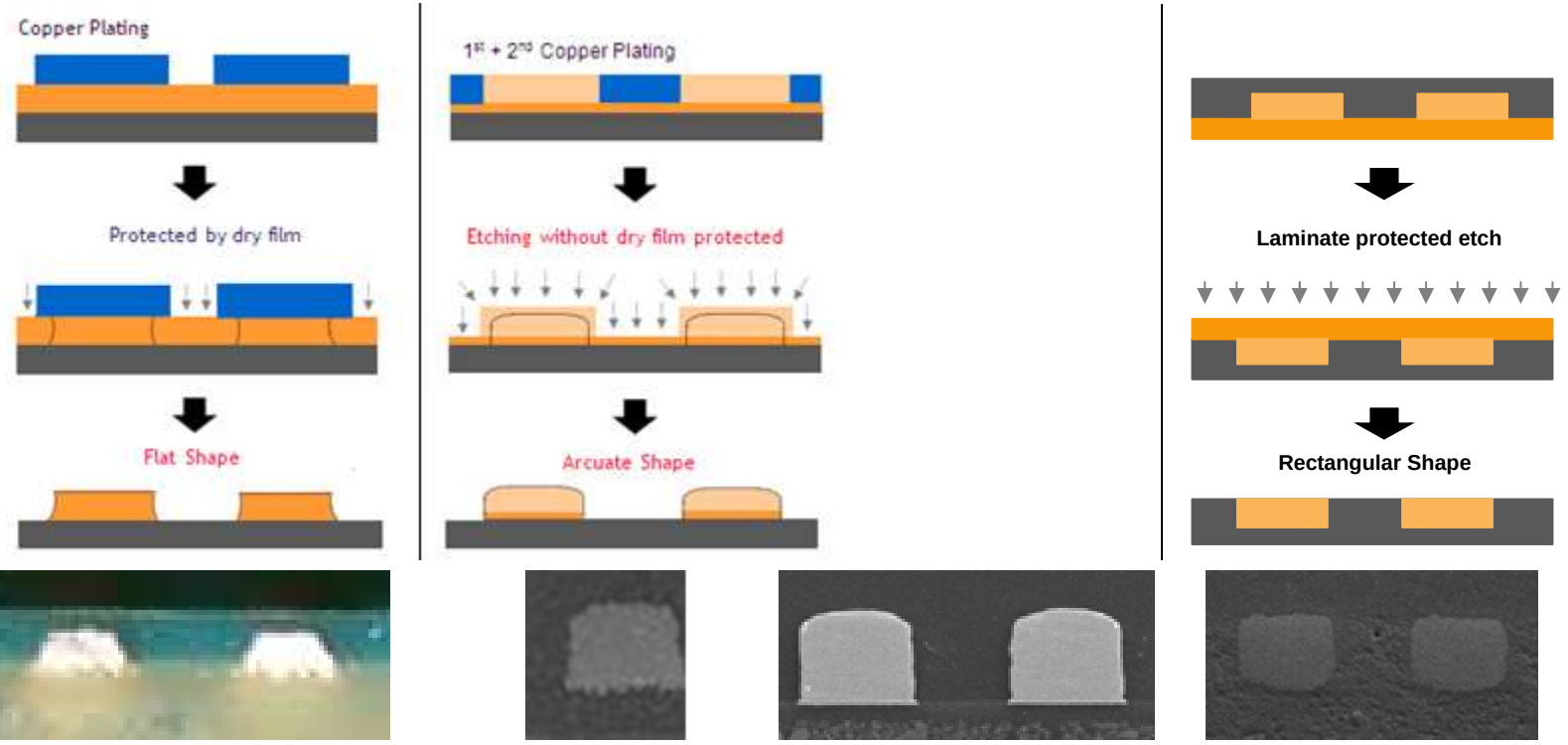
- EPP (Embedded Pattern Process) II
  - Pattern plating, Flash Etch, De-carrier, Backside Etch



Substrate manufacturing

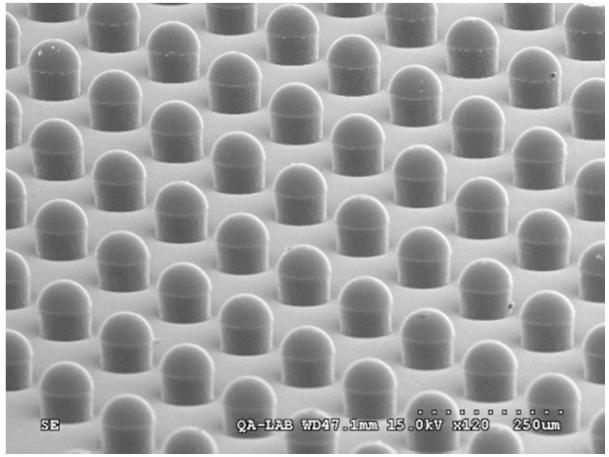
- Subtractive vs. MSAP vs. SAP vs. EPP

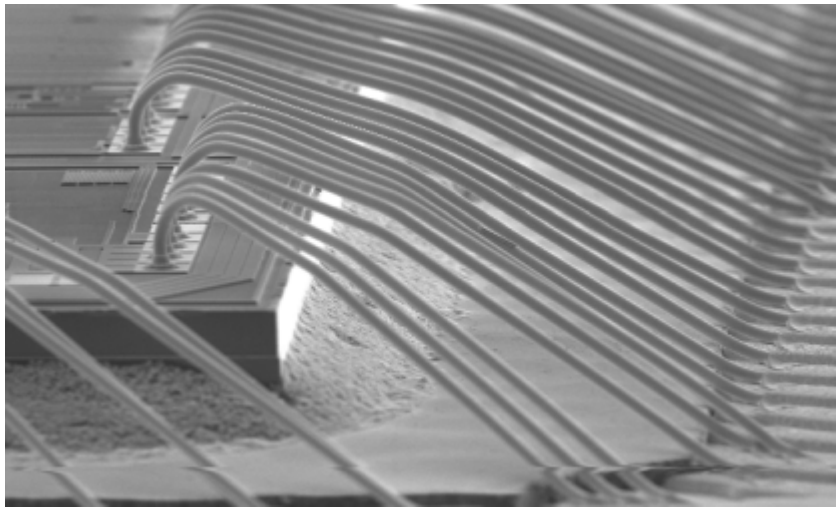
Process	Subtractive	MSAP	SAP	EPP
L/S, Pitch	50/50, 100	25/25, 50	20/20, 40	15/15, 30
Top	Flat	Round	Round	Flat
Head Foot Ratio	(1-(2/3CuT)):1	1:1	1:1	1:1



Fine Pitch Bumping

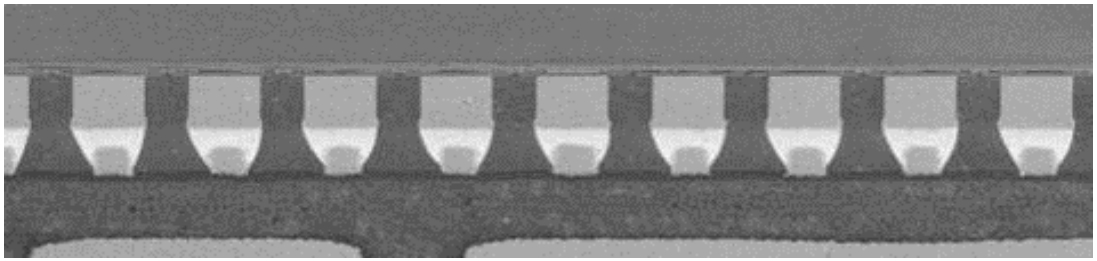
- N40nm / N28nm / N20nm wafer node and beyond
  - Small Die Size
  - High I/O Count
  - Small Pitches
- FC Bumping Pads
- Wire Bond Pads

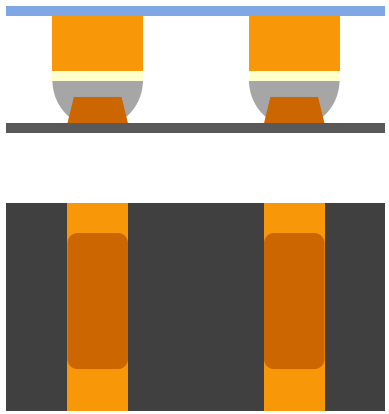


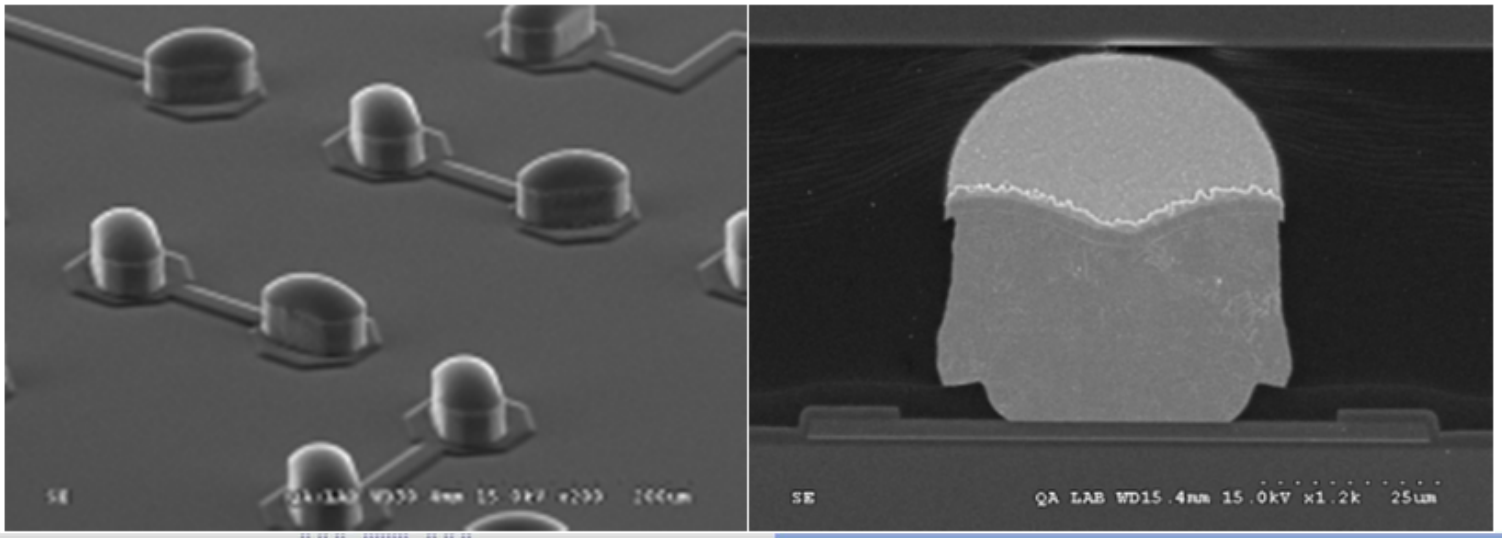


Fine Pitch Cu Pillar FlipChip

- CuBOL (Cu Pillar Bond On Line)
  - Solder Cap of Cu Pillar encroaches the Cu Trace on Substrate
  - Trace Volume adds to the Solder Cap Volume
  - Solder Cap Volume expands
- Along the Trace
- Perpendicular to the Trace

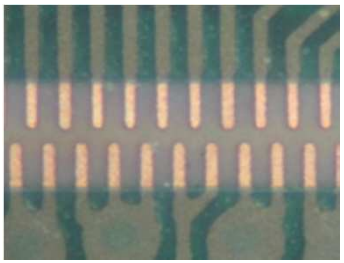
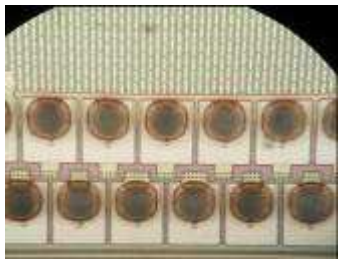
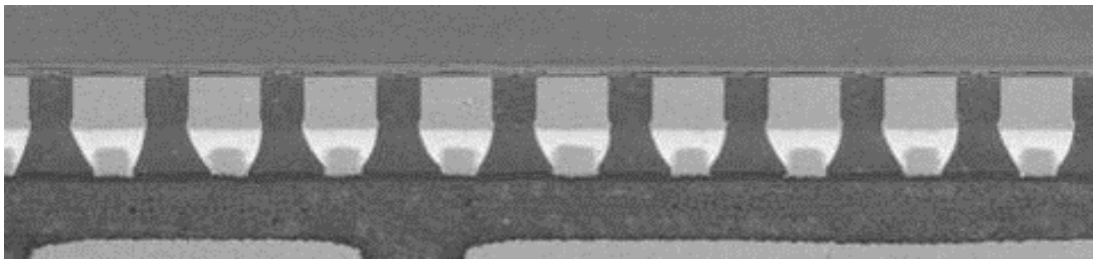




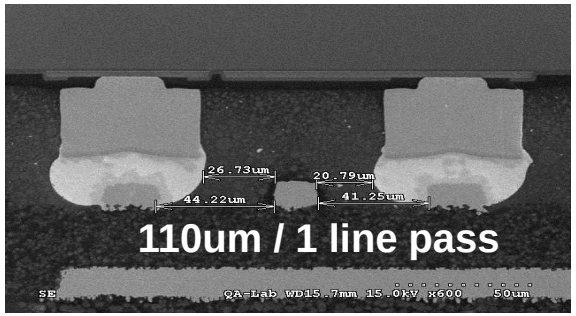


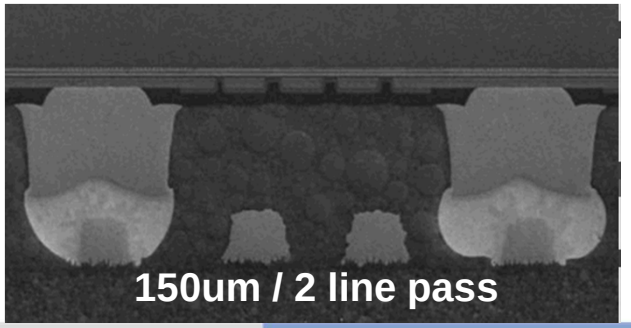
Fine Pitch Cu Pillar FlipChip

- FC MR MUF (FlipChip, Mass Reflow, Mold Under Fill)
  - 2 Rows Peripheral Cu Pillar Bumps 60um Pitch each row

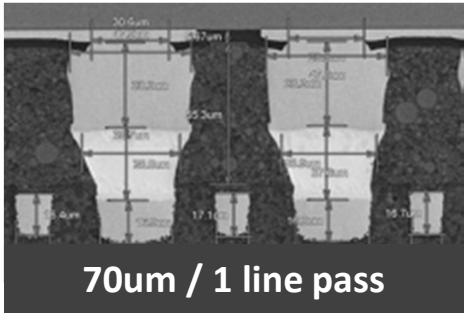
  - 3 and more Rows Cu Pillar Bumps have the need of traces routing between bond pads. These traces can not be covered by Solder Mask



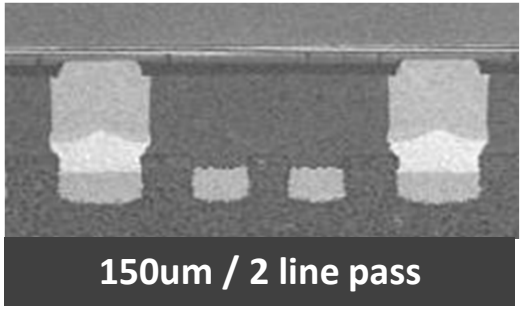


Fine Pitch Cu Pillar FlipChip

- CuBOL on EPP Substrate
  - Solder Cap of Cu Pillar wets the Cu Trace Top on EPP Substrate
  - Trace Volume does not add to the Solder Cap Volume

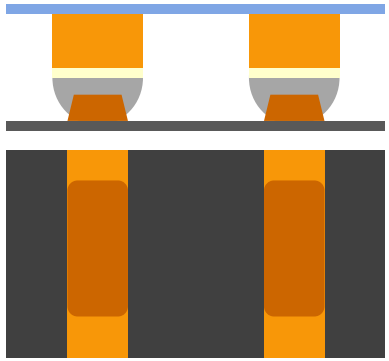


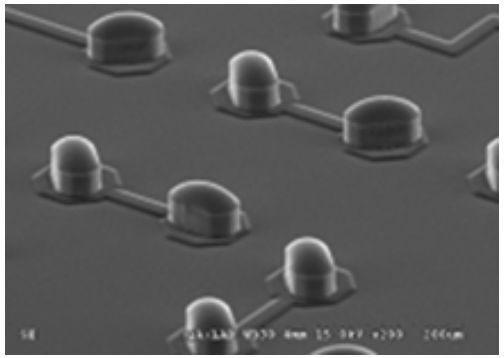
70um / 1 line pass

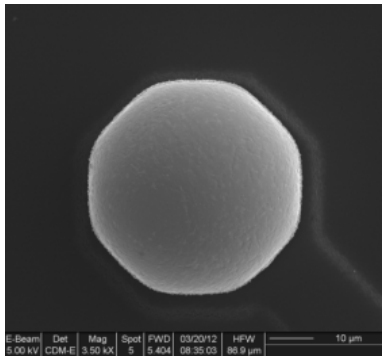


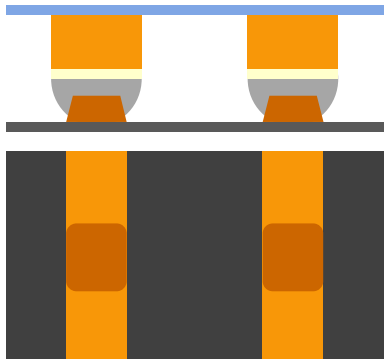
150um / 2 line pass

- Oval or Bar shape Cu Pillar enlarges the Solder Bond Area









Fine Pitch Cu Pillar FlipChip

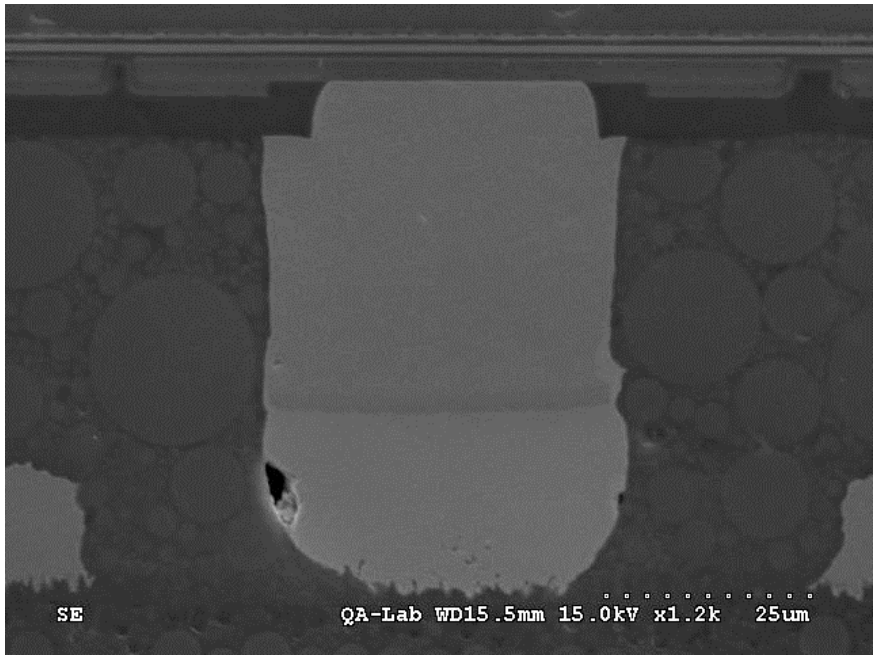
- Reliability comparison CuBOL vs. CuBOL EPP Substrate
  - Device 11.8x11.8 mm², 515 Balls, Die 6.6x5 mm²,
    899 oval Cu pillar 45x95, pitch 150 um with 2 lines pass

Device Version	MSL3/2aa	TCB 1000 cyc	HAST 96 hrs	TCT 3500 cyc	HTST 3000 hrs
CuBOL	Pass	Pass	Pass	Pass	Pass
CuBOL EPP	Pass	Pass	Pass	Pass	Pass

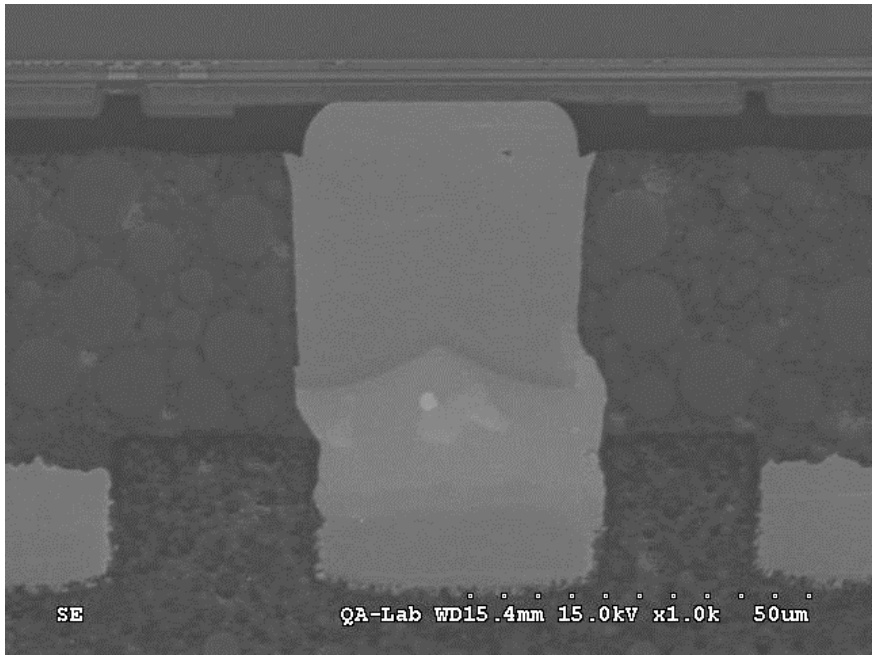
Fine Pitch Cu Pillar FlipChip

- Reliability comparison CuBOL vs. CuBOL EPP
  - Comparison after TCT 3500 Cycles

CuBOL –
Cu Trace no longer oberservable

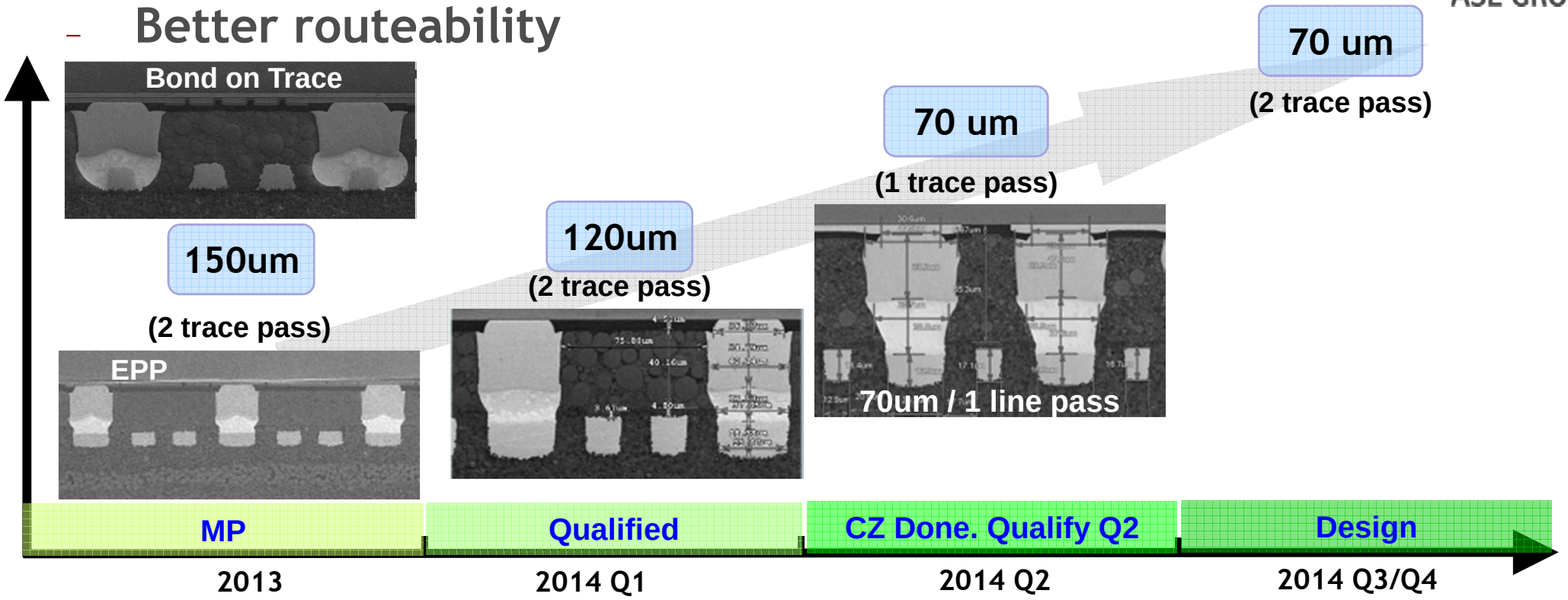


CuBOL EPP –
Half of the Cu Trace diluted



Cu Pillar Fine Pitch Roadmap

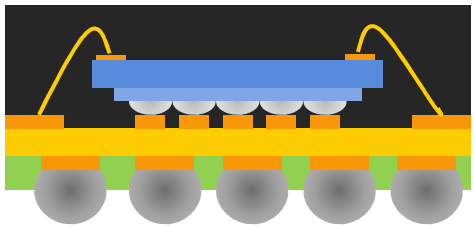
- Advantage of EPP on fine pitch
  - Better routeability

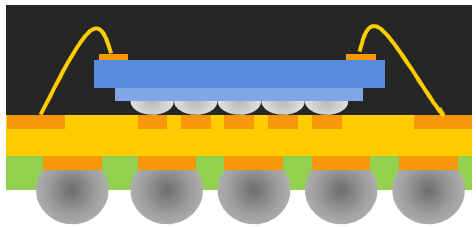


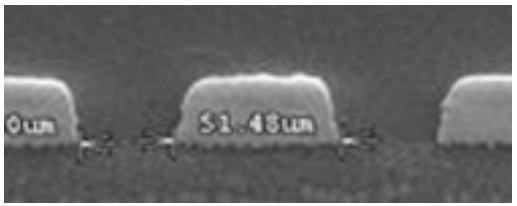
Wafer	28 nm			20 nm	
Process	MR Cu Pillar (BOT / EPP)		MR Cu Pillar (EPP)		
SBS	L/S=20/20	L/S=15/15	L/S=12/12	L/S=10/10	L/S=8/8
C4 Pad	BOT 40	EPP 35		EPP 30	EPP 25
UBM to Trace Space	17.5	15		10	7.5

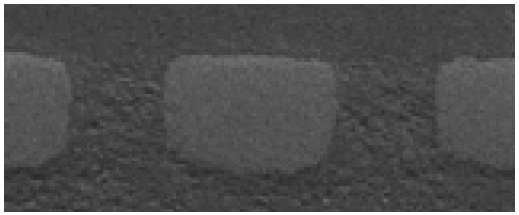
Bond Finger Pitch

- Hybrid Packages with Wire Bond Die on Top
  - Bond Finger Pitch
  - Bond Finger Top Width

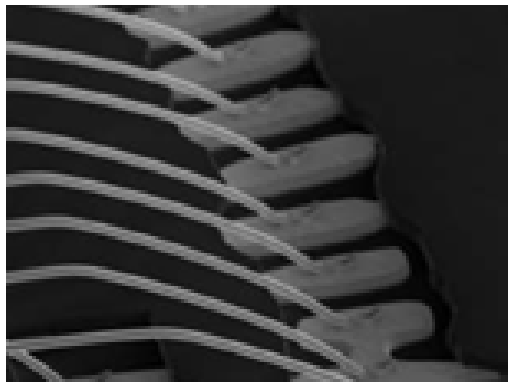


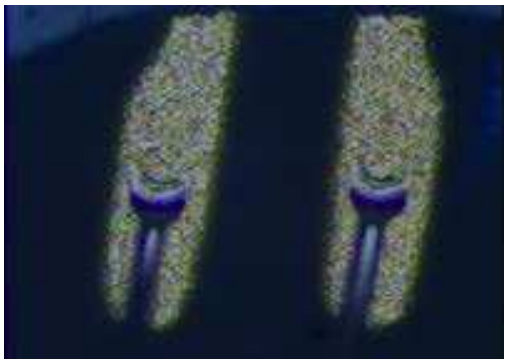






Process	Head	Foot	Pitch
Sub	40	55	85
MSAP	40	50	80
EPP	40	40	60





Conclusion

- EPP Substrates as a result of coreless substrates can be manufactured in any layer count with flexible via connections from layer to layer – high routability
- Embedded Traces result in finer pitches for Cu pillar FC assembly as well as for wire bond and hybrid assembly
- Slower IMC formation due to only one contact surface to the Copper Pillar solder cap; expect similar reliability test results
- EPP Substrates can be a good solution when ultra fine pitch Cu Pillar Flip Chip is requested.

Thank You

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