Fine Pitch Substrate for Cost Effective Flip Chip Package using Embedded Trace Substrate Technology

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ASE Europe
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EPP Substrates

- ASE Substrate Manufacturing
- Substrate manufacturing
  - Subtractive
  - MSAP/ SAP
  - EPP
- Cu pillar FlipChip fine pitch
  - Peripheral, Array, Pitches on Substrate
  - Reliability Results
- Wire Bond Finger Pitch (Hybrids)
- Conclusion
Substrate Manufacturing Sites

ASEMTL Shanghai outlook
- Operation began from 2003
- Capital: $140M USD
- Capacity: 48kk pcs /Month based on PKG(27x27mm)
- Manpower: 1,750
  - Manufacture: 1300
  - PE, RD & QA: 280
Substrate Manufacturing Sites

ASEMTL Kaohsiung outlook
- Operation began from 1995
- Capital: $135M USD
- Capacity: 22kk pcs /Month based on PKG(27x27mm)
  (future expansion to 36kk pcs/Month)
- Manpower: 1,000
  - Manufacture: 650
  - PE, RD & QA: 250

ASEMTL Shanghai, China

PBGA  Module  BOC  TFBGA  FCCSP  HG
Substrate manufacturing

- **Subtractive**
  - Via drill, E’less Cu, Panel Plating, Tent’n’Etch
Substrate manufacturing

- MSAP (Modified Semi Additive Process), SAP
  - Via drill, E’less Cu, Pattern Plating, Flash Etch
Substrate manufacturing

- **EPP (Embedded Pattern Process) I**
  - Pattern plating, Lamination, Via Drill, E’less Cu

1. Material release
2. Press lamination (1)
3. PR image transfer
4. L1 pattern plating
5. PR stripping
6. Press lamination (2)
7. Laser drilling
8. E’less Cu plating
9. PR image transfer
Substrate manufacturing

- EPP (Embedded Pattern Process) II
  - Pattern plating, Flash Etch, De-carrier, Backside Etch
Substrate manufacturing

- Subtractive vs. MSAP vs. SAP vs. EPP

<table>
<thead>
<tr>
<th>Process</th>
<th>Subtractive</th>
<th>MSAP</th>
<th>SAP</th>
<th>EPP</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/S, Pitch</td>
<td>50/50, 100</td>
<td>25/25, 50</td>
<td>20/20, 40</td>
<td>15/15, 30</td>
</tr>
<tr>
<td>Top</td>
<td>Flat</td>
<td>Round</td>
<td>Round</td>
<td>Flat</td>
</tr>
<tr>
<td>Head Foot Ratio</td>
<td>(1-(2/3CuT)):1</td>
<td>1:1</td>
<td>1:1</td>
<td>1:1</td>
</tr>
</tbody>
</table>

- Copper Plating
- Protected by dry film
- Flat Shape

- 1<sup>st</sup> + 2<sup>nd</sup> Copper Plating
- Etching without dry film protected
- Arcuate Shape

- Laminate protected etch
- Rectangular Shape
Fine Pitch Bumping

- N40nm / N28nm / N20nm wafer node and beyond
  - Small Die Size
  - High I/O Count
  - Small Pitches
- FC Bumping Pads
- Wire Bond Pads
Fine Pitch Cu Pillar FlipChip

- **CuBOL (Cu Pillar Bond On Line)**
  - Solder Cap of Cu Pillar encroaches the Cu Trace on Substrate
  - Trace Volume adds to the Solder Cap Volume
  - Solder Cap Volume expands

- Along the Trace
- Perpendicular to the Trace
Fine Pitch Cu Pillar FlipChip

- **FC MR MUF (FlipChip, Mass Reflow, Mold Under Fill)**
  - 2 Rows Peripheral Cu Pillar Bumps 60um Pitch each row
  - 3 and more Rows Cu Pillar Bumps have the need of traces routing between bond pads. These traces can not be covered by Solder Mask
Fine Pitch Cu Pillar FlipChip

- **CuBOL on EPP Substrate**
  - Solder Cap of Cu Pillar wets the Cu Trace Top on EPP Substrate
  - Trace Volume does not add to the Solder Cap Volume

- **Oval or Bar shape Cu Pillar enlarges the Solder Bond Area**
Fine Pitch Cu Pillar FlipChip

- Reliability comparison CuBOL vs. CuBOL EPP Substrate
  - Device 11.8x11.8 mm², 515 Balls, Die 6.6x5 mm², 899 oval Cu pillar 45x95, pitch 150 um with 2 lines pass

<table>
<thead>
<tr>
<th>Device Version</th>
<th>MSL3/2aa</th>
<th>TCB 1000 cyc</th>
<th>HAST 96 hrs</th>
<th>TCT 3500 cyc</th>
<th>HTST 3000 hrs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CuBOL</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>CuBOL EPP</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
</tbody>
</table>
Fine Pitch Cu Pillar FlipChip

- Reliability comparison CuBOL vs. CuBOL EPP
  - Comparison after TCT 3500 Cycles

CuBOL – Cu Trace no longer observable

CuBOL EPP – Half of the Cu Trace diluted
Cu Pillar Fine Pitch Roadmap

- **Advantage of EPP on fine pitch**
  - Better routeability

<table>
<thead>
<tr>
<th>Wafer</th>
<th>2013</th>
<th>2014 Q1</th>
<th>2014 Q2</th>
<th>2014 Q3/Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 nm</td>
<td>MR Cu Pillar (BOT / EPP)</td>
<td>MR Cu Pillar (EPP)</td>
<td>MR Cu Pillar (EPP)</td>
<td>MR Cu Pillar (EPP)</td>
</tr>
<tr>
<td>L/S=20/20</td>
<td>L/S=15/15</td>
<td>L/S=12/12</td>
<td>L/S=10/10</td>
<td>L/S=8/8</td>
</tr>
<tr>
<td>BOT 40</td>
<td>EPP 35</td>
<td>EPP 30</td>
<td>EPP 25</td>
<td></td>
</tr>
<tr>
<td>UBM to Trace Space</td>
<td>17.5</td>
<td>15</td>
<td>10</td>
<td>7.5</td>
</tr>
</tbody>
</table>

- **Bond on Trace**
  - 2 trace pass

- **EPP**
  - 2 trace pass

- **Process**
  - 2014 Q2

- **2014 Q1**
  - (1 trace pass)

- **2014 Q3/Q4**
  - (2 trace pass)

- **Design**
  - 70 um

- **70 um**
  - 70 um / 1 line pass

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Bond Finger Pitch

- Hybrid Packages with Wire Bond Die on Top
  - Bond Finger Pitch
  - Bond Finger Top Width

<table>
<thead>
<tr>
<th>Process</th>
<th>Head</th>
<th>Foot</th>
<th>Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub</td>
<td>40</td>
<td>55</td>
<td>85</td>
</tr>
<tr>
<td>MSAP</td>
<td>40</td>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td>EPP</td>
<td>40</td>
<td>40</td>
<td>60</td>
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</tbody>
</table>
Conclusion

- EPP Substrates as a result of coreless substrates can be manufactured in any layer count with flexible via connections from layer to layer – high routability
- Embedded Traces result in finer pitches for Cu pillar FC assembly as well as for wire bond and hybrid assembly
- Slower IMC formation due to only one contact surface to the Copper Pillar solder cap; expect similar reliability test results
- EPP Substrates can be a good solution when ultra fine pitch Cu Pillar Flip Chip is requested.
Thank You

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