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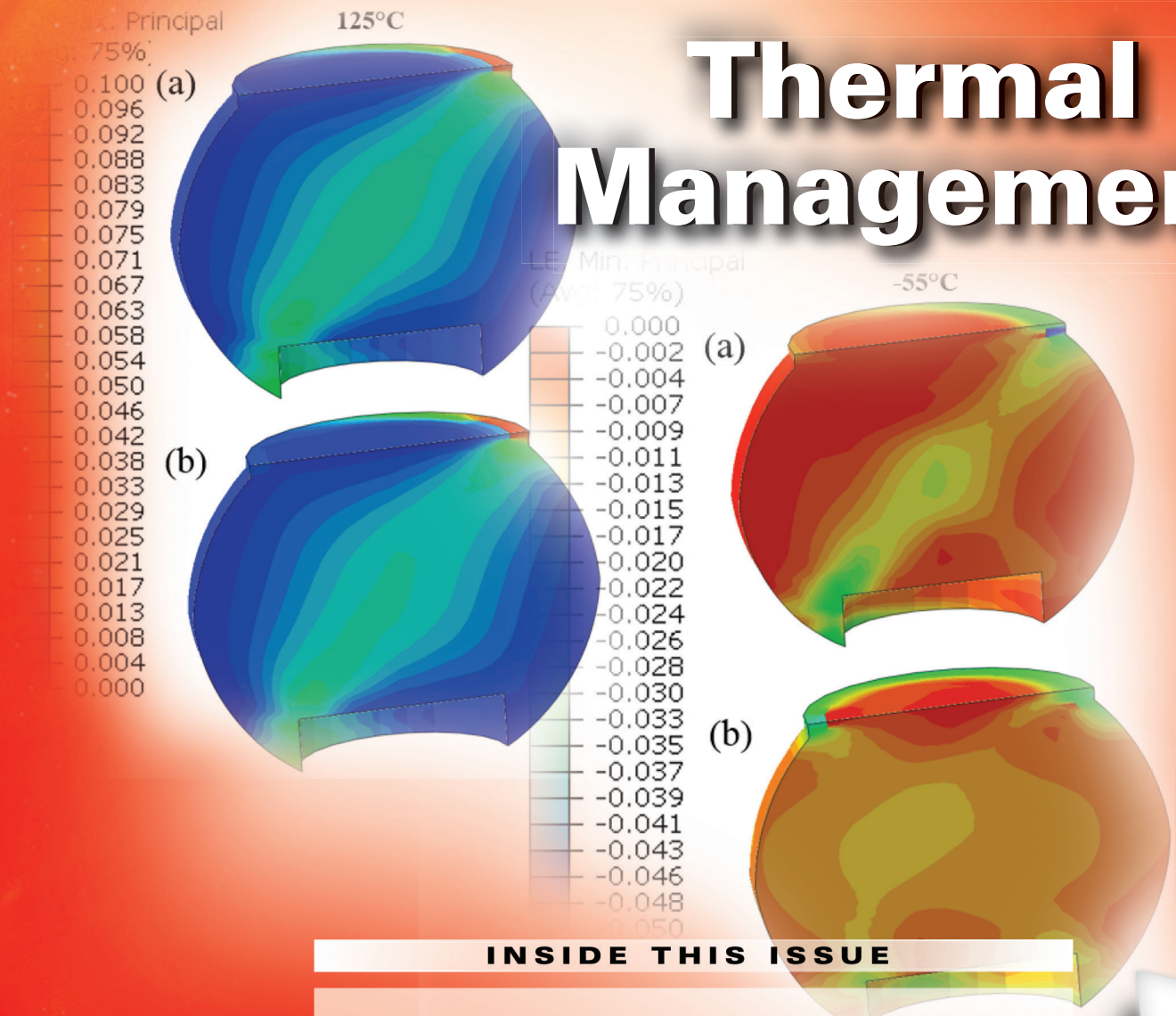
SEPTEMBER/OCTOBER 2017
Vol. 44 No. 5



Thermal Management

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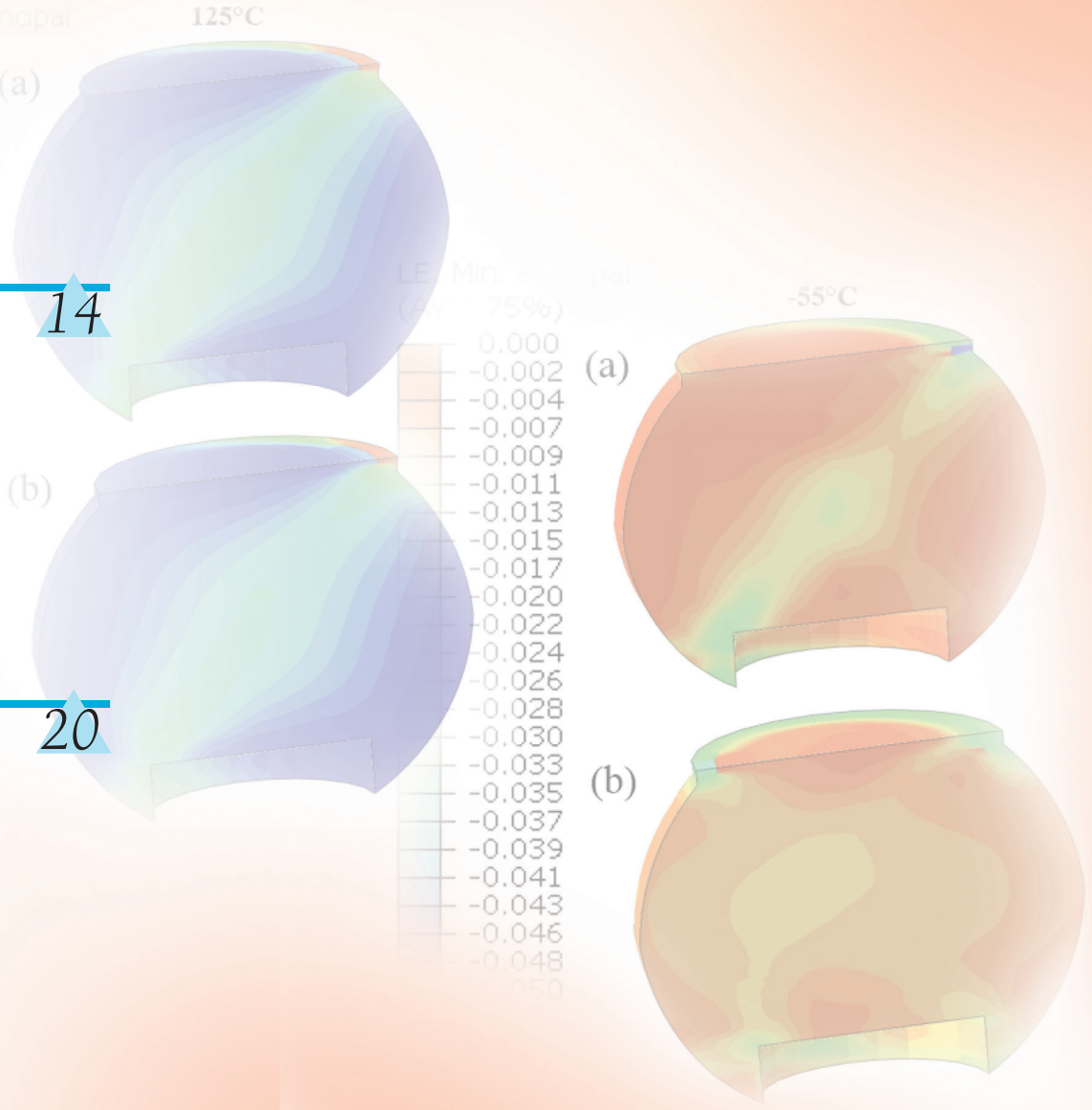

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Sn63Pb37 Maximum principal strain at 125°C for the corner BGA: (a) with conformal coating; (b) without conformal coating.

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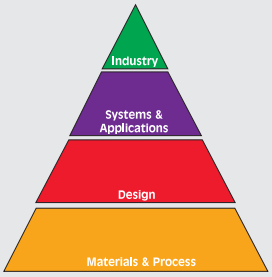

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Device Packaging 2018
March 5-8, 2018 We-Ko-Pa Resort and Casino, Fountain Hills, Arizona

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Advancing Microelectronics (formerly Inside ISHM) is published six times a year and is a benefit of IMAPS membership. The annual subscription price is $95; $15 for a single copy.

FROM THE GUEST EDITOR

David Saums
Principal
DS&A LLC

Thermal Management: Tracking Technology Developments

We have an update every year on developments in electronics thermal management, held in Silicon Valley since 2000: the IMAPS Advanced Technology Workshop (ATW) on Thermal Management. As with all of the IMAPS-sponsored conferences and workshops, this event is made possible by a team of volunteers on the organizing committee. This particular Workshop has been held longer than those on any other topic. Examining the value to the industry engineer of such events is an important exercise, especially given the constraints for every company and research institution, large and small, on human resources, time, and budgets.

Why, with the ability to search widely and deeply into many topics on line, as well as with conference calling and the ability to collaborate through online documents, do we need to gather in these face-to-face meetings? Observations about the IMAPS ATW on Thermal Management, with its long history, can provide good insight on the benefits of these events to the IMAPS community.

Engineering societies (including ASME, IEEE, and others) hold conferences, workshops, and symposia on an astounding variety of industry topics. The Thermal Management ATW continues to be seen as an ideal venue for presenting, discussing, and learning about very recent developments. Topics include advanced thermal and packaging materials, thermal components (a recent example being flexible organic vapor chambers), systems, and market developments that are creating new needs for change and development.

A critical component of the ATW Thermal, to a greater degree than in virtually any other thermal management workshop or conference, is the degree of person-to-person networking and discussion that occurs during the course of three full days of technical presentations. Dinners are held on two evenings, with an evening technical session on those nights. This is done specifically to encourage further discussions at dinner and after the evening program concludes. Not only do these establish business relationships, but friendships developed at this Workshop have continued for decades; your editor can speak to those friendships personally, from all parts of the globe.

The organizing committee for the ATW Thermal is made up of volunteers from semiconductor, system, and component manufacturers, and academia. Technical program chairs since 2000 have been Herman Chu (now at nVidia), Cullen Bash (HP Labs), David Copeland (retired from Oracle), and Vadim Gektin (Huawei), our current technical program chair. Key to how this Workshop is organized is solicitation of presentation topics from speakers in selected areas of the industry; this is done in order to assemble a cohesive technical program. For example, each year has typically included sessions on organic thermal interface materials; non-organic TIMs; CTE-matched materials; liquid cooling; mobile device design; and market drivers.

The first IMAPS ATW Thermal was held in Breckenridge, Colorado in 1992; the focus for that Workshop included multi-chip modules, gate arrays, early ASICs, and microprocessors, as well as thermal materials. A focus in the 1995 Workshop on the potential application of heat pipes for mobile processors used in notebook PCs was led by Hong Xie of Intel. It paralleled development at Wakefield Engineering for the first concept and use of what has since been termed the Remote Heat Exchanger (RHE) for mobile processors. Wakefield applied for and was granted a US patent. Interestingly, that same basic assembly design has now shipped in notebook PCs for more than twenty years.

DARPA's recent Thermal Ground Plane program is another example of new developments, including very thin titanium vapor chambers and the flexible vapor chamber manufactured with PCB methods, have been presented for the first time globally.

The Workshop relocated in 2000 from the mountains of Colorado to Palo Alto, California. HP Labs provided strong support each year and a student abstract competition was proposed by Chandrakant Patel, now Chief Engineer of HP Labs, to promote interest from undergraduate and graduate engineering and science students. The initial funding for this program was provided by HP Labs, with several other companies and the Microelectronics Foundation joining in, for this very successful new addition to the annual program. This tradition continues today and winning student presenters have returned to present again, now employed in positions in industry and research institutions.

A market drivers session, added in 2002, has identified specific developing needs for improvements and new types of devices exacerbating thermal design issues. Tabletop exhibits were added to the Workshop in 2004; a particular goal was established to have exhibitors who also were presenters, to further connect and enable opportunity for discussion of new developments.

Keynote speakers have addressed topics including heat spreading challenges in handheld and mobile devices, medical devices, limits on thermal design for smartphones, developments in thermal management and testing for military airborne communications systems, photonic and other developments in enterprise servers, microprocessor thermal challenges for smartphones, and single- and two-phase liquid cooling in enterprise servers. Keynotes have been given by senior engineers, managers, and professors from Samsung (Korea), IBM, Intel, HP Labs, Qualcomm, Rockwell Collins, AMD, University of Colorado, University of Texas, and Microsoft.

The ATW Thermal technical program is structured with a single session track, to ensure that all attendees are able to attend and participate in each presentation.

IMAPS France initiated a parallel event in 2006, held in La Rochelle, France. The La Rochelle workshop is modeled after the IMAPS ATW Thermal and focuses not only on thermal management topics, but also packaging and packaging materials developments that are very closely aligned with thermal issues. This very successful workshop has grown to become a pan-European event with speakers and attendees from across the EU, with some also from North America and Asia. The thirteenth event will be held in La Rochelle, beginning on January 30, 2018.

The opportunity to meet annually and review the latest in technology and market developments surrounding thermal management issues for electronics systems is not limited to the IMAPS ATW Thermal, alone. Another IMAPS event with a significant thermal management content is the jointly-organized HiTEN and HiTEC conference pair. HiTEN is organized as a high temperature electronics conference held in the UK during odd-numbered years, with HiTEC held as a companion conference on the same subjects in Albuquerque, New Mexico, in even-numbered years. The high temperature environment is an increasingly challenging market for electronic materials and components of many kinds.

SEMI-THERM Symposium will be held for the thirty-fourth year in San Jose, California, in March 2018. This is the largest conference in North America focused solely on electronics temperature measurement and thermal management. Therminic is organized in the European Union each year, generally in September, and moves to different cities each year. ASME InterPack and IEEE I-Therm are both conferences held in North America annually with very significant thermal content.

Note also that the IMAPS Symposium, held in North America on an annual basis, also has had excellent thermal sessions and that tradition continues for 2017, with the Symposium again to be held in Raleigh, North Carolina.

Participation in these events as an attendee, speaker, exhibitor, or as a volunteer to assist with organizing a given workshop or conference, continues to be a significant contributor to our industry and our knowledge base for new developments in electronics packaging and thermal management. Get involved!

David Saums has thirty-nine years of business development and technical marketing experience with advanced packaging and thermal materials, components, and two-phase liquid cooling systems. He has chaired or given technical conference presentations in eight countries on thermal management topics. Dave is general chair for the IMAPS ATW on Thermal Management (eighteen years), has participated with the IMAPS France thermal and packaging workshop organizing committee (fourteen years), and served as general chair for Semitherm in 2006. Dave founded and has operated a full-time consulting business for fourteen years to assist in applying new materials and technologies for applications as diverse as handheld devices and HEV powertrain inverters. He has made hundreds of visits to OEM engineering groups globally.

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Assessing the Effect of Improper Conformal Coating on SnPb and Pb-free BGA Solder Joints during Thermal Cycling: Experiments and Modeling

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Abstract

Electronic components, such as ball grid array (BGA), chip scale packages (CSP) and bottom terminated components (BTC), used in harsh use environments often require the use of conformal coatings to meet reliability requirements. In certain coating application methods, the conformal coating materials can flow underneath the component and cause solder joint failure during thermal expansion and contraction of the electronic assembly. In this study, BGA components were coated with an acrylic conformal coating material using two application methods and subjected to two different thermal cycling profiles to assess the integrity of SnPb and Pb-free BGA components. To better understand the observed failure modes, Finite Element Analysis (FEA) was performed on the conformally coated BGA packages. Material characterization was performed using Dynamic Mechanical Analysis (DMA) and Thermal Mechanical Analysis (TMA) to capture the temperature dependent properties of the conformal coating to better correlate simulation and experimental results. Failure modes were found to greatly depend on the conformal coating material properties around the glass transition temperature (T_g) rather than temperature cycle range. Significant differences in the failure mode were found between the Pb-free and SnPb BGA components with acrylic conformal coating materials and temperatures profiles.

Keywords
conformal coating, thermal cycling, Ball Grid Arrays, solder fatigue, Finite Element Modeling, SAC305, Sn63Pb37

1. Introduction

Conformal coatings are used on Printed Circuit Boards (PCB) with the intent of providing protection from harsh environments containing moisture and contamination, such as dust and metallic debris that could cause shorts in electronic components. In addition, some conformal coatings are designed to provide thermal insulation, shock vibration attenuation and electrical insulation for high voltage components at high altitudes [1]. Conformal coatings are also being used to help mitigate the risk of tin whiskers on pure tin surface finishes [2]. These attributes make conformal coatings especially attractive for the high reliability application environments of avionic and aerospace electronics. Previous studies have shown that the application of conformal coating to surface mount resistors and CSPs can reduce the thermal strain in solder joints and thus extend the thermo-mechanical fatigue life of components [3-5].

Potential concerns regarding solder joint integrity arise when the conformal coating material is allowed to flow underneath the package. Recent investigations have shown that the presence of conformal coating under a plastic quad-flat no lead package (PQFN) dramatically reduces the thermo-mechanical fatigue (TMF) life of the device by changing the equivalent plastic strain of solder joints from predominantly shear to an axial loading mode [6]. In such a condition, the conformal coating expands and contracts in the vertical direction. As thermal cycling progresses, failure in solder joints could result from the lifting of the component that causes excessive tensile and compressive stresses. The amount of axial stress will greatly depend on the leverage of the conformal coating on the particular component and the variation of coefficient of thermal expansion (CTE) and elastic modulus (E) of the coating with temperature. In addition, conformal coating materials with a T_g that is within the thermal cycle range could drastically reduce fatigue life of solder interconnects. As the temperature approaches the material's T_g, large expansion occurs along with a reduction of the material stiffness. In cases when the conformal coating material expansion occurs prior to adequate softening, large stresses would be applied to solder joints. This behavior

is inherent in thermoset polymers since materials expansion tends to be driven by the changes in the free volume while changes in the modulus tends to be driven by the increased movement of the polymer chains. Due to the intrinsic properties and large variety of conformal coating used by the electronics industry, their effects on solder joint life should be better understood.

This research aims to investigate the impact that conformal coatings, and their application method, can have on Pb-free and SnPb area array components subjected to thermal cycling. The experimental procedure follows that of a previous study that only included components with SnPb solder [7]. Results from mechanical characterization of the acrylic conformal coating were used in finite element simulations to assess the effects of conformal coating, application method, solder alloy and thermal cycle range on BGA component reliability and failure mode.

2. Experimental Approach

Simulations in the current study were based on the experimental thermal cycle testing on BGA components with Sn63Pb37 (63Sn37Pb) solder balls [7] and SAC305 lead-free solder balls [8]. Assembled test vehicle included 60 components, with unrealistically thick conformal coating on the right half. Standard conformal coating was then applied to the left side of the board. An Anatech event detector system continuously monitored the continuity of the daisy-chain BGA components to determine the thermal cycle at which solder joint failure occurred.

2.1 Material Properties

Acrylic conformal coating is widely used in a large variety of electronic assemblies. To understand the temperature- dependent mechanical behavior of the material, bulk samples of the acrylic conformal coating were prepared and characterized using TMA and DMA to measure the material's CTE and modulus as a function of temperature as shown in **Figure 1**. These measured temperature-dependent properties were implemented in FE modeling. The acrylic coating did not exhibit an abrupt property transition in a small temperature range, so the material T_g was defined as ~15°, which is the midpoint of the region in which the modulus decreased and CTE rapidly increased.

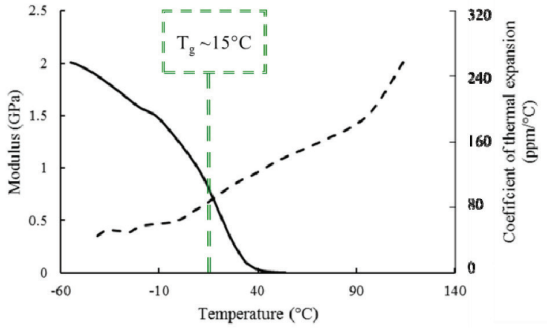

Figure 1. DMA and TMA results of acrylic coating.

2.2 Test Vehicle

The test vehicles included daisy-chained, 1mm pitch, 256 IO BGA components with a package size of 17mm x 17mm. Each test board was populated with 60 individual components as shown in **Figure 2**. The FR4 test boards were 2.05mm (81 mil) thick and included 8 dummy inner layers to simulate circuitry. BGA components assembled using a 0.127mm (5 mil) thick stencil. Two conformal coating configurations were applied to the two halves of each test vehicle. The left half of each board was coated using "Standard" production spray process while the right half of the boards was coated with a manual process using pneumatic syringe to completely fill the conformal coating material under each BGA. This configuration, which is referred to as "Thick" application in this paper, represents a worst-case scenario of conformal coating application that can occur in dipping method and heavy spray coating applications. Additional "Control" boards with no conformal coating were also included in the test to compare to the reliability of components that were not coated. X-ray imaging was performed on the thick coated parts to ensure the conformal coating is filled completely underneath each component with no voids. The same approach was used on the stands spray coated components to ensure conformal coat did not wick underneath the parts.

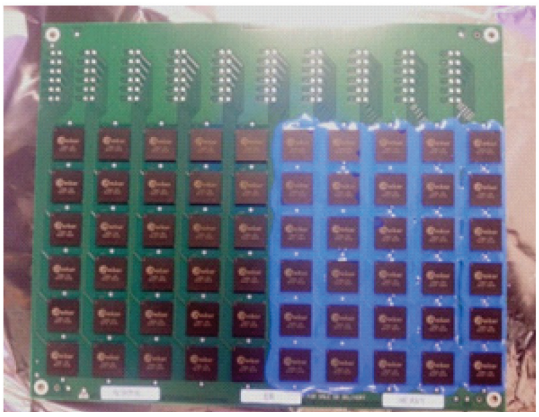

Figure 2. Assembled test vehicle showing two halves of the board with one side applied with Thick conformal coating [7].

3. Thermal Cycle Testing

Each test vehicle was subjected to one of two different thermal cycling ranges. Temperature Profile 1 had a temperature range of -55°C to +125°C for 620 cycles while Temperature Profile 2 used a temperature range of -20°C to +80°C for 2020 cycles. The two profiles, which are shown in **Figure 3**, used a minimum 15 minute dwell time at each temperature extreme and a ramp rate of 5-10°C/minute, per IPC- 9701 [9].

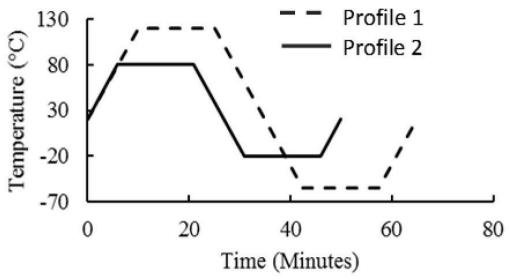

Figure 3. Thermal cycles used in experiment and modeling.

4. Test Results

Reliability data of BGA components were analyzed using regression analysis to determine the Weibull shape factor (β) and characteristic life (η) for each configuration.

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The Weibull function correlates the cumulative failure distribution F(t) to the number of thermal cycles at which failure occurs shown in equation (1).

$$F(t) = 1 - \exp\left(-\frac{t}{\eta}\right)^{\beta} \qquad (1)$$

The reported characteristic life corresponds to number of cycles at which 63.2% of the population is expected to have failed.

4.1 Failure Data Analysis

Table 1 summarizes the failure data for the two solder alloys (SAC305 and Sn63Pb37), two thermal cycle ranges (Temperature Profiles 1 and 2) and the three coating conditions (Control, i.e. no coating, Standard application and Thick application). The table shows the calculated Weibull coefficients and the first measured failure for that population. It can be noted that no distinct difference in characteristic life between the control and Standard coated components can be observed. This indicates that there could be no interaction between the Standard acrylic coating and the BGA package during thermal cycling. In some configurations, the control outlasted the Standard coating and in others the opposite was true. This behavior limits any inference of possible contribution of the Standard coating process to the fatigue life of BGAs.

Table 1. Weibull Coefficients for Experimental Data

Alloy	Application method	Temp Profile	β	η	First failure
SAC305	Control	1	7.9	256	173
	Standard	1	5.7	448	245
	Thick	1	16.7	197	171
	Control	2	8.4	2600	1532
	Standard	2	4.2	2054	935
	Thick	2	3.8	191	88
Sn63Pb37	Control	1	16.9	631	514
	Standard	1	14.6	567	472
	Thick	1	6.1	573	364
	Control	2	N/A	N/A	N/A
	Standard	2	13.5	1453	1060
	Thick	2	4.8	1554	756

Figure 4 shows the cumulative failure distribution for BGAs with SAC305 solder joints and compares the reliability of Standard and Thick coatings for both temperature profiles. For the Control samples and those with Standard coating application, the thermal cycling profile significantly affected the reliability, with the samples subjected to the less severe temperature excursions exhibiting much longer fatigue life. However, the poor reliability of the samples with Thick coating was essentially just as low with Temperature Profile 1 as with Temperature Profile 2.

Figure 5 combines the cumulative failure distribution data from reference [7] for Sn63Pb37 components with acrylic coating with test data for Temperature Profile 2 [8]. This compares the effects of the two coating applications and temperature profile. Under the more severe thermal cycle profile of -55 to +125°C, samples with the Thick coating experienced earlier failures than those with Standard coating, which failed somewhat earlier than the Control samples. In contrast, under the less severe Temperature Profile 1, the SAC305 Standard coated parts had a somewhat higher average life than the Sn63Pb37 parts. While the average life of the SAC305 components significantly differed depending on whether the coating was Standard or Thick, the Sn63Pb37 solder joints did not appear to be significantly affected by the application method.

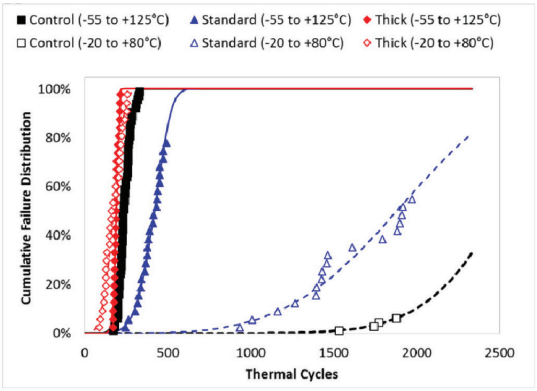

Figure 4. Cumulative failure distribution for the SAC305 samples with Standard and Thick acrylic coating. Solid lines/ symbols correspond to -55 to +125°C testing; dashed lines/open symbols correspond to -20 to +80°C testing.

Note that testing at the Temperature Profile 2 did not include any Control (uncoated) samples, due to limited availability of samples for testing and the very long test time that would have been needed to generate failures under the less severe temperature cycling conditions.

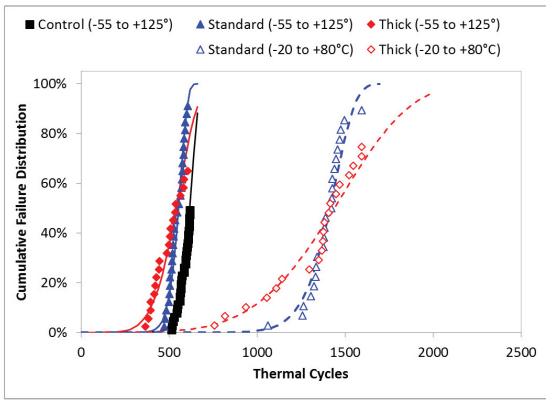

Figure 5. Cumulative failure distribution for the Sn63Pb37 samples with Standard and Thick acrylic coating.

4.2 Cross-sectional Failure Analysis

Post thermal cycling metallographic cross sectioning was performed on SAC305 and Sn63Pb37 BGAs to assess the solder joint damage and crack locations. **Figure 6** shows a solder ball from a SAC305 Control sample that exhibits cracking at the (lower) circuit board pad interface. Sn63Pb37 Control components more typically had cracks at the (upper) package interface.

Figure 7 shows cross sections of failed SAC305 components for both Standard and Thick coating applications. The appearance of the solder joint and locations of the crack for the Control and Standard conformal coating samples is quite similar, suggesting that they encountered the same failure mechanism. However, the Thick conformal coating introduced a new failure mechanism that significantly compressed the solder joint, which ultimately separated away from the circuit board a considerable

distance. It appears that the acrylic conformal coating, which occupied a much larger portion of the package than the solder joints, placed mechanical stresses on the solder joints, likely due to thermal expansion of the conformal coating itself.

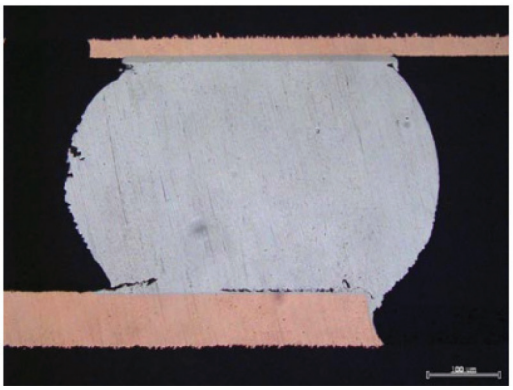

Figure 6. SAC305 corner BGA Control sample (no coating) showing cracking along bottom pad.

Figure 7b shows severe plastic deformation in the SAC305 solder joints and no evident distance to neutral effect. Similar cracking at the board pad was observed for the -20°C to 80°C thermal cycle, but with less plastic deformation as in Figure 7b. Large compressive strains caused the solder joint to be extruded outwards. This failure mode is also attributed to the lack of adhesion and interaction between the conformal coating and solder alloy during the low and high temperature extremes. At the high temperature dwell, solder joints creep and conformal coating softens and eliminates any possible adhesion between solder and the acrylic material. At the cold temperature extreme, the solder is compressed and squeezed outward in the normal direction to the applied load. The lack of hydrostatic stress on solder joints during low temperature dwell implies that no physical constraint is being placed on the solder and allows for the deformation to occur. This solder/conformal coating interaction is greatly dependent on the conformal coating CTE and modulus at the dwell temperature. It should be noted that the cross-sections shown in Figure 7 were made after the samples had accumulated more than 1000 thermal cycles. Since the SAC305 component exhibited a solder joint electrical open at ~100 thermal cycles, it is reasonable to assume that the majority of the severe deformation evident in Figure 7b occurred well after the initial solder joint failure.

Failure analysis showed that the Standard coated Sn-63Pb37 solder joints experienced similar failure mechanisms as the Control components, with cracks located on the upper solder/component pad interface. As shown in **Figure 8**, a Sn63Pb37 BGA with Standard acrylic coating that was subjected to 1600 thermal cycles under Temperature Profile 2, exhibited only slight cracking and grain coarsening.

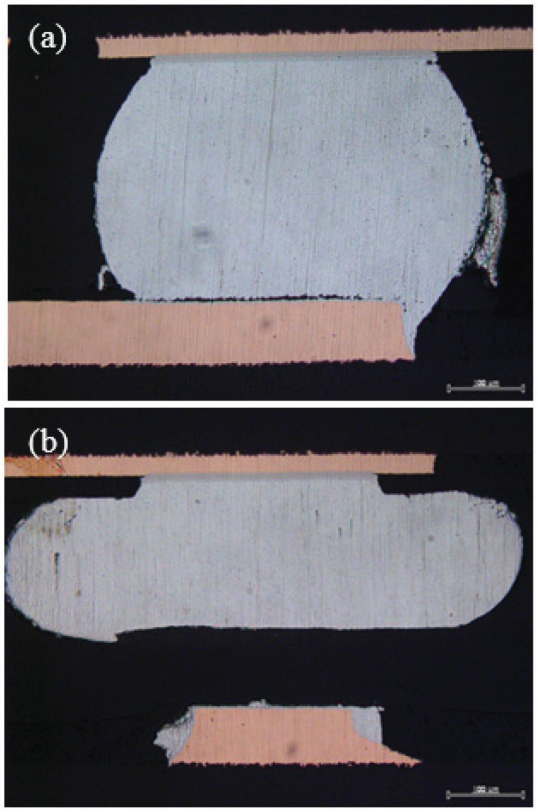

Figure 7. Failure of SAC305 corner BGA with acrylic conformal coating (-55 to 125°C): (a) Standard; (b) Thick coating.

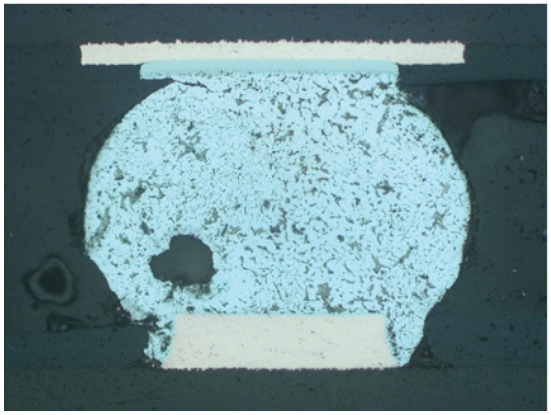

Figure 8. Sn63Pb37 corner BGA with acrylic Standard coating showing cracking in upper left size of solder joint at 1600 cycles.

Cross-sections of the Sn63Pb37 solder joints revealed that the magnitude of damage closely correlated to the characteristic life variation determined under both thermal cycles. A different failure mechanism with the thick acrylic coating between the Sn63Pb37 and the SAC305 solder joints was observed. **Figure 9** shows Sn63Pb37 solder joints with Thick acrylic coating after thermal cycling for a) corner joint and b) joints at the center of the row for the -20°C to 80°C thermal cycles. Cracking along the diagonal of the Sn63Pb37 solder occurs along with grain coarsening at the crack area as well as some extrusion similar to that seen in the SAC305 components. However, unlike the SAC305 components, electrical fail-

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ures in the Sn63Pb37 components were due to cracks along the diagonal of the solder joints that propagated prior to the severe compressive deformation that later took place. While failures in the SAC305 components were due to axial loads that were uniform across the component, the Sn63Pb37 components exhibited the more traditional effects of the distance to neutral point. The Sn63Pb37 components showed relatively little damage in the solder joints near the center of the row that progressively increased in joints closer to the edge of the part. This can be attributed to the lower stiffness of the Sn63Pb37 solder joints, which allows for more components warpage and load sharing between neighboring solder joints.

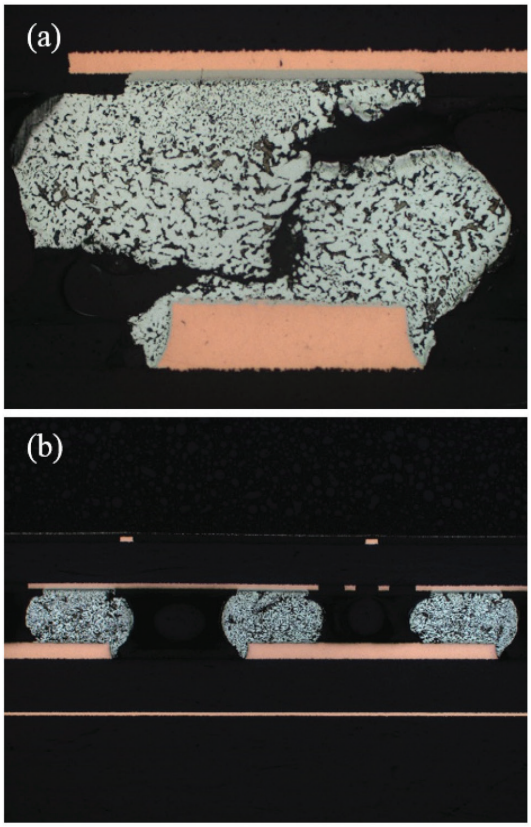

Figure 9. Sn63Pb37 BGA with thick conformal coating failed at 1055 thermal cycles (-20 to 80°C): (a) corner joint; (b) joints in the middle of a row.

The differences in the characteristic lives of the SAC305 and Sn63Pb37 components is also related to the local CTE mismatch between solder alloy and component. Differences in the microstructure and mechanical properties lead to lower axial strain, but with larger shear strains, for the corner Sn63Pb37 joints than those with SAC305. When combined with the axial compression induced by a Thick acrylic coating, those solder joints are placed under mixed-mode thermo-mechanical loading that causes cracks to progress along their diagonal.

A small number of the Sn63Pb37 components with Thick coating continued to show electrical continuity throughout thermal cycling. **Figure 10** shows examples of corner and middle row solder joints of one of these BGAs after experiencing 1600 thermal cycles of -20°C to 80°C. Clearly the solder joint was significantly affected by the thermal cycling and its lack of a failure could be simply a result of a signal resolution problem with the event detector. However, it is possible that vertical deformation of the solder joint induced by the acrylic coating compressed the joint together to a sufficient degree so as to overcome the effects of lateral or diagonal cracking. Essentially, the coating appears to have mechanically held the joint together sufficiently well enough that electrical continuity was maintained.

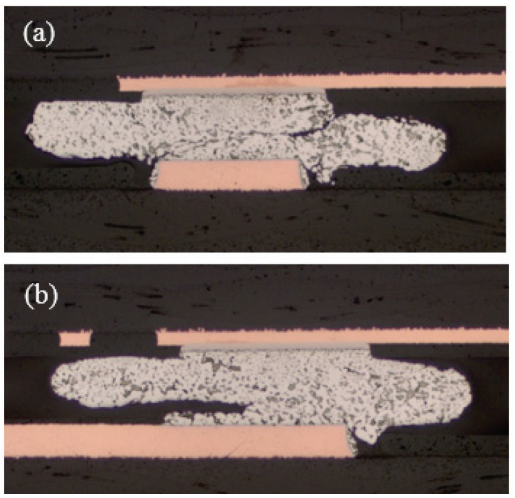

Figure 10. Sn63Pb37 corner BGA with thick acrylic coating survived 1600 cycles: (a) corner joint; (b) joint in middle row.

5. Finite Element Modeling

The BGA package was modeled using commercial finite element software: ABAQUS 16.4. A global/local modeling approach, which has proven to provide accurate results in modeling solder in electronic packaging [10]. The model consists of a quarter-symmetric, finite element model of the BGA package. Copper pads on both the PCB and substrate were modeled without solder mask. 'Plugs' of fine mesh were created to model the corner solder joints while plugs with a coarse mesh were used to model the rest of the solder joints **(Figure 11)**.

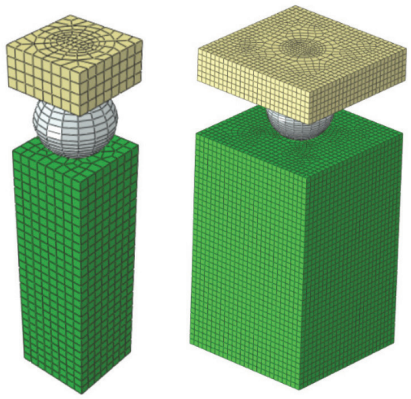

Figure 11. Local model 'plugs': (a) solder joint with coarse mesh; (b) solder joint with fine mesh.

To capture creep and plasticity deformation of solder joints, Schubert's constitutive model based on a hyperbolic sine function, which is shown as Equation (2) and implemented for both SAC305 and Sn63Pb37 solder. In this equation $\dot{\varepsilon}^{cr}$ is the steady state creep strain rate, k is Boltzmann's constant, T is the absolute temperature and σ is the applied stress. The constants A_1, α, n and H_1, which is the apparent activation energy, are material properties that depend on the material and define the power law relationship between creep strain rate and applied stress. Published values for SAC305 and Sn63Pb37 are listed in **Table 2** [11].

$$\dot{\varepsilon}^{cr} = A_1(sinh\alpha\sigma)^n \exp\left(-\frac{H_1}{kT}\right) \qquad (2)$$

Table 2. Schubert's Constitutive Model Coefficients

Solder	A1	α	n	H1
SAC305	277984	0.02447	6.41	54041
Sn63Pb37	23343480	0.06699	3.30	67515

The primary focus of this study was to better understand the mechanisms that led to the difference in failure modes between the Control samples and those with Thick acrylic coating. Simulation of the Standard coating process was not preformed due to the lack in distinction in characteristic life between the control and Standard coating process. Models of these two configurations with the two solder types investigated were created and analyzed. **Figure 12** shows the global view of the quarter symmetric BGA model with no coating.

Material properties used in the analysis are presented in **Table 3**. These values are a culmination of both published and measured quantities and are assumed to be linear elastic except for the solder alloys.

Local BGA plugs and a single quarter symmetric model were merged and constraints were generated between the plug surfaces and global model. **Figure 13** shows a single solder joint in the Thick coating model.

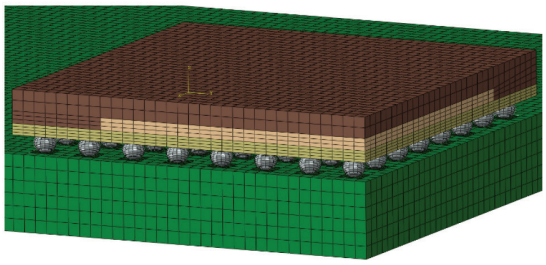

Figure 12. Global model without underfill.

Table 3. Material Properties used in Simulations

Material	Elastic Modulus (GPa)	Poisson's ratio	CTE (ppm/°c)
PCB	33.9	0.13	17
Substrate	28	0.13	13
Copper	118.5	0.326	16.7
Silicon	130	0.28	2.6
SAC305	*Properties defined by Equation (2)*		20
Sn63Pb37			24

This included a 20 µm gap between the solder and the conformal coating to avoid potentially over constraining the solder joint during thermal expansion. When solder joints are over constrained in thermal simulation large hydrostatic stresses can be generated in the model and provide overestimation of the mechanical loads solder joints experience. In real world conditions, solder alloys creeps at low temperatures and under mild loading conditions. As solder alloys undergo creep deformation any residual stresses or strains built up from underfilling material diminish due to the accompanying stress relaxation which occurs as solder alloy creep.

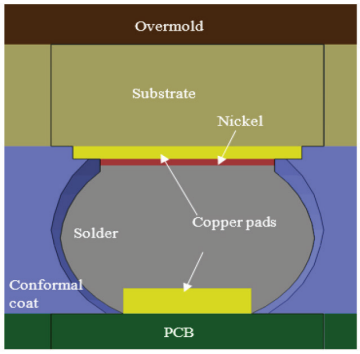

Figure 13. FE model structure with Thick conformal coating.

5.1 SAC305 BGA

Figure 14 shows the Von Mises stress contour plot for the corner and die shadow SAC305 solder joints at the beginning of a hot dwell period in Temperature Profile 1. The zero-stress state of the solder interconnects was taken at the initial temperature of 20°C. Residual stresses in solder joints due to shrinkage effects of the thick conformal coating during cure were not considered in this analysis. Stress relaxation behavior of the acrylic material is necessary in order to study the influence of process induced parameters on solder fatigue and are beyond the scope of this research.

For the corner solder joint in Figure 14, the maximum stress occurs at the solder/copper pad interface along with a slight distance-to-neutral-point effect, i.e., lateral stresses due to the board-to-package CTE mismatch. However, the stress in the solder joints in the die shadow show much more axial stress that indicate vertical loading. The location of maximum stress changes from the upper to lower interface during high and low dwell periods, respectively. **Figure 15** shows the volume-averaged stress in a 25 µm layer of elements directly above the board copper pad of a corner SAC305 solder joint during three full cycles of Temperature Profile 1, with and without Thick conformal coating. The largest average strain in the BGA solder joints occurred at the center and gradually decreased toward the solder/copper interface. Average stress values were largest at the interface and decreased toward the center of the joint. Since solder displacement is driven by thermal expansion of the conformal coating, solder joints are placed under displacement controlled loading conditions. With the thick conformal coating, larger axial strains accumulated during the cold temperature dwell. This value occurred at a point at which the acrylic material still maintained a high modulus. More damage accumulated at temperatures below the glass transition temperature than above it. As the glass transition region is approached from the minimum cycle

continued on page 12

continued from page 11

temperature, the elastic modulus of the acrylic is still large enough that even a small increase in the CTE generates significant stress.

Figure 16 compares the compressive loading caused by conformal coating contraction during the cold temperature dwell. This figure plots the axial strains over time for the SAC305 BGA with and without Thick conformal coating for the same layer of elements. It can be seen that, at the first high temperature dwell, both the Control and Thick coated joints, reach an equivalent state. However, the Thick coated joints reach a much larger compressive strain than the Control. This causes a shift from positive to negative axial mean strain, which correlates to the failure mode observed in cross-sectional analysis.

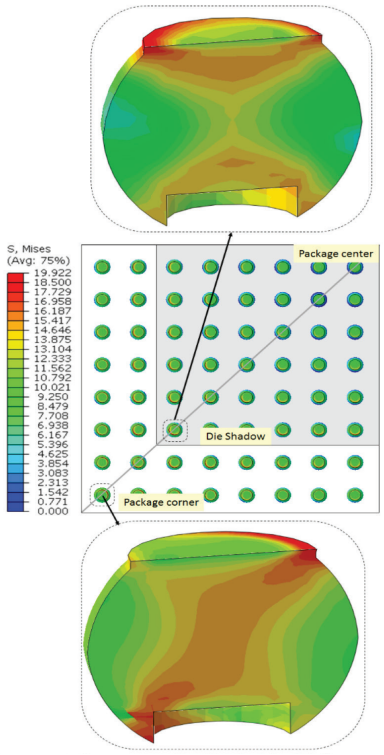

Figure 14. Von Mises stress distribution in SAC305 BGA with Thick conformal coating at 125°C.

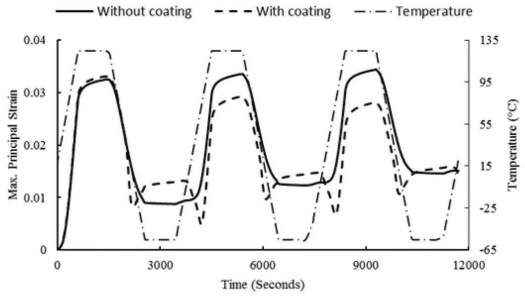

Figure 15. Maximum principal strain over time and temperature with and without conformal coating for SAC305 corner solder joint under Temperature Profile 1.

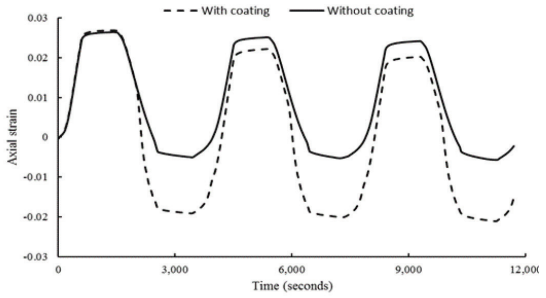

Figure 16. Axial stress distribution with time for SAC305 corner solder joint under Temperature Profile 1 with and without Thick conformal coating.

At the start of the subsequent thermal cycle, the interface of the SAC305 solder joint is under compressive loading. The existence of a compressive preload has been previously shown to contribute to larger accumulation of plastic work per thermal cycle [12]. In this case, the compressive preload occurred at the cold temperature dwell and continued up to the glass transition temperature at which the acrylic material softens. A similar trend is observed at both temperature profiles, with higher strains resulting from more severe temperature profile temperature extremes.

5.2 Sn63Pb37 BGA

The stress-strain behavior of the Sn63Pb37solder joints at the interface is similar to that observed in SAC305 components only with noticeable difference in magnitude. **Figure 17** illustrates the maximum principal strains at the corner BGA with and without Thick conformal coating at the high temperature dwell.

The strain distribution confirms the dominance of the distance-to-neutral-point effect in the Sn63Pb37 components. **Figure 18** illustrates the same Sn63Pb37 components during the cold.

With the Thick coating, larger strains are concentrated along the diagonal of the joint as compared to the more uniform distribution of the Control component. This result agrees with the measured impact of the coating on the solder joint life and failure mechanisms observed in the post testing cross sections, temperature dwell, in which case the Thick coating induces a noticeable difference in the stress distribution.

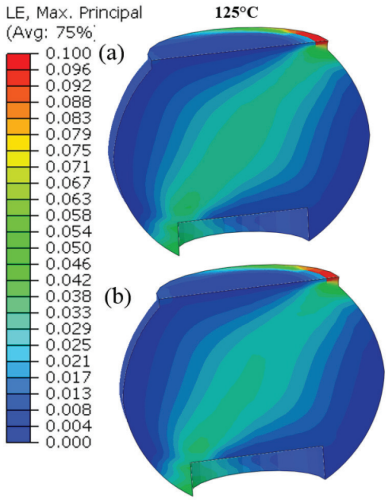

Figure 17. Sn63Pb37 Maximum principal strain at 125°C for the corner BGA: (a) with conformal coating; (b) without conformal coating.

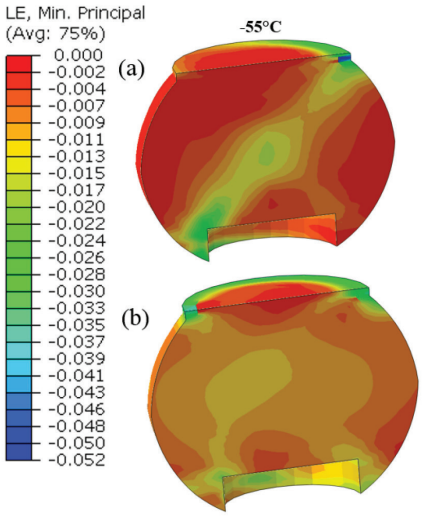

Figure 18. Sn63Pb37 BGA Min. principal strains at -55°C for corner joint: (a) with Thick coating; (b) without Thick coating.

6. Conclusions

This study resulted in identifying the effect of conformal coating materials on solder joint fatigue life in SAC305 and Sn63Pb37 BGA packages. Experimental testing of acrylic conformal coating materials with various temperature dependent CTE and E exhibited failure modes ranging from fatigue to overstress in SAC305 and Sn63Pb37 solder joints. Finite element simulation stress-strain states proved to correlate well with the observed failure modes. An accurate characterization of the conformal coating temperature- dependent properties has shown that the glass transition temperature of the conformal coatings is a critical factor affecting fatigue life. The stresses induced by coatings that pass through their glass transition temperature can be more severe than those caused by the temperature cycle maximum/minimum temperatures. The Sn63Pb37 BGA components were less susceptible to the effects of Thick acrylic conformal coating due to ability to better plastically deform. Additional experimentation is required to fully investigate the influence of conformal coating BGA components by altering the conformal coating materials and package type along with thermal cycling conditions.

Acknowledgments

The authors would like to thank Gil Sharon for his fruitful discussion of the modeling results as well as technical staff of DfR Solutions and Rockwell Collins for assisting with sample preparation, test setup and material characterization.

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Manufacturability Trade-Offs of Bare-Die FCBGA Package Using Thin or Core-Less Substrate:

Package Design Solutions to Maximize Thermal Performance, Improve Package Reliability and Eliminate Warpage Failures Utilizing Bare Die FCBGA

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Abstract

With the increasing demand for thinner packages and higher electrical and thermal performance requirement, bare-die packaging is an inevitable trend that is growing. The assembly process for manufacturing of bare die in thin or core-less substrate FCBGA packages can be challenging, especially considering the effects of substrate warpage during flip chip bonding and the excessive warpage of the flip chip package. We are evaluating the manufacturing risks during bare-die FCBGA package assembly to eliminate package warpage failures using experimental techniques and improve the functional performance of the flip chip package. Various substrate and under fill materials were tested for package warpage values for warpage-free control in the full range of temperature variation. Die designs at 28nm and 40nm process nodes are extremely complex in order to achieve the highest electrical and thermal performance requirement. Die design constraints on advanced process nodes necessitate increased thermal dissipation requirements thereby requiring investigation of thermal solutions utilizing thermal interface materials (TIM) with heat-sink. The interaction of such thermal solutions with the bare die packages is evaluated using various trial and error for material selection, experimental and simulation techniques to improve the assembly process. This study also focuses on selection of thermal interface materials [TIMs] and heat sinks which have considerable impact on die integrity during package assembly and/or during process of removal for failure analysis.

Keywords

bare die, lidless, FCBGA, manufacturing risks, thermal performance, package reliability, package warpage

1. Introduction

High performance, low cost flip chip BGA SoC consumer product requirements continue to drive submicron circuit designs in advanced CMOS process geometries and FCBGA package designs in thinner package profiles. Thermal performance improvements for space-constrained system enclosures drive package transition from over molded FCBGA to exposed bare die (lidless) FCBGA packaging [1]. Electrical performance, especially higher device signal frequency and lower voltage supply margins, are also driving bare die FCBGA designs to FCBGA chip-scale packages (CSP) with thin or coreless substrates. Bare die FCBGA and FCCSP designs are where die mechanical stress and substrate warpage (associated with manufacturing processes, board assembly, and subsequent reliability) become increasing constraints to quality and reliability. A review of the control plans of standard FCBGA manufacturers also indicate, that in many cases, bare die manufacturability concerns are not sufficiently addressed by the over-molded control plans except in the critical optical inspections as part of the manufacturing process flow. This requires a more comprehensive emphasis on factors pertaining to die/substrate material selection/properties, package design/ manufacture, package assembly, and subsequent damage mitigation during volume manufacturing assembly, test and customer handling. This paper captures our experiences in evolving from over molded FCBGA to a high performance, thin core bare die FCBGA and FCCSP packages and leveraging off our experiences and overcoming technology limitations from a legacy process technology node device in a coreless substrate FCBGA package and applying best practices to scale and prepare for new products in advanced process node bare die (lidless) and lidded packages in coreless substrate packages.

2. 28nm Process and Thermal Management

As die design circuit feature sizes continue to shrink below 100 nanometers, leakage current becomes the major component of static power consumption [2] [3]. In semiconductors, there are two components that contribute to the total leakage I_{leak}: subthreshold voltage leakage I_{sub} and gate oxide tunneling leakage Iox per the following equation:

$$I_{leak} = I_{sub} + I_{ox}$$

Subthreshold Leakage: As geometries become smaller, drain-source junctions get closer. Leakage exhibits a draining of carriers from the drain junction at subthresh-

old voltages. Since the behavior is dominated by drain of carriers (rather than drift), they form a complex behavior with temperature and increases non-linearly. Leakage current due to subthreshold voltage leakage is described by the equation below.

$$I_{sub} = K_1.W.\exp^{-\frac{V_{th}}{n.V_\theta}} .\left(1 - \exp^{-\frac{V}{V_\theta}}\right)$$

$$V_\theta = 25\ mV\ varies\ linearly\ with\ temperature$$

Oxide Tunneling: As geometries scale, oxide thickness scale down as well. With reduced oxide thickness, tunneling of electrons increase and are dependent on the temperature. Tunneling is a quantum phenomenon and depends on the energy and barrier band-gap. Leakage current due to gate oxide tunneling is described by the equation below.

$$I_{ox} = K_2.W\left[\frac{V}{T_{ox}}\right]^2 \exp^{\left[\frac{-\propto T_{ox}}{V}\right]}$$

During device characterization, the total leakage behavior may be more linear with (NMOS-PMOS) process corners SS (slow-slow) devices, and exhibits non-linear behavior for TT (typical-typical) and FF (fast-fast) devices.

For such an advanced IC design in 28nm (henceforth Test Vehicle A) thermal runaway due to the additional non-linear leakage current was a severe limitation with a standard overmolded FCBGA package, even with a heat-spreader. This necessitated bare die FCBGA package design optimization along with a heatsink to effectively meet the die and package thermal requirements.

3. Package Design and Substrate Warpage

The most relevant parameters in die stress and substrate warpage are the material components and their thickness derived from the mismatch of coefficient of thermal expansion (CTE) between die and substrate materials [4]. The thickness of the material components as a relevant parameter is shown in **Fig. 1**. Increasing the thickness of the compliant underfill clearly reduces the warpage.

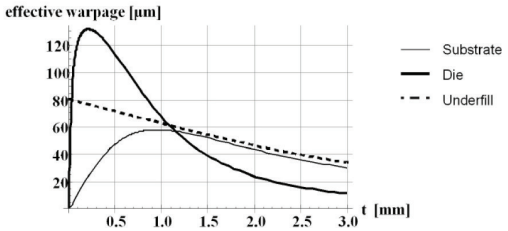

Fig. 1. Effect of thickness of individual layers [4].

In a lidless package, mold thickness and mold cap occupancy are ruled out as contributors to package warpage. The substrate core has the function of providing stiffness and strength to the substrate, while keeping the effective CTE low enough; the core thickness varies greatly from design to design, with a clear trend towards thinner cores. To the effect of evaluating dependent factors and mitigating major package reliability contributors such as excessive warpage, low-k dielectric layer cracking, solder mask cracking, and solder bump cracking [5], we used 3 test vehicle configurations for the study. Test Vehicle A uses a 17x17mm substrate on an advanced 28nm CMOS technology node bare die. Test Vehicle B uses a 10x10mm substrate on a mature 40nm CMOS technology node with an offset bare die. We also leveraged extensive package assembly experiences from Test Vehicle C using an 8x8mm overmolded FCCSP package with coreless substrate package on a legacy 90nm CMOS technology node die.

For a given package configuration there is a die and substrate thickness that also exacerbates warpage. It's been found through analytical modeling how warpage dependence on the thickness ratio is impacted by the substrate Young's modulus (EO), and as depicted in **Fig. 2**, that the die is under the highest stress when the substrate to die thickness ratio is close to 1.0. It is interesting to note that substrate stiffness has a negligible effect beyond a certain value of the thickness ratio, i.e. 3.0 [4].

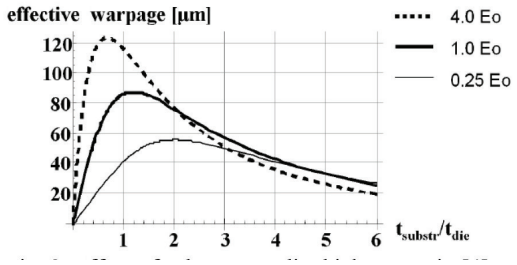

Fig. 2. Effect of substrate to die thickness ratio [4].

Applying this ratio comparison to the 3 test vehicles discussed in Table 1 helps evaluate and compare material property factors to mitigate qualification and reliability issues, as for, e.g., when the die is under the highest stress, package warpage becomes the most critical factor in die cracking, solder extrusion, and solder bump breakage.

Test Vehicle	Process Node	Package Type	Substrate Thickness (mm)	Die Thickness (mm)	Ratio
A	28nm	Bare Die FCBGA	0.590	0.787	0.75
B	40nm	Bare Die FCCSP	0.260	0.300	0.87
C	90nm	Overmold FCCSP	0.170	0.254	0.67

Table 1. Substrate Thickness to Die Thickness Ratio of Test Vehicles A, B, and C

Major influencing factors for overmolded package warpage are material properties, die size, die thickness, substrate thickness, mold thickness, and mold cap occupancy in the substrate area. The effect of package size and die size can be seen in **Fig. 3** which illustrates that warpage varies linearly with package size and it is approximately proportional to the second power of the die size [4].

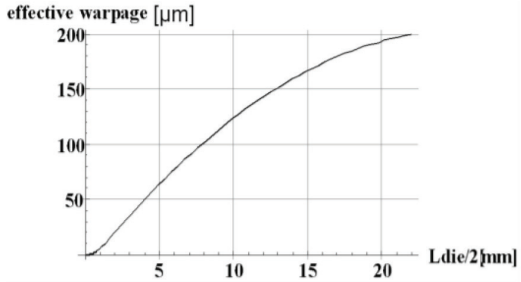

Fig. 3. Effect of die size on warpage [4].

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For Test Vehicle A, 1+2+1 build-up type substrate with low CTE core material (C1) and high tensile strength solder resist material (SR1) was selected. This test vehicle failed reliability testing at post-preconditioning stage due to warpage induced stress during reflow. Upon failure analysis of the failing devices, solder extrusion was found in the substrate vias which caused a short with adjoining traces as depicted in **Figs. 4 and 5**.

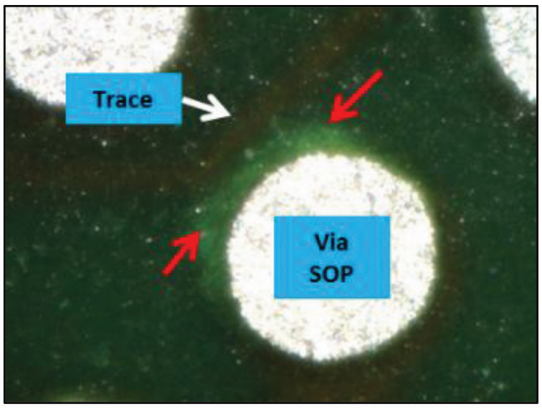

Fig. 4. Optical image of via solder-on-pad (SOP) with solder extrusion.

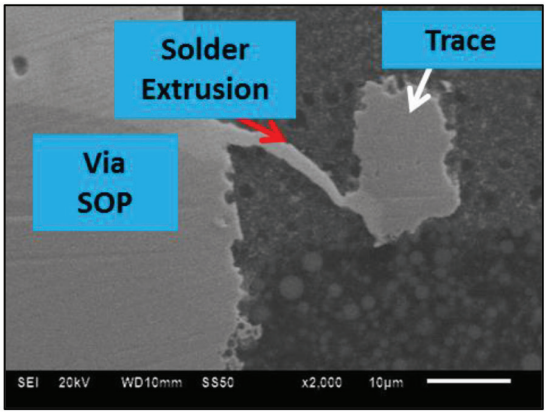

Fig. 5. Cross-section SEM image of solder extrusion and solder bridging between via solder-on-pad (SOP) and adjoining trace.

During reflow (240° C), the contributing factors that exacerbated the solder extrusion failures are:

1) Substrate core C1 had a relatively higher CTE than required coupled with the fact that the tensile strength of solder resist SR1 was lower than required for a lidless package with thin core substrate;
2) Higher ratio of substrate thickness/die thickness;
3) Lower silicon volume/substrate volume ratio;
4) Traces on substrate near the die edge must have more trace spacing to prevent shorts related to package warpage and solder resist cracks.

For substrates with thin core and fine pitch trace designs it is imperative to use ultra-low CTE core material. Hence a new material set was explored for the substrate of this bare die package. New core material C2 which has ultra-low CTE and solder resist material SR2 which has higher tensile strength were chosen. A comparison of material properties of C1 and C2 as well as that of SR1 and SR2 is shown in **Tables 2 and 3**.

Material properties			Unit	PCB Core	
				C1	C2
				V0	V1
Thermal Conductivity			W/m°K	0.81	0.65
Glass transition Temp. (T_g)		DMA	°C	163~173	260
		TMA	°C	207	300
CTE	α_1	X	ppm/°C	14~16	10~11
		Y		15~17	10~11
		Z		25~35	15~25
	α_2	X		11~13	4~6
		Y		12~14	4~6
		Z		140~170	90~120

Table 2. Comparison of Material Properties between PCB Cores of Substrate Versions V0 and V1

Material properties	Solder Resist	
	SR1	SR2
	V0	V1
Tg (°C @TMA)	102	131
CTE (ppm/°C) alpha 1	55	38
CTE (ppm/°C) alpha 2	140	115
Elastic Modulus (GPa)	2.6	3.8
Tensile Strength (MPa)	48	100

Table 3. Comparison of Material Properties between Solder Resists of Substrate Versions V0 and V1

Shadow Moiré test results of substrate version V0 (with C1 and SR1 materials) and V1 (with C2 and SR2 materials) are shown in **Figs. 6 and 7**. The Shadow Moiré graphs in Figs. 6 and 7 show that V0 version of substrate has higher warpage during reflow in comparison with V1 version.

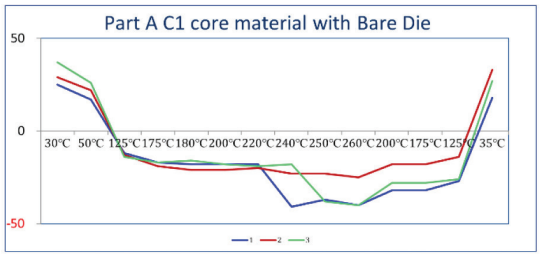

Fig. 6. Shadow Moiré graph of test Vehicle A with V0 substrate with bare die.

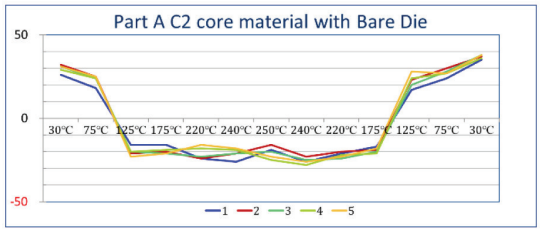

Fig. 7. Shadow Moiré graph of test Vehicle A with V1 substrate with bare die has lower warpage than V0 substrate version.

The improvement in warpage of test Vehicle A with V1 substrate with change in core and solder resist materials led to improved reliability results. Test Vehicle A version V1 substrate passed all reliability qualification tests, especially precondition test (reflow at 240°C). **Fig. 8** shows the SEM cross section image of the same via and trace on V1 substrate which had solder extrusion in case of V0 substrate reflow test. No solder extrusion was observed post precondition in the test Vehicle A with V1 substrate.

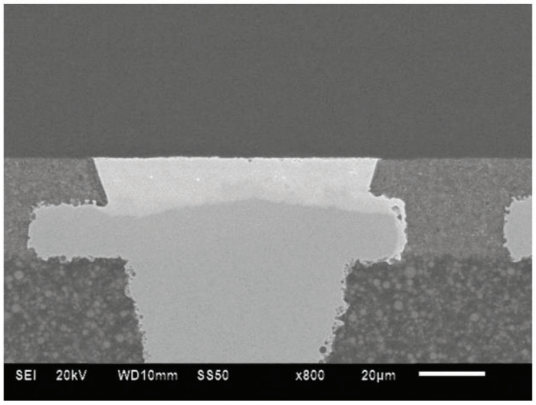

Fig. 8. Cross-section SEM image of critical via in V1 substrate. No solder extrusion was observed.

For test Vehicle B, a 1+2+1 build-up type substrate was selected. In this case, with a less fine pitch trace design, it was acceptable to use a more normal CTE thinner core material than test Vehicle A. Test Vehicle B overmolded package version exceeded thermal limits during normal functioning leading to a need for bare die package. Various process techniques for lidless packages were explored including film mold, strip grinding and no mold packages. The film mold and no mold techniques require a capillary underfill while the strip grind technique uses a molded underfill (MUF) material. The Shadow Moiré test of all four package types is shown in **Fig. 9**. Overmold package has lowest warpage but poor thermal performance. Strip grind technique had worse warpage than no mold and film mold packages. Film mold package has low warpage but there is a risk of film bleed on die during assembly, hence the no mold option was selected.

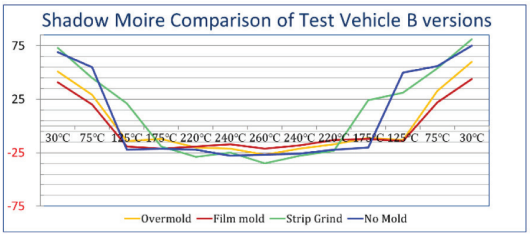

Fig. 9. Shadow Moiré of various lidless package process techniques in comparison with overmolded package.

Test Vehicle B has poorer thermal performance, so die back grind to less than half the wafer thickness was required along with underfill and substrate thickness optimization for warpage reduction. The latter required a detailed case study of normal and low cost underfills and thicker and thinner substrate core materials. Hence the material set was explored for the underfill and substrate CTE of this bare die package. Underfill material UF1 which was more compliant (low CTE) and had higher cost was chosen. A comparison of underfill material properties of UF1 and UF2 are shown in **Table 4**.

Model Name	Units	UF1	UF2
Resin type	-	Epoxy	Epoxy
Hardener type	-	Biphenyl	Phenol
Particle Size	um	30	10
Tg (TMA)	'C	141	80
CTE α1 / α2	ppm/'C	11/39	32 / 120
Modulus @ 25°C	GPa	24	8.0
Cost	$	High	Low

Table 4. Comparison of Underfill Materials UF1 and UF2 for Test Vehicle B with Bare Die

Test Vehicle C uses a 0.170mm thin coreless substrate for an 8x8mm overmolded FCCSP package.

Both Molded Under Fill (MUF) and Capillary Under Fill (CUF) processes were considered for test vehicle C. MUF approach offers a unique solution with promising advantages over CUF such as lower material cost, higher through put and reliability to meet the overall product needs [6].

Although MUF process has multiple advantages, it was challenging to use MUF material on test vehicle C with eutectic bumps as it has a lower melting temperature compared to Pb-free bumps. The MUF material requires higher reflow temperature than with CUF.

Typically, very high mold temperatures are required to allow good mold flow of MUF material which is in the close vicinity of the melting temperature of eutectic bump (~183°C). Hence it is preferred to use materials with a wide working temperature range and that can be molded at a much lower temperature than 183°C as possible to avoid melting bumps during the mold process which could otherwise cause the device chip to de-wet from the package substrate during molding process [6].

The melting temperature of MUF material used with test vehicle C is 150°C but for better flow the temperature needs to be close to 170°C with a process variability of +/- 10°C. During initial engineering builds with the MUF process all X-ray and CSAM results were normal. Test Vehicle C also passed all reliability tests. Pilot lot test of test vehicle C using MUF encountered higher continuity fails. Upon failure analysis, it was found that the eutectic bumps melted and formed solder bridge with neighboring bumps due to the higher molding temperature. **Fig. 10** shows an SEM image of a continuity test failing unit with molten bumps causing solder bridging.

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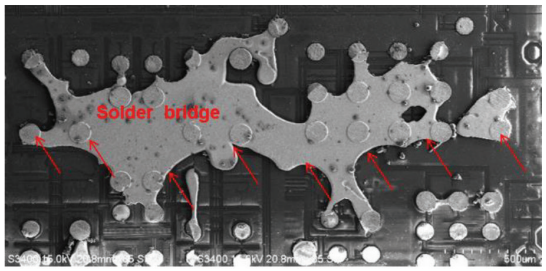

Fig. 10. Solder bump bridging due to molten solder bumps.

To improve production assembly yield as well as prevent melting of bumps during molding process, the MUF process temperature window was optimized and restricted to 165°C (+/- 10°C).

Test Vehicle C uses a coreless 3-layer embedded trace substrate. Coreless substrates are thinner than build-up substrates. These thinner coreless substrates warp more than the build-up substrates as they lack the core that provides thickness and strength to the package. Substrate warpage can lead to reliability failures like bump IMC cracks, die cracks, etc. during the flip chip process step or during the reflow post flip chip process. Some precautions need to be taken during the flip-chip process and reflow steps to avoid defects like die cracks and bump IMC cracks. Some units from pilot production lots failed continuity tests and failure analysis revealed cracks in bump IMC as shown in **Fig. 11**.

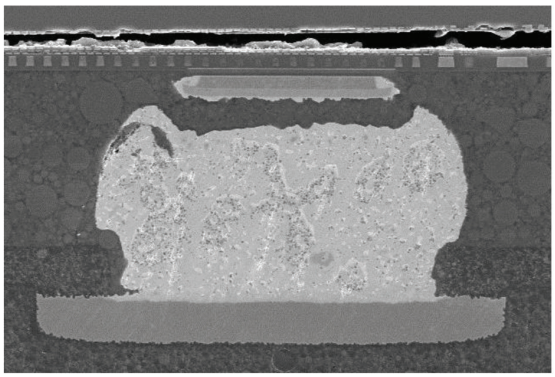

Fig. 11. Bump IMC crack and die crack due to substrate warpage during reflow.

Upon comparison of assembly process records, the thin core substrates were found to be warping in strip form during reflow post flip chip step. The warpage of strip led to cracks in bump IMC of corner edge bumps. To reduce substrate warpage during reflow, substrate strip carrier boat used during reflow step in **Fig. 12(a)**, was replaced with a mesh type carrier boat as shown in **Fig. 12(b)**. This mesh type carrier boat provides stability for each substrate location on the strip.

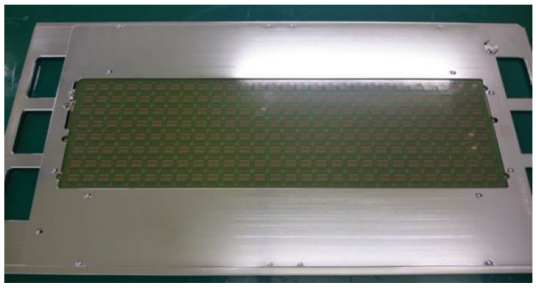

Fig. 12(a). Normal substrate carrier boat which is used for thicker substrates.

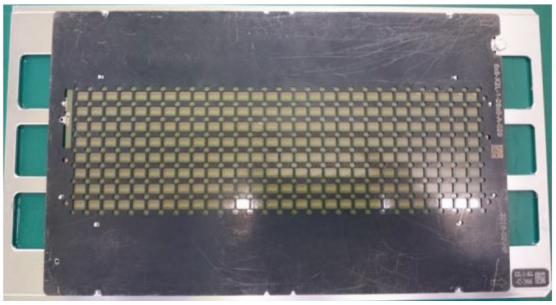

Fig. 12(b). Mesh type carrier boat is needed for thin coreless substrates.

4. Thermal Optimization

Along with bare die FCBGA package design optimization for warpage, a heatsink is required to effectively optimize the die and package thermal requirements. In this thermal architecture, a low-profile heatsink is typically applied directly to the back side of a silicon device through a thermal interface material (TIM). The TIM bond line thickness (BLT), interface material area, and interface material thermal conductivity must be selected to optimize the total thermal solution. The preferred TIM material is a double-sided pressure-sensitive adhesive (PSA) tape with an electrically insulating composite material type ceramic filled acrylic polymer. PSA adds mechanical strength to the bond between the bare die and the heat sink. These tapes have been found to last greater than ten years versus aluminum foil type PSA tapes which only last up to three years when used across extended temperature ranges [7].

Another TIM material, designed to meet the thermal reliability requirements of high-end thermal applications, is a thermal phase change material (TPCM) [8]. Per the material datasheet [9], "TPCM begins to soften and flow at temperatures above its Tg transition temperature (typically 50ºC), filling the microscopic irregularities of the components it comes into contact with. The result is an interface with minimal thermal contact resistance. Due to the gradual change in viscosity (softening), it minimizes migration (pump-out)." It should be noted that whatever TIM (PSA or TPCM) is selected, the material should be qualified by the TIM supplier per ASTM D5470 [109].

5. Other Manufacturing Risks and Failure Types

Apart from the aforementioned examples (solder extrusion, bump crack, and die crack due to substrate warpage during reflow), we have experienced a number of potential risks in other parts of the manufacturing flow. A few examples are shown in **Figs. 13, 14 and 15**.

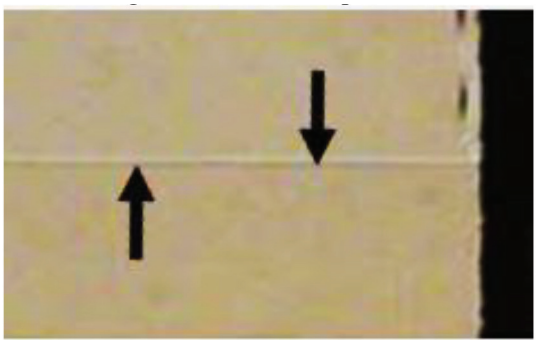

Fig. 13. Backside die crack due to foreign particle on the wafer chuck table during wafer backgrind.

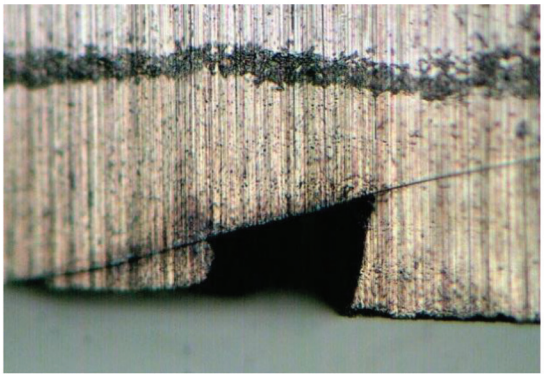

Fig. 14. Backside crack/chipout after wafer saw.

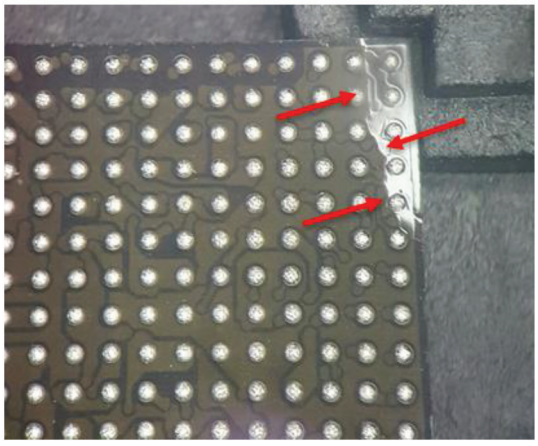

Fig. 15. Substrate crack during assembly/test.

6. Summary and Conclusion

With shrinking die circuit feature sizes and increasing complexity of die circuit designs in advanced process nodes there is a need to investigate and understand FCBGA die/package interactions to ensure package and die functioning as well as reliability are not being compromised during volume manufacturing. Initially the thermal management of an advanced SoC design was considered in the use of a bare die package. Later bare die and overmolded FCBGA test Vehicles A, B and C with varying materials, substrate and die thickness were investigated. The impact of CTE of substrate core, solder resist material, die and substrate thickness on warpage was understood. Next the bare die heatsink thermal architecture was optimized with the selection and qualification of thermal interface materials [TIMs]. Finally, some actual examples of failure categories across the manufacturing and test flows were presented. All of these findings to date has helped set us on the next path, which is to investigate bare die with coreless substrate packaging for future FCBGA advanced SoC products.

Acknowledgment

The authors would like to acknowledge and appreciate the efforts from Signetics and ASE ChungLi for their valuable contributions towards this paper.

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Conformal Coatings and Area Array Components

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Introduction

High performance electronic products must continue to operate in life critical/operational critical situations, even in a harsh environment. These products often include conformal coating materials to protect printed circuit assemblies from dirt, moisture and other detrimental environmental hazards. The Restriction of Hazardous Substances (RoHS) legislation has led to a growing use of conformal coating materials as a tin whisker risk mitigation strategy. In these applications, conformal coating material must be consistent in terms of thickness and coverage on the printed circuit assembly. Since the absence of conformal coating on adjacent leads of a leaded surface mount component can increase the risk of shorting due to corrosion or tin whiskers, coating processes generally strive for uniform coverage over all surfaces. However, the desire to ensure that all surfaces be adequately coated can potentially lead to excessive coating that can adversely affect solder joints in area array components such as ball grid arrays (BGAs), chip scale packages (CSPs) and flip chips (FCs). Studies have shown that the presence of conformal coatings underneath area array components generate stresses that can lead to solder damage, such as that shown in **Figure 1**.

The solder joint deformation in Figure 1 occurred after components had been subjected to thermal cycle conditioning. The deformation results from the global coefficient of thermal expansion (CTE) mismatch between the BGA package, the solderballs, the conformal coating material and the printed circuit board laminate. The modulus of elasticity (E) of the various constituents of the coated BGA also contributes to generating thermal stresses in the solder joints. These two properties, CTE and E, of the packaging materials interact in different ways depending on the package geometry and use environment. This article briefly describes a number of studies that have been conducted by Rockwell Collins to better understand the mechanisms by which conformal coatings can influence solder joint reliability in BGA and FC area array components

Ball Grid Array Components

A series of tests were used to investigate the effects of conformal coatings on the reliability of BGA packages. Reliability was assessed through thermal cycle conditioning in which components were subjected to temperature cycles while the electrical continuity of their solder joints was monitored. Tests were conducted to assess the effects of a number of design/test parameters on the impact of conformal coating on BGAs.

- A variety of different conformal coating materials are available and the decision regarding which material to use in a given application depends on the environmental conditions in which it will be used as well as costs related to the material and its application processes. While tests have been conducted with a wide variety of conformal coating materials [2], this article

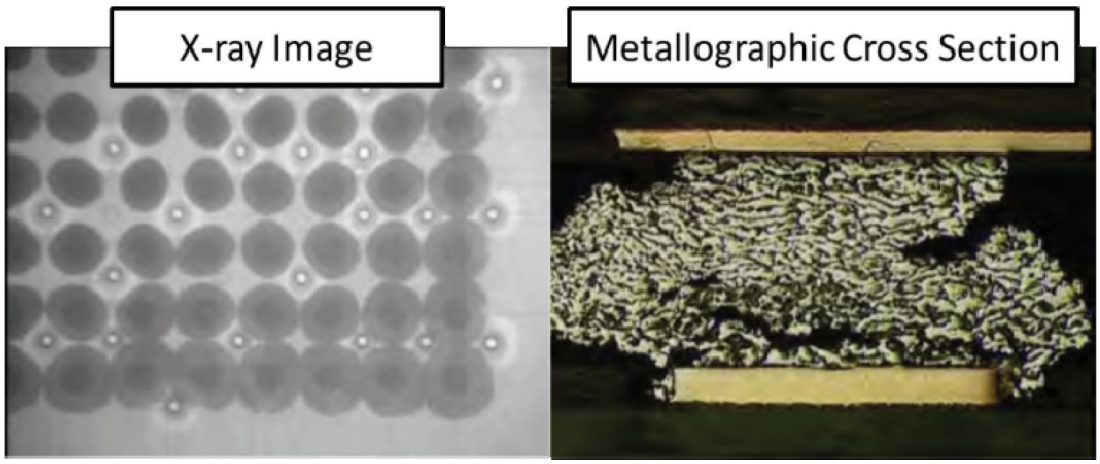

Figure 1: Top and side views of BGA solder joints with improper conformal coating after thermal cycling [1].

will only discuss the results for acrylic- and silicone-based conformal coatings.

- A number of different application methods, such as spraying, dipping, and brushing, are used with conformal coatings. Depending on the application method, coating thickness can be increased to influence the level of protection that it provides.
- Many harsh environment electronics systems, such as avionics, may be exempt from requirements for lead-free assembly. However, these systems may also use leading edge components that are only available with lead-free solder. Therefore, tests were conducted with both eutectic tin-lead (SnPb) and lead-free (SAC3015) solder balls on the BGAs.
- Different levels of accelerated life testing, based on thermal cycle conditioning, are used in different industries and by different OEMs. This testing used two different levels of thermal cycling to compare the effects of high stress conditions.

Testing was conducted with daisy chain BGAs (17mm x 17mm, with 256 solder balls on a 1mm pitch) soldered to a 0.081 inch (2mm) FR-4 circuit board with an immersion silver surface finish. The circuit board included 8 inner layers of copper traces to simulate the effect of copper interconnect on the board's thermal expansion. Details on the test board assembly are provided in Ref. [2]. After the circuit boards were assembled, they were conformally coated with different materials including acrylic- and silicone-based coatings. One half of each test board was coated using 'Standard' conformal coating practices while the other half of the test board was coated with a manual process using a pneumatic syringe to completely fill the conformal coating material under each BGA. This configuration, which is referred to as the "Thick" application, represents a worst-case scenario of conformal coating application that can occur in dipping method and heavy spray coating applications. Additional 'Control' test boards were left uncoated.

Figure 2 shows a test board under normal lighting as well as black light, which more clearly indicates the different levels of coating thickness.

Test boards were placed in two different thermal chambers and subjected to two different levels of thermal cycle conditioning. One chamber, at Rockwell Collins, used a temperature range of -55°C to +125°C while the other chamber, at DfR Solutions, used a temperature range of -20°C to +80°C. Both profiles used a minimum 15 minute dwell time at each temperature extreme and a ramp rate of 5-10°C/minute, per IPC-9701. The daisy chain configuration of the BGAs allowed the solder joints to be electrically monitored to determine when a solder joint on a device became electrically open.

Figure 3 shows reliability data for conformally coated BGA components with SnPb solder when subjected to thermal cycling of -55 to +125°C. The cumulative failure rate of each population is plotted against the number of thermal cycles. This figure shows the effects of two conformal coatings (acrylic and silicone), with both 'Standard' and 'Thick' conditions. Symbols indicate test data while lines show calculated Weibull distributions for each data set. The plot also includes 'Control' components that had no conformal coating. Results show that the components with Thick coating failed earlier than the control samples. The components with Standard acrylic coating failed somewhat earlier than the Control samples while those with silicone coating appeared to be unaffected by the coating. Note that the Control and acrylic test boards were removed from the thermal chamber after 500 cycles so that cross section analysis could be performed, hence the data in the plot appear to be truncated.

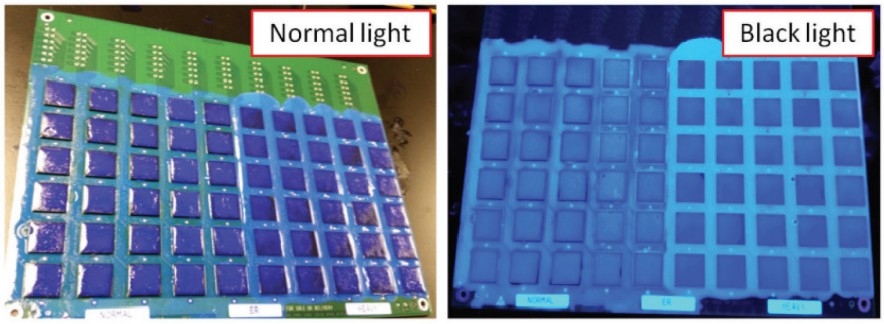

Figure 2: Conformally coated BGA test board (left side has 'Standard' coating; right side has 'Thick' coating).

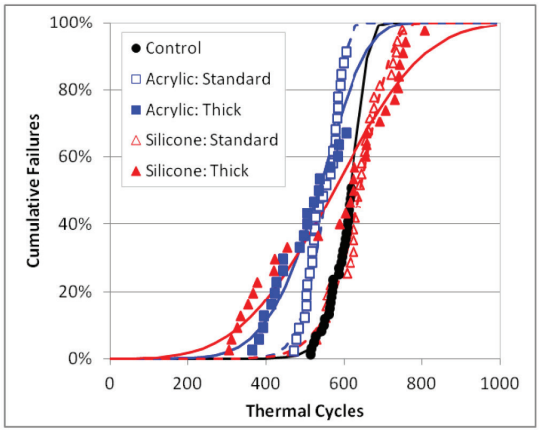

Figure 3: BGA reliability: SnPb solder, -55 to +125°C thermal cycle profile.

Figure 4

Figure 4 shows similar data for components with SAC305 lead-free solder, again with the -55 to +125°C thermal profile. Interestingly, the Standard acrylic coating substantially improved the reliability of the components relative to the Control samples. The Standard silicone coating also improved the SAC305 BGA reliability, but to a much lesser extent. Thick coatings decreased the reliability to the same degree for both of these coatings. The reduced reliability of the SAC305 Control components, relative to those with SnPb solder, is typical for components tested at these severe thermal cycling conditions [3].

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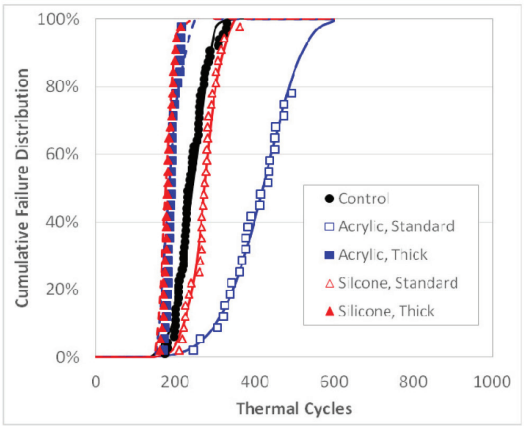

Figure 4: BGA reliability: SAC305 solder, -55 to +125°C thermal cycle profile.

Figure 5

Figure 5 shows the component reliability results when the BGAs were subjected to the less severe -20 to +80°C thermal cycle. This shows somewhat different results, with the Control samples exhibiting the highest reliability and the samples with Standard conformal coating having measurably lower reliability. The control and Standard coated samples survived far more thermal cycles at the less severe thermal cycling profile than in the more severe cycling profile of -55 to +125°C. In contrast, the samples with Thick coating had similar reliability characteristics for both thermal cycle profiles.

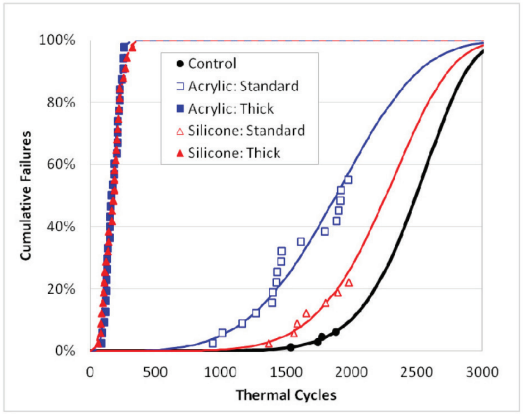

Figure 5: BGA reliability: SAC305 solder, -20 to +80°C thermal cycle profile (courtesy of Maxim Sebrini, DfR Solutions).

Table 1

Table 1 summarizes the Weibull coefficients calculated for the different tests. Note that SnPb components were not tested at the -20 to +80°C thermal cycle profile. The Weibull distribution is shown in Equation 1. Weibull coefficients were determined using a regression analysis of the data to estimate the values of the characteristic life, η, and the slope, β. The characteristic life, which is often referred to as N63, is an indicator of the average life of the population and corresponds to the number of cycles in which 63.2% (=1-1/e) is expected to have failed. The Weibull slope is an indication of manufacturing consistency; if all components were to fail at precisely the same point, the slope would be infinite.

$$F(t) = 1 - \exp\left(-\frac{t}{\eta}\right)^{\beta} \qquad \text{Equation } \{1\}$$

Table 1 quantifies the results that were previously observed by assessing the plots in Figures 3-5. All of the results for SnPb solder showed a characteristic life in relatively narrow range of ~550-650 cycles, with the samples with acrylic coating being lower than the others. The Thick coatings led to lower shape factors in the SnPb samples with severe thermal cycling and SAC305 with milder thermal cycling, which suggest that the failure mechanism was less uniform with those combinations.

Figure 6

After thermal cycling, selected components were removed from the test boards for metallographic cross sectioning analysis. **Figure 6** shows cross sections of solder balls on the outer rows of components with acrylic coating. The top row of images corresponds to SnPb solder while the bottom row corresponds to SAC305. Moving left to right, each column indicates more coating (from none, to Standard, to Thick). The SnPb solder ball with Standard coating does show some deformation and indications of stress. The Thick coating samples show extreme deformation of the SnPb and SAC305 solder balls. This solder joint damage appears to be the result of the BGA being pulled down to the circuit board by the conformal coating as it contracted during the low temperature portion of the thermal cycle. The solder joints failed due to separation from a bond pad as a result of this axial force. In the case of the SnPb solder joint, a cohesive failure in the solder led to this separation while the SAC305 solder joint appears to have suffered from an adhesive failure.

Table 1: Calculated Weibull Coefficients for BGA Conformal Coating Tests

Thermal Cycle Profile		-55 to +125°C				-20 to +80°C	
Solder		SnPb		SAC305			
Coating	***Thickness***	η	β	η	β	η	β
Control	n/a	629	17.0	256	7.92	2604	8.42
Acrylic	Standard	567	14.6	448	5.74	2054	4.15
	Thick	568	6.14	171	19.7	191	3.78
Silicone	Standard	665	10.6	286	9.19	2398	6.31
	Thick	636	3.58	161	16.8	193	2.84

Figure 7

Figure 7 shows similar results for the components with silicon conformal coating. These images do not show the same level of severe damage in the thick coated materials. However, the SnPb solder joints clearly have been subjected to high stress levels.

The differences in the reliability characteristics of the solder joints are due to complex interactions resulting from the combination of the temperature-dependent solder properties, the temperature-dependent properties of the conformal coating (primarily the temperature-dependent modulus of elasticity and the coefficient of thermal expansion), the temperature cycle and the specific package geometry. A 'quick and dirty' simplified finite element analysis (FEA) of the effects of the package and conformal coating was unable to correlate the predicted stresses and failure rates [3]. A much more comprehensive FEA, which includes non-linear effects and more detailed measurements of conformal coating properties, is ongoing and has shown encouraging results [4].

Flip Chip Components

Flip chip (FC) components are typically underfilled to improve solder joint integrity during thermal expansion and dynamic loading. The presence of underfill prevents conformal coating from ingressing underneath these parts. Therefore, there is typically little concern about a potential reliability impact of conformal coating on FC solder joints. However, testing has demonstrated that some extremely small FC components can be qualified for use in high-rel environments without being underfilled. Therefore, testing was conducted to assess the effects of a specific conformal coating, as applied using standard processes, on the thermal cycle reliability of a number of low I/O flip chip components. **Table 2** lists the geometries of the components included in this study. All components used SAC305 solder.

Table 2: Flip Components Tested with Acrylic Conformal Coat

ID	#I/O	Size	Ball Diameter	Pitch
1	4	0.81mm x 0.81mm	0.26 mm	0.4 mm
2	4	1.6mm x 1.6mm	0.39 mm	0.8 mm
3	6	1mm x 1.5mm	0.33 mm	0.5 mm
4	4	0.8mm x 0.8mm	0.22 mm	0.4 mm
5	4	11 x 13 mm	0.6 mm	1.0 mm
6	4	0.86mm x 0.86mm	0.26 mm	0.4 mm
7	6	1mm x 1.5mm	0.29 mm	0.5 mm

Unlike the BGA components evaluated in the previous studies, the FC components were not available in daisy chain configurations. Therefore, the electrical continuity of the solder joints could not be continuously monitored. Instead, components were evaluated by removing a portion of the population at various points in the thermal cycle conditioning process and metallographic cross section assessments were made to assess the physical state of the solder joints. Furthermore, since this work was part of a qualification evaluation of components as assembled in a factory setting, only a single conformal coating process and material was used. A 'dry spray' process using a hand held sprayer with fixed levels of spray and air assist pressure was used to coat the devices with a 'Standard' process that components would encounter in production.

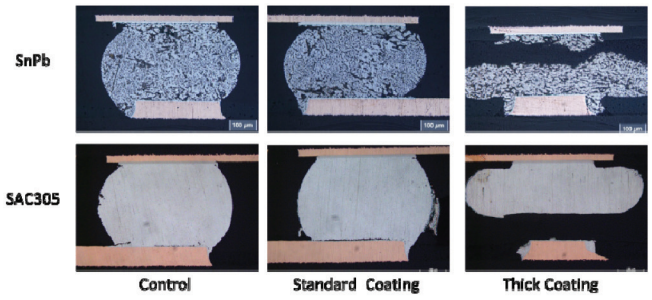

Figure 6: Cross sections of solder joints with acrylic conformal coating.

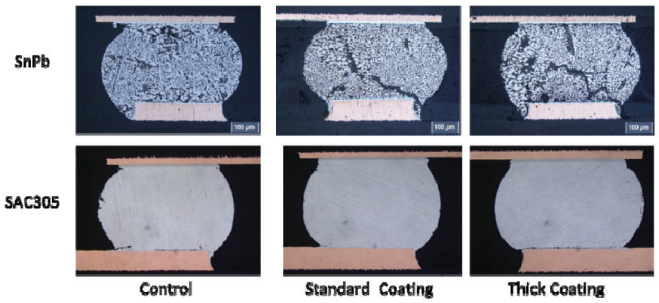

Figure 7: Cross sections of solder joints with silicone conformal coating.

Figure 8

Figure 8 shows an example of a metallographic cross section of a flip chip component. In this case, the image was purposely overexposed to illustrate the locations of conformal coating, which is black in the image and noted with arrows.

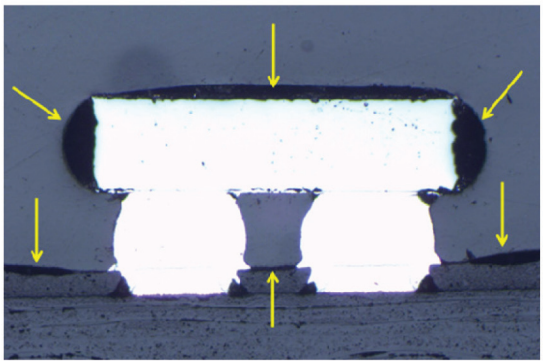

Figure 8: Overexposed image of flip chip cross section (to illustrate conformal coating coverage).

The flip chip components were tested for 1000 thermal cycles of -55 to +125°C, using the same IPC-9701 specification ramp and hold rates used in the BGA testing. Individual components were removed at ~200, 400, 500, and 1000 thermal cycles so that they could be cross sectioned. **Figure 9** shows example cross sections for the 1mm pitch flip chip component (ID #5 in Table 2). Inspection of the cross sections for all parts included in the study found that (a) solder joints did not exhibit any cracks at the end of 1000 thermal cycles, and (b) the production spraying process did not result in any of the FC solder joints being encapsulated with conformal coating.

continued on page 24

continued from page 23

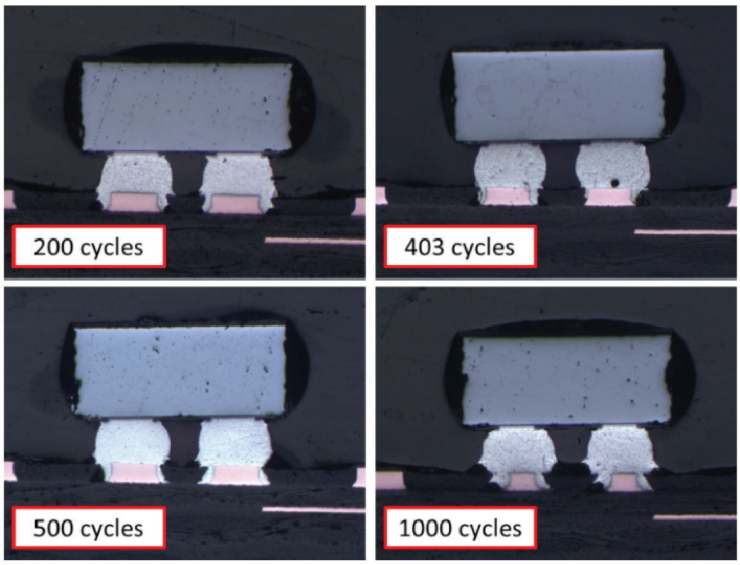

Figure 9: Cross sections of FC (ID #5) after thermal cycling.

Summary/Conclusions

Testing results showed if conformal coating can get under area array components, it can significantly degrade solder joint reliability. The overall impact of the conformal coating depends on the geometry of the area array part, the solder alloy, the temperature cycle effects and the material properties of the coating material itself. Properly applied conformal coating tends to have minimal ingress under area array components, particularly in smaller parts such as flip chips.

Acknowledgements

This work summarizes a number of investigations by Rockwell Collins to assess the effects of conformal coatings on area array components. The work includes internal research projects, collaboration with DfR Solutions and student design projects at Iowa State University. The authors acknowledge contributions to these various projects by: Doug Pauls, Dan White, Katelyn Gilbertson, Kim Cho, Mark Dimke (Rockwell Collins); Mason Hasty, Khalid Alamri, Jeff Kuderer, Qinyu Liu, Charmaine Johnson, Dianna Blais, Shengjie Zhuang (ISU); Maxim Sebrini, Nathan Blattau, Craig Hillman (DfR Solutions).

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1. D. Hillman, et al., "Flip Chip Component Technology Qualification for High Performance Avionics Products," SMTAI Conference, Chicago IL USA, 2014.
2. R. Wilcoxon, et al., "The Impact of Improper Conformal Coating Processes on BGA Solder Joint Integrity," SMTAI Conference, Chicago IL USA, 2015.
3. J.-P. Clech, "Lead-Free and Mixed Assembly Solder Joint Reliability Trends," Proceedings of APEX 2004, S28-3, Anaheim CA USA, February 24-26, 2004.
4. M. Sabrini, "The effect of improper conformal coating on SnPb and Pb-free BGA solder joints during thermal cycling: Experiments and modeling," SEMI-THERM Symposium, San Jose CA USA, 2017.

IMAPS 14th International Conference and Exhibition on
Device Packaging

www.imaps.org/devicepackaging

We-Ko-Pa Resort and Casino
Fountain Hills, Arizona - USA
March 5-8, 2018

General Chair:
Peter Ramm
Fraunhofer EMST

Past General Chair:
Gilles Poupon
CEA

Call For Abstracts Now Open On-Line!
ABSTRACT and PDC DEADLINE: October 20, 2017

The 14th Annual Device Packaging Conference (DPC 2018) will be held in Fountain Hills, Arizona, on March 5-8, 2018. It is an international event organized by the International Microelectronics Assembly and Packaging Society (IMAPS). The conference is a major forum for the exchange of knowledge and provides numerous technical, social and networking opportunities for meeting leading experts in these fields. People who will benefit from this conference include: scientists, process engineers, product engineers, manufacturing engineers, professors, students, business managers, and sales and marketing professionals. The 2018 conference will feature ***4 keynote presentations***, an embedded ***Global Business Council Forum***, an interactive poster session, panel discussions and more.

Featuring 3 Topical Workshop Tracks on

- **INTERPOSERS, 3D IC and PACKAGING**
- **FAN-OUT, WAFER LEVEL PACKAGING, and FLIP CHIP**
- **ENGINEERED MICRO SYSTEMS/DEVICES**

(including MEMS and Sensors; Chaotic/Non-Linear Systems, and more)

Those wishing to present their work at the Device Packaging Conference must submit a 500+ word abstract electronically **no later than OCTOBER 20, 2017**, using the on-line submittal form at: www.imaps.org/abstracts.htm. No formal technical paper is required. A reproduction-ready two- to six-page concise summary ("extended abstract") with text (figures and graphs included if necessary) will be required for the Conference "APP" and Download on Friday, January 19, 2018. A post-conference DOWNLOAD containing the full presentation material as supplied by authors will be mailed 15 business days after the event to all attendees. Please contact Brian Schieman by email at bschieman@imaps.org if you have questions.

Device Packaging Exhibit and Technology Show:
IMAPS will hold a concurrent exhibition for vendors and suppliers who support the many aspects of **Device Packaging**. This venue features an ideal atmosphere to showcase your products and services to key decision making professionals in the industry. Only 65 full 8' by 10' exhibit spaces will be available. To reserve booth space, please fill out the application form before December 1, 2017 at: www.imaps.org/devicepackaging or contact Brian Schieman by email at bschieman@imaps.org. ***The exhibits have sold out every year since 2006 and we expect a sell-out again in 2018 - so book long before December (sold out in OCTOBER in 2016)!***

Device Packaging Professional Development Courses (PDCs):
For those wishing to broaden their knowledge of device packaging, a selection of half-day courses will be offered on Monday, March 5th, preceding the technical conference. If you would like to participate as an instructor, please submit a description of your short course on-line at www.imaps.org/pdc **no later than OCTOBER 20, 2017.**

Go on-line to www.imaps.org/devicepackaging for all your DPC 2018 information and to register.

Schedule-at-a-Glance

Monday, October 9	
9:00am-12:00pm	**David C. Virissimo Golf Tournament** Supporting the Microelectronics Foundation
8:00am-5:30pm	**Professional Development Courses** *Track A Courses* *Track B Courses* *Track C Courses* *Track D Courses*
10:00am-3:00pm	**Microelectronics Industry Tour of Micross Components**
5:30pm-7:30pm	**Welcome Reception**
7:00pm-7:45pm	**Celebrating Diversity Reception**

Tuesday, October 10	
8:00am-8:15am	**Welcome from IMAPS President**
8:15am-11:45am	**Keynote Addresses** **Title TBD** Roawen Chen, Qualcomm **Packaging Without the Package – A More Holistic Moore's Law** Subu Iyer, UCLA **Electronics Outside the Box: Building a Manufacturing Ecosystem for Flexible Hybrid Electronics** Ben Leever, Air Force Research Laboratory **Transforming Electronic Interconnect** Tim Olson, DECA
11:45am-12:00pm	**What's Next for IMAPS?** Urmi Ray, VP of Technology
12:00pm-5:00pm	Exhibit Hall Open
12:00pm-2:30pm	Lunch in the Exhibit Hall
2:30pm-6:25pm	**Technical Presentations in Session** *Materials and Reliability I* *Packaging to Meet the RF Roadmap – 2.4 to 26 to 60 GHz* *3D Technologies: Materials, Processes, and Applications* *Wafer Level Packaging and Panel Level Packaging* *Novel Materials/Processes I*
7:00pm-10:00pm	President's Party and 50th Anniversary Celebration *By Invitation Only*

Schedule-at-a-Glance

Wednesday, October 11	
8:00am-11:25am	**Technical Presentations in Session** *System Integration* *Miniaturization of Bio-Devices* *Emerging Packaging Technologies* *Heterogeneous & Complex System Packaging* *Polymers in Microelectronics*
11:00am-5:30pm	**Exhibit Hall Open**
11:30am-1:00pm	Lunch in the Exhibit Hall
1:00pm-3:25pm	**Technical Presentations in Session** *Advanced CMOS Nodes* *Power, Batteries and Energy Harvesting* *LTCC and Ceramic Technologies* *Wire Bonding* *Novel Materials/Processes II*
3:30pm-5:30pm	**Happy Hour in Exhibits**
5:30pm-7:30pm	**International Panel Session and Wine Reception**

Thursday, October 12	
8:00am-11:10am	**Technical Presentations in Session** *Process Integration* *Extreme Environment Device Reliability* *Fanout Wafer Level Packaging* *Antennas and Advanced RF System Integration* *Reliability*
11:15am-12:55pm	**Posters and Pizza Session**
1:00pm-2:55pm	**Technical Presentations in Session** *Materials and Reliability II* *Assuring Device Security – Network and Microelectronic Solutions* *Embedded Packaging* *Panel/Board Level System Integration* *Additive Manufacturing*
3:15pm-4:00pm	**Chapter Leadership Meeting**

From the General Chair

Hello IMAPS Members!

I'm looking forward to seeing you at ***the best ever International Symposium on Microelectronics*** in Raleigh, North Carolina this October 9th – 12th. This is a significant historical year for IMAPS with this as the **50th annual Symposium** and it's been a pleasure to be serving as your General Chair. Raleigh is the perfect location for the 50th International Symposium since it serves as the IMAPS international headquarters and a great innovation hub for the microelectronics industry.

I've been honored to work with a great group of committee chairs and the IMAPS staff to put together an exceptional program "**Celebrating our 1st 50 years and preparing for the next 50 years of microelectronics.**" Our industry has been part of driving new innovations in chip-package interactions, wafer level packaging, and additive manufacturing to reality and you'll see a strong emphasis on those topics reflected in this year's technical program as well as traditional cornerstones of advanced packaging, materials, processes and reliability. This year's Technical Chair, Dr. Mary Cristina Ruales Ortega, has led her Technical Committee in putting together the strongest and best organized Technical Program ever with **more than 150 technical presentations and posters** on today's most relevant topics in 5 parallel technical tracks. The program is available earlier than ever too, so you have more time to plan out your time at the Symposium.

We're continuing with changes in the Symposium structure implemented in 2015 and 2016 that include a strong Plenary Session with 4 keynote speakers in technical and Global Business topics, the popular Posters and Pizza session which continues to grow each year, and expanded opportunities for networking and time on the exhibit floor visiting our more than 120 great exhibitors. As part of our commitment to continuous improvement, there are new events and opportunities such as a fun and technically focused Panel Discussion highlighting the international nature of IMAPS and the microelectronics community looking at 21st century microelectronics packaging needs. NAGASE will be sponsoring this great International Panel Discussion by providing a Wine Happy Hour in conjunction with it.

You'll have the ability to enhance your technical skills through one of the 16 Professional Development Courses offered on October 9th. Also preceding the kickoff of the Technical Program will be the annual David C. Virissimo Memorial Golf Classic that directly benefits the future professionals of IMAPS with proceeds going to the Microelectronics Foundation that funds student involvement and awards. Speaking of students, IMAPS continues to provide opportunities for university students to showcase their research and win valuable prize money, including travel grants for qualifying students. The IMAPS outreach to local high school students will include a tour of the exhibit hall floor. Please look for the students and engage them about the opportunities within our community. Last year I was able to spend time with a local high school robotics team, Clockwork Orange, and see their enthusiasm for Science, Technology, Engineering, and Math (STEM) future careers and answer some of their questions about how to be successful in such a career.

There will also be time to celebrate our rich heritage through special events highlighting the first 50 years of IMAPS. This will be a great opportunity for newer and earlier career attendees to learn about who and what got us to where we are and will be a fun time for others to reminisce about the impact of IMAPS on their careers and lives and also their impact on IMAPS and the microelectronics industry.

As a personal aside, I never could have guessed how much of a positive impact my participation in IMAPS (as a presenter and session chair at the first event I attended in 2005) would have on my life. That first event for me was the 1st International Conference on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT). Since then, my involvement has continued and increased to include more speaking and session chairing, technical chair, and general chair roles within CICMT, and now General Chair for IMAPS' showcase event – the International Symposium on Microelectronics. My involvement has contributed to my career advancement, meeting new collaborators, growing friendships, and, most significantly, meeting my wife.

This is an exciting time to be part of the microelectronics, assembly, and packaging supply chain as our industry becomes more and more international, connected, and integrated. Connectivity is changing our personal and industrial worlds and that is driving new and changing challenges and opportunities for the IMAPS community to be part of.

Thanks to all of you and to the Symposium Committee for making the 50th Annual Symposium on Microelectronics the best ever! It's been an honor and pleasure to work with my team to organize the symposium and I'm excited to see all of you in Raleigh, North Carolina.

Please keep sending your feedback and ideas for incorporation into this or future symposia and look for updates on the IMAPS website at www.imaps2017.org. Make sure you download the IMAPS app so you have the latest information during the symposium.

Mark your calendar now for October 9th through 12th and see you in Raleigh.

Dan Krueger
Honeywell
General Chair, IMAPS 2017

From the Technical Chair

Dear IMAPS Members!

I'm really excited for the ***50th International Symposium on Microelectronics*** in October in Raleigh, North Carolina. I've had the honor to work with a wonderful technical team and we have prepared a strong technical program. The 50th International Symposium will open the Plenary Session with dynamic keynote speakers from important and diverse companies in the microelectronics community. We will have 5 parallel technical tracks:

- Chip Packaging Interactions (CPI)
- High Performance, Reliability, and Security
- Advanced Packaging and Enabling Technologies
- Advanced Packaging and System Integration
- Advanced Materials and Processes

The Coffee Breaks, Posters and Pizza session, as well as different receptions and lunch breaks are wonderful opportunities to network and share with colleagues and friends. The exhibits are also a great way to see new products and technologies in the industry. In addition, to celebrate the 50th anniversary of the society we will have an International Panel Session to discuss the vision for microelectronics packaging in the future.

Thanks to all of you and especially to the Technical Committee for your great work. The 50th Annual Symposium on Microelectronics is going to be the best ever! Your feedback is very important for us. Please keep sending your comments and ideas for the annual symposium. Remember to look for updates on the IMAPS website at www.imaps2017.org.

I'm looking forward to seeing all of you in October in Raleigh, North Carolina. Don't forget to mark your calendar October 9th through 12th and see you in Raleigh!

Mary Cristina Ruales Ortega
University of Missouri, Kansas City
Technical Chair, IMAPS 2017

IMAPS 50th International Symposium on Microelectronics
Raleigh, North Carolina USA • October 9-12, 2017

The Largest Conference Program for Microelectronics, Assembly, Reliability, Emerging Applications, Materials and Advanced Packaging in the Fall of 2017

This year's attendees will find an IMAPS 2017 program with technical sessions balancing between emerging, new and mature topics, and a large cross-section of vendors exhibiting their products and technologies in the exhibition hall.

The IMAPS committees and many dedicated volunteers have prepared the 2017 Symposium with an emphasis on exciting topics that are relevant within the microelectronics community with session topics on fan-out wafer level packaging; embedded packaging; heterogeneous & complex system packaging; advanced CMOS nodes; miniaturization of bio-devices; 3D technologies; wire bonding; additive manufacturing; materials; and much more.

Complementing the technical sessions, multiple Professional Development Courses (PDCs) are on tap with a variety of topics bound to enhance and broaden your technical portfolio.

The IMAPS exhibition returns featuring a 2-day show floor with more than 120 exhibit booths, featuring companies and research labs that will showcase a vast array of new products serving all segments of the microelectronics industry, including Consumer, Healthcare and Biomedical, Military, Aerospace, Computing, and Automotive/Industrial. Browsing the exhibit hall and talking to the exhibitors are bound to be exciting and we hope that this enables you to learn the latest and greatest solutions to the changing needs in your business and research.

Next stop: RALEIGH!

Keynote Speakers

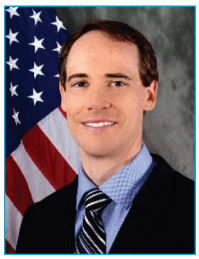
Title Coming Soon!

Roawen Chen,
Senior Vice President
of Global Operations,
Qualcomm

Dr. Roawen Chen

Electronics Outside the Box: Building a Manufacturing Ecosystem for Flexible Hybrid Electronics

Benjamin Leever, Senior Materials Engineer, Air Force Research Laboratory (AFRL) Soft Matter Materials Branch



Benjamin Leever

Packaging without the Package - A More Holistic Moore's Law

Subramanian S. Iyer (Subu), University of California at Los Angeles and Center for Heterogeneous Integration and Performance Scaling (CHIPS)

Subu Iyer, UCLA

Transforming Electronic Interconnect

Tim Olson, Chief Technology Officer, DECA

Tim Olson

Exciting Events to Expect

Welcome Reception

Join us on Monday, October 9th for North Carolina-inspired food and drink, plus bluegrass entertainment from the Sir Walter String Band!

Celebrating Diversity Event

Just prior to the close of the Welcome Reception, join us for a diversity networking event. More details soon!

Pizza and Posters

Our most popular poster event of the year! Enjoy a slice of pizza (or a few) while engaging with authors over poster presentations.

Happy Hour with the Exhibitors

Mingle with our exhibitors and network over Happy Hour in the exhibit hall.

Micross Facility Tour

Register for the Micross Components facility tour and spend lunch learning about this Research Triangle Park facility!

Microelectronics Foundation Golf Classic

Get your golf game on for the Microelectronics Foundation at the Lonnie Poole Golf Course at NC State University.

Celebrating 50 Years of IMAPS

Celebrating the past and looking toward the future IMAPS 2017 will feature an installation of historical exhibits, including photos, hardware, and more.

Have history to submit?

Contact Brianne Lamm at blamm@imaps.org.

Registration

Early Registration and Hotel Reservation Deadline: September 8, 2017

The Conference & Exhibition is being held at the
Raleigh Convention Center, 500 S Salisbury St, Raleigh, NC 27601

Full attendee registrations (not exhibits only) include Opening Ceremonies, IMAPS Annual Business Meeting, IMAPS Awards Ceremony, Keynote Presentations, Welcome Reception, Technical Sessions, GBC Plenary Session, Panel Discussion, Exhibit attendance, Breaks, Exhibit Hall Reception on Wednesday, Exhibit Hall Lunch on Tuesday, one 2017 Proceedings Download (and access via our Mobile APP) and an automatic one-year IMAPS membership renewal for individual and student members in good standing at the time of registration. For an additional fee you can register for a Professional Development Course (PDC), the Golf Tournament, and other activities/purchases. All prices below are subject to change.

Full Symposium cancellations will be refunded (less a $100 processing fee) only if written notice is postmarked on or before Friday, September 8, 2017. No refunds will be issued after that date.

Register with promo code **drone-giveaway** and be entered to win a drone worth $1,000!

Register Online at www.imaps2017.org

Type	Early Fee Through 9/8/2017	Advance/Onsite Fee After 9/8/2017
IMAPS Member	$775	$875
Non-Member	$875	$975
Speaker	$625	$725
Chair	$625	$725
Chapter Officer	$625	$725
Student (IMAPS Member)	$50	$75
Student (Non-Member)	$75	$100
Exhibits Only (LUNCH INCLUDED)	$30	$30
Exhibits Only (NO LUNCH INCLUDED)	Complimentary	Complimentary
Additional Registration Fees		
Short Course / Professional Development Course "PDC" (one 2-hour PDC: Monday – can take up to four total)	$300	$400
Golf (1 Golfer, Monday) – Scramble 9am Start at Lonnie Pool Golf Course NCSU	$125	$125

Hotel Scams Alert!

The only way to book a room in the official IMAPS Housing Block using the reservations information above. IMAPS does not authorize any other hotel service/group to operate on its behalf.

Book your Hotel Registration Today!

Early Registration & Hotel Deadline: **September 8, 2017**

Book your hotel reservation today! We have reserved a block of rooms at the host hotels to accommodate our attendees. The discounted room rates are only available until the hotel deadline listed above, or until the room block sells out (and they often sell out early - before the expire dates). Reservations received after the noted deadline or after the room block has been filled may be subject to significantly higher rates. IMAPS room blocks at most hotels historically sell out ahead of the discount deadline, so we encourage you to make your hotel reservations quickly for the best price and availability.

IMAPS is pleased to partner with the following hotels for IMAPS 2017:

Marriott Raleigh City Center
500 Fayetteville St, Raleigh, NC 27601
Single/Double: $174 + Taxes/Fees

Sheraton Downtown Raleigh
421 S Salisbury St, Raleigh, NC 27601
Single/Double: $189 + Taxes/Fees

Both hotels are considered host hotels for IMAPS 2017 and are located directly across the street from the Raleigh Convention Center (less than one block).

Cal Poly to Launch Online Professional Certificate Program in Packaging

Cal Poly's Packaging Program will soon offer courses and certificates aimed specifically at packaging industry professionals that will feature interactive coursework on the critical subsets of the packaging value proposition in a global context.

Each nine-unit certificate program will take three to six months to complete, although individual courses can be taken.

Courses for the Packaging for Logistics and Supply Chains Certificate will launch in Fall 2017. The program will explore the impact of commoditization of packaging on its value proposition through global distribution, logistics and supply channel operations.

Packaging Value Chain Certificate courses will be offered in Fall 2017 and Winter 2018. Courses will provide an introduction to the value proposition in the global packaging industry, essential codes of practice as well as marketing and sales concepts.

Packaging Program Director and Professor Jay Singh said classes taken through the certificate program are also transferable into Cal Poly's M.S. Packaging Value Chain program, which will launch in the Fall of 2018. The master's program will also be offered exclusively online.

"The dynamic and engaging online curriculum will promote transference of learning to the workplace while providing professionals opportunities to assume leadership roles and advance their careers," he said. Cal Poly also has plans to offer other specialized certificates in packaging design, analytics and marketing for professionals working across the nation and around the world, Singh said.

Applications for both certificate programs are open to those who have completed a bachelor's degree in packaging or a related field from an accredited college or university with a 2.5 GPA. Applications also require a résumé, official transcript of coursework and a statement of purpose. The deadline for applications for the certificate programs are two weeks before the first course begins.

For more information on Cal Poly's packaging certificates and the application process, visit the Orfalea College of Business Graduate Programs website at http://bit.ly/2tbyphU.

INDUSTRY NEWS

Brewer Science Partners with Arkema to Develop High-Chi DSA Materials for Advanced Node Patterning

July 10, 2017 – Rolla, Missouri, USA – Brewer Science Inc. announced from SEMICON West the extension of its partnership with Arkema to develop second-generation directed self-assembly (DSA) materials using high-x (chi) block copolymers. These new materials target advanced-node wafer patterning processes because they enable even smaller feature sizes than first-generation DSA materials. As such, they provide a cost-effective solution to achieving device nodes down to 5nm and beyond, thereby enabling the continuation of Moore's Law.

"There have been very high expectations that DSA would solve all patterning issues," said Darron Jurajda, Business Unit Manager, Brewer Science Inc. "Like all worthwhile technologies, there are many challenges to be solved before going into production. Leveraging our earlier DSA collaboration with Arkema offers the best path for implementing the next generation of materials. Together, we look forward to unlocking DSA's full potential in accordance with industry timelines for manufacturing."

High-chi block copolymers will further extend DSA's advantages, achieving feature sizes that meet the requirements for 5nm and beyond. Extending their partnership allows these companies to build on their knowledge base, giving them a head start on developing high-chi materials.

As feature sizes shrink more aggressively with each node, it has become cost prohibitive to create them using existing patterning processes, such as EUV, self-aligned double patterning and self-aligned quad patterning. This presents a challenge for foundries and integrated device manufacturers preparing to ramp to 7nm and 5nm processes. DSA provides an alternative solution to achieving fine feature patterning, can be explored for minimal investment, and is cost efficient in final production. Development of high-chi materials also expands the opportunity for implementing DSA in other applications, including photonics, membrane applications and other areas of microelectronics.

The original collaboration between the two companies combined Brewer Science's know-how in patterning and process integration with Arkema's leading-edge expertise in block copolymer development to develop polystyrene-polymethyl methacrylate DSA materials, which are now production-ready to manufacture sub-22nm features.

Contact:
Eric Lawson, Tel: (US) +1.480.276.9572
email: elawson@kiterocket.com

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Helping engineers meet specific requirements

Understanding Optical Transmission Properties of Adhesives

Optical transmission is the ability for light to be channeled through a material, and it is measured from 0 to 100% on a wavelength scale of approximately 200 to 3,100 nanometers (nm). This property is essential for a number of applications in the optical and electro-optical industries. Most optically clear epoxies, polysulfides, and silicones offer excellent light transmission across the visible and near IR ranges, with select systems providing high transmission in the UV and in the middle IR wavelength ranges. This article explains optical transmission and provides specific examples of products that excel in this area.

Read more at https://www.masterbond.com/articles/optical-transmission-properties-adhesives?utm_source=opticaltransmission&utm_medium=email&utm_content=opticaltransmission&utm_campaign=cart

EP30: Low Viscosity, Optically Clear Two Part System

Featuring superb strength characteristics, EP30 bonds well to a variety of substrates including metals, glass, ceramics, many plastics and rubber materials. This highly dimensionally stable system has very low shrinkage after cure, less than 0.003 in./in. Its low viscosity enables this system to be used for bonding surfaces with tight clearances. The product features outstanding chemical resistance, hardness and superb optical clarity.

For more information, request a technical data sheet on EP30.

MasterSil 151: Optically Clear, Water Resistant, Addition Cured Silicone System

For potting applications where low exotherm and high flexibility are required, MasterSil 151 is an ideal candidate. Featuring outstanding electrical insulation properties and a low viscosity, MasterSil 151 also provides superior resistance to vibration and shock. This high strength compound has an elongation of 120-150% and very low shrinkage upon cure. Serviceable over the wide temperature range of -65°F to +400°F, MasterSil 151 also offers convenient handling. It has the ability to cure at room temperature or faster at elevated temperatures. Specialty uses include encapsulating LEDs, optical fiber cladding and potting connectors.

For more information, request a technical data sheet on MasterSil 151.

INDUSTRY NEWS

MB600: One Part Sodium Silicate System Resists High Temperature

MB600 is an aqueous based sodium silicate system for bonding and coating. This one component low viscosity adhesive is capable of withstanding temperatures up to 1,500°F. It is optically clear and has very special light transmission properties, particularly in the range of 200-350 nm. MB600 is a competent electrical insulator, offers rigidity, excellent dimensional stability and provides a barrier to moisture.

For more information, request a technical data sheet on MB600.

UV15: Exceptionally High Glass Transition Temperature

Cationic curing systems, such as UV15, tend to have much higher temperature resistance than other UV type systems. Its glass transition temperature (Tg) with a straight UV cure is 90-95°C, and when post cured for 30 minutes at 125°C, the Tg is 125-130°C. This post cure also enhances UV15's chemical resistance. The halogen free adhesive meets IEC 61249-2-21 standard and has a service temperature range of -80°F to +350°F. It also withstands 1,000 hours at 85°C/85% RH.

For more information, request a technical data sheet on UV15.

Master Bond
Website:www.masterbond.com
Email:newsletters@masterbond.com
Phone:+1 201 343 8983

TechSearch International Analysis Examines FO-WLP Developments and Sensor Packaging Trends

July 19, 2017 – Mobile devices, specifically smartphones, represent the single greatest volume driver for MEMS and other sensors today. Sensors found in these products include electronic compasses, motion sensors, barometers, microphones, and fingerprint sensors. Package types include land grid arrays (LGAs), leadframe packages such QFNs, and wafer level packages (WLPs). Apple is expected to account for 28 percent of the total smartphone sensor market as a result of increased sensor adoption. With the trend toward smart factories, industrial applications are also expected to account for increased sensor demand.

New FO-WLP versions are targeting high-performance applications including networking, data centers, and artificial intelligence. Fan-out on substrate versions such as ASE's Fan-Out Chip-on-Substrate (FOCoS), TSMC's InFO, and Amkor's Silicon Wafer Integrated Fan-out Technology (SWIFT™) are being considered as a low-cost heterogeneous integration alternative to silicon interposers. FO-WLP on substrate fills the interconnect gap between lower-density FO-WLP and the highest density silicon interposers.

The analysis is provided in the latest Advanced Packaging Update, an 84-page report with full references and an accompanying set of 46 PowerPoint slides. The report also provides results from TechSearch International's annual survey on substrate design rules. The design rules include body size, core thickness, via and pad diameter, minimum bump pitch supported, and substrate finish.

TechSearch International, Inc., founded in 1987, is a market research leader specializing in technology trends in microelectronics packaging and assembly. Multi- and single-client services encompass technology licensing, strategic planning, and market and technology analysis. TechSearch International professionals have an extensive network of more than 18,000 contacts in North America, Asia, and Europe.

For more information, contact
Jan Vardaman
TechSearch at tel: 512-372-8887
or visit www.techsearchinc.com.
Follow us on twitter @Jan_TechSearch

Chesapeake Chapter and UMD Student Chapter

UMD Student Chapter and Chesapeake Chapter members at the symposium.

The IMAPS Chesapeake Chapter held its annual Summer Technical Symposium on June 8th, 2017, at the Applied Physics Laboratory (APL) of Johns Hopkins University. The symposium focused on the reliability issues and emerging trends in multilayer packages and simulation techniques. This symposium was also jointly organized by the IMAPS University of Maryland (UMD) Student Chapter.

The evening began with a technical presentation by Dr. Daniel Hines from the Laboratory for Physical Sciences at the University of Maryland. Dr. Hines presented on recent work and advancements in additive manufacturing of microelectronic devices.

Next, the student poster competition was held. Thirteen different student posters were entered into the competition with a summary of each of the poster topics and presenters provided below.

Dr. Daniel Hines from the Laboratory for Physical Sciences at the University of Maryland.

Presenter	Topic	University/Organization
Nripendra Patel	Reliability Testing of Ceramic Anodes of Solid Oxide Fuel Cells through Design and Analysis of Experiments	University of Maryland
Junfu Li	A Parameter Estimation Method for Electrochemical Model for Li-ion Batteries	Harbin Institute of Technology
Yi Wu	Ultrasonic Sensing Approach for Lithium-ion Battery Failure Detection	Nanjing University of Aeronautics and Astronautics
Lingxi Kong	Lithium Battery Internal Shorts due to Dendrite Formation	University of Maryland
Jonathan Kordell	Fiber Optic Conjugate Stress Sensors for Prognostic Health Monitoring of Structures	University of Maryland
Yongzhi Zhang	Remaining Available Energy Prediction of Lithium-ion Batteries	Beijing Institute of Technology
Jordan Jameson	Thermo-mechanical Degradation of Polyimide Insulation and its Effect on Electromagnetic Coil Impedance	University of Maryland
Subramani Manoharan	Decapsulation of Copper Wire Bonded Devices	University of Maryland
Guru Prasad Pandian	Assessing the Long-term Reliability of Electronic Assemblies Under Laboratory Storage and Usage Conditions	University of Maryland
Hao Huang	Mechanical Behavior of Assemblies Bonded with Pressure-Sensitive Adhesives	University of Maryland
Edmond Elburn	Analysis of Thermal Uprating Capabilities and Component Temperature Ratings For Semiconductor Devices	University of Maryland
Jennifa Li	Shelf Life Evaluation Method of Electronic Components	University of Maryland
Michael Rego	Power Packaging Thermal and Stress Model for Quick Parametric Analysis	U.S. Army Research Laboratory

Student Poster Competition at the IMAPS Summer Symposium 2017.

The judging for the competition was completed on the basis of five topics: clarity of work, creativity of research, merit of research, presentation skills, and overall depth of knowledge. There were five judges that viewed each of the presentations and determined the winners of the competition: Dr. Lauren Boteler, Dr. Erica Folk, Dr. Will McKinzie, Dr. Bruce Romenesko, and Dr. Daniel Hines. The winner of the event and the top prize of $200 was Jonathan Kordell, who presented on fiber optic stress sensors for structural prognostic health management. Finishing in second place and winning $150 was Subramani Manoharan, who presented on the decapsulation of copper wire bonded devices. Finishing in third place and winning $100 was Jordan Jameson, who presented on the thermo-mechanical degradation of polyimide insulation and its effect on electromagnetic coil impedance.

Jonathan Kordell, winner of the Student Poster Competition, receiving his certificate from Dr. Lauren Boteler.

Subramani Manoharan, second place finisher, receiving his certificate from Dr. Lauren Boteler.

Jordan Jameson, third place finisher, receiving his certificate from Dr. Lauren Boteler.

The second talk was by Anto Peter from the Center for Advanced Life Cycle Engineering at the University of Maryland. Mr. Peter presented on the opportunities and challenges associated with using conductive polymers in electronics. The proceedings for the day concluded with a dinner, giving the members of the chapter, speakers, and guests an opportunity to interact with each other.

Speakers and Abstracts

Presentation Title:

Additive Manufacturing Methods and the Fabrication of Printed Hybrid Electronic Circuits.

Abstract:

3D printing is an emerging manufacturing method which allows for the design and fabrication of complex structures not otherwise achievable using standard (subtractive) manufacturing methods. In the past, additive manufacturing methods have been utilized primarily in the area of structural prototyping, for example, in automotive and aviation industries. Further advances in AM are bringing the fabrication of electronics into the realm of 3D printing. For example, advanced electronics would provide an alternative to the ubiquitous Cu/FR4 flat, rigid printed circuit boards (PCBs) generally found in present-day computers and other electronics devices and fabricate the electronics into a part itself. Examples of such advanced electronics would be a smart electronic bandage for the health care industry or an impact sensor and/or communication electronics built into the shell of a sports helmet. Several examples of employing additive manufacturing methods for the fabrication of advanced electronics circuits will be presented during this talk.

About the Speaker:

Dr. Daniel Hines obtained an MS in Physics from Michigan State University and a Ph.D. from the University of Maryland. Prior to coming to the Laboratory for Physical Sciences (LPS) in 2003, he worked at Schumberger's research center in Ridgefield, CT and at the NEC Research Institute (NECI) in Princeton, NJ. At LPS, he initially developed transfer printing techniques used to fabricate high quality organic and carbon-based thin-film transistors on plastic substrates. Since 2012, he has been developing additive manufacturing methods for the fabrication of printed hybrid electronics.

Presentation Title:

Conductive Polymers in Electronics - Opportunities and Challenges.

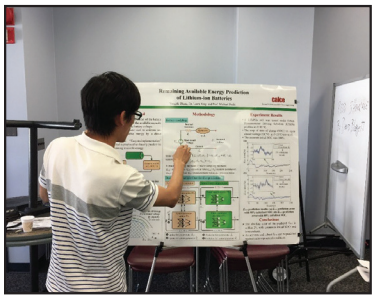
Abstract:

Conductive polymers are organic polymers that have conductivities in the range of semiconductors and metals. Intrinsically conductive polymers typically feature conjugated systems with delocalized π-electrons. While they were discovered in the 1970s, it was not until recently (since 2000) that they began to be used widely in commercial electronics applications. Unlike most materials used in electronics, conductive polymers can be processed quite easily, and often at significantly lower temperatures. These materials can also be engineered to have the necessary properties required for the specific needs of their applications. Conductive polymers can also be made transparent, biocompatible, biodegradable and porous. One particular conductive polymer — polyethylene dioxythiophene (PEDOT) — is being used extensively in organic (OLED) displays, conductive textiles and fabrics, solar cells, supercapacitors, lithium batteries and electrolytic capacitors. While PEDOT offers better reliability and performance than conventionally used liquid electrolytic systems, it remains vulnerable to degradation at higher temperatures and humidity levels. Advances being made in the processing of PEDOT and in the way we package electronic components might help mitigate some of these issues.

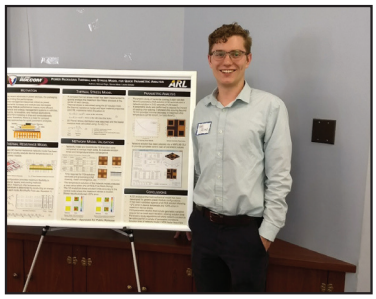
About the Speaker:

Anto Peter is a PhD candidate at the Center for Advanced Life Cycle Engineering at the University of Maryland, College Park. He graduated from the National Institute of Technology, Trichy with a bachelor's degree in mechanical engineering, and received his master's in mechanical engineering from the University of Maryland. His research focuses on physics of failure modeling of passive electronic components. He has also worked with the National Academy of Sciences on investigating reliability prediction and reliability growth in defense electronics systems. His other research interests include rapid screening and assessment techniques for supplier selection, new materials for energy storage and impact of harsh environments on electronics reliability. Anto has also served as the president of the IMAPS UMD student chapter since 2014.

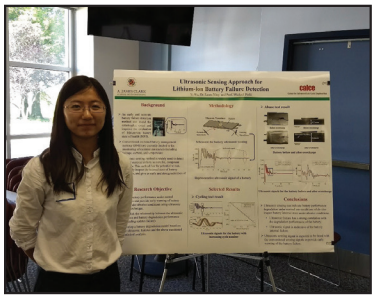
Poster Competition Additional Images:



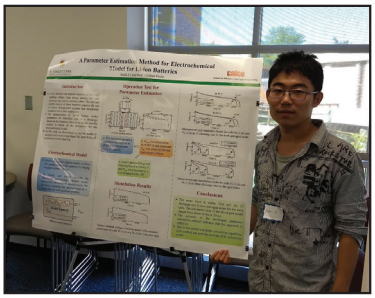
Yongzhi Zhang, a visiting researcher from Beijing Institute of Technology, presenting his work on predicting remaining energy levels of lithium-ion batteries.



Michael Rego, from the U.S. Army Research Laboratory, presenting his work on the development of a power packaging thermal and stress model for quick parametric analysis.



Yi Wu, from Nanjing University of Aeronautics and Astronautics. presenting her work on the ultrasonic sensing approaches for lithium-ion battery failure detection.



Junfu Li, from Harbin Institute of Technology, presenting his work on a parameter estimation method for electrochemical model related to Li-ion batteries.

Guru Pandian presenting his work on the long term reliability of electronic assemblies for the judges.

Submitted by Edmond Elburn

International Microelectronics Assembly and Packaging Society (IMAPS)
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Call for Abstracts

2017 Topical Workshop and Tabletop Exhibition on

Thermal Management

Toll House Hotel, Los Gatos, CA, USA
November 7-9, 2017

Additional Information: www.imaps.org/thermal

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Dave Saums
DS&A LLC
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(978) 499-4990

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Futurewei Technologies
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(408) 330-5352

ENGINEERING AND SCIENCE UNIVERSITY STUDENT ABSTRACT AND STIPEND COMPETITION
See details on following page. Open to undergraduate and graduate students, globally.

Since 1992, this Workshop has been organized annually by IMAPS to specifically address current market needs and corresponding technical developments for electronics thermal management. Presentations on leading-edge developments in thermal management components, materials, and systems solutions for effectively dissipating heat from microelectronic devices and systems are sought from industry and academia. The Workshop emphasizes practical, high-performance solutions that target current and evolving requirements in mobile, computing, telecom, power electronics, military, and aerospace systems. Single-company product development concepts are acceptable subjects; however, all abstracts will be judged on their novelty and innovative contributions to the industry knowledge.

Speakers are expected to attend the entire Workshop to encourage greater interaction between registered attendees. Every year, authors and attendees find this IMAPS Workshop format to be an effective forum for networking between all participants. The reduced registration fee for speakers makes active participation in the program even more beneficial. Activities beyond the technical program, including meals, breaks, and exhibit hours, are focused on maximizing networking effectiveness. Attendees typically view individual discussions during this event to be a critical aspect of attendance and participation – to a much greater extent than in a typical technical conference.

TOPICS ARE EXPECTED IN THE FOLLOWING AREAS

- **Market Drivers:** Understanding thermal challenges and business / economic drivers that influence change in electronic systems design and manufacturing – and how these impact thermal design requirements. Developing market trends, market segmentation, cost drivers and reliability factors are examples of topics that set the framework for where and what types of new technical solutions are viable.
- **Multi-Die Packaging:** Advanced packaging technologies, such as System-in-Package, Multi-Chip Module and Multi-Package Module, stacked-die, etc. provide significant opportunities for miniaturization and performance enhancements. These technologies also can introduce significant thermal and interconnect challenges that must be balanced against those benefits.
- **Mobile and Handheld Devices and the Internet-of-Things (IoT):** Wearables, mobile and medical devices, small displays, tablets and notebooks are increasingly critical for our interconnected world. These devices often introduce unique component- and system-level thermal management challenges that require novel design approaches and materials.
- **Wireless and Telecom Infrastructure:** High performance telecom hardware have challenging component and system level requirements that require technical advances to meet the evolving needs for routers, networked systems, base stations, etc.
- **Power Semiconductor Thermal Components, Systems, and Solutions:** Developments in IGBT thermal management and packaging strongly influence advances in electronic and electrical drive systems. These advances are increasingly important in the Electric Vehicle/Hybrid Electric Vehicle and renewable energy markets.
- **Mil/Aerospace:** Emerging military and aerospace systems, including avionics, RF, and microwave components and modules for phased array radar, countermeasures, and other systems, require advanced thermal management as well as high-temperature materials and packaging.
- **System-Level Cooling:** The thermal design of complex systems, such as high-performance computing systems, relies on extensive component- and system-level thermal management analysis to address the broad spectrum of issues that entail a comprehensive system design.

Thermal Management...continued

- **Data Center Cooling:** Data center cooling includes a variety of design optimization activities including cooling provisioning, airflow control, temperature distribution and migration paths that range from forced air convection to system liquid cooling.
- **Liquid Cooling, Phase-Change, and Refrigeration:** Advanced cooling methods that use liquid, latent heat and/or active cooling provide opportunities for enhanced performance and design flexibility. Effective designs must balance these advantages against factors including life-cycle cost, reliability and serviceability impact.
- **Thermal Interface Materials (TIMs) and Testing:** Advanced thermal interface materials that may include organic, metallic, graphitic materials in bulk form as well as nanoscale are enabling significant advances in the thermal management of high-performance processors, memory, telecom, IGBT, RF, and microwave components and systems. Effective testing and reliability methods and standards are critical in determining the suitability of a TIM for a given application.
- **CTE-Matching and High Thermal Conductivity Materials:** Metallic, ceramic and composite materials have been engineered to exhibit excellent thermal conductivity with controlled coefficient of thermal expansion (CTE) properties to allow for better matching with GaN, SiC, silicon or ceramic materials to reduce thermal stresses in component packaging.

Announcement:
Engineering and Science University Student Abstract Competition

The IMAPS ATW Thermal has included a competition for engineering and science university student abstracts each year since 2004. This portion of the program has been very well received by Workshop attendees and a number of past winners have returned to participate in the Workshop program again. This competition is open to both undergraduate and graduate engineering and science students. Stipends are provided to each winning author (one stipend per winning presentation, even when there are multiple co-authors).

Student Stipends are sponsored by the Microelectronics Foundation

The Microelectronics Foundation sponsors Student Paper Competitions in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Authors must be currently enrolled in either an undergraduate or graduate program and must mark the checkbox indicating their student status on the abstract submission form. Only those abstracts marked as being submitted as student abstracts will be considered for this competition. The organizing committee will evaluate student abstracts submitted and award a stipend for each of a minimum of two winning abstracts. The stipend amount has varied each year but has always been a minimum of $600 per award. The winning authors are required to attend the event and present the winning presentations in order to receive the stipend award. One award is made per abstract, to the presenting lead speaker.

Tabletop Exhibits

A MAXIMUM of 11 tabletop exhibits are planned for this event, for electronics thermal management services, materials, software and characterization tools, and components. ***Book early; tabletop spaces sell out each year.***

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MOST VIEWED CONTENT FROM IMAPS CONFERENCES AND SYMPOSIA

Factors influencing microstructural evolution in nanoparticle sintered Ag die attach
S.A. Paknejad, A. Mansourian, Y. Noh, K. Khtatba, L. Van Parijs, S.H. Mannan
2015 High Temperature Electronics Network

Copper Migration in Flip-Chip Substrates Under Biased-HAST Conditions
Matthew E. Stahley, John W. Osenbach
2016 International Conference on Device Packaging

Advanced wire bonding for high reliability and high temperature applications
M. Guyenot, M. Reinold, Y. Maniar, M. Rittner
2016 International Symposium on Microelectronics

MOST VIEWED ARTICLES

Download these most popular Journal of Microelectronics and Electronic Packaging articles of May and June 2017

Electrical Performance of a 32-I/O HTCC Alumina Package for High-Temperature Microelectronics
Liang-Yu Chen, Philip G. Neudeck, David J. Spry, Glenn M. Beheim, Gary W. Hunter
Vol. 14, No. 1, January 2017

Temporary Wafer Bonding Materials with Mechanical and Laser Debonding Technologies for Semiconductor Device Processing
Xiao Liu, Qi Wu, Dongshun Bai, Trevor Stanley, Alvin Lee, Jay Su, Baron Huang
Vol. 14, No. 1, January 2017

Proposal of Ultrafine and High Reliable Trench Wiring Process for Organic Interposer
Kazuyuki Mitsukura, Masaya Toba, Kousuke Urashima, Yoshinori Ejiri, Kenichi Iwashita, Tomonori Minegishi, Kazuhiko Kurafuchi

TOP SEARCH TERMS

The most popular search terms throughout IMAPSource publications

1. GBC
2. High Temperature
3. Wire / 3D / Bonding

Announcement and Call for Abstracts

International Conference and Exhibition on

High Temperature Electronics (HiTEC)

www.imaps.org/hitec

May 8-10, 2018

Hotel Albuquerque
Albuquerque, New Mexico USA

Abstract Deadline: January 22, 2018

Overview: HiTEC 2018 continues the tradition of providing the leading biennial conference dedicated to the advancement and dissemination of knowledge of the high temperature electronics industry. Under the organizational sponsorship of the International Microelectronics Assembly and Packaging Society, HiTEC 2018 will be the forum for presenting leading high temperature electronics research results and application requirements. It will also be an opportunity to network with colleagues from around the world working to advance high temperature electronics.

Abstracts being requested include the following topics:

- **Applications:**
  - Geothermal
  - Oil well logging
  - Automotive
  - Military/aerospace
  - Space
- **Device Technologies:**
  - Si, SOI
  - SiC
  - Diamond
  - GaN
  - GaAs
  - Contacts
  - Dielectrics
- **MEMS and Sensors:**
  - Vibration
  - Pressure
  - Seismic
- **Packaging:**
  - Materials
  - Processing
  - Solders/brazes
  - PC boards
  - Wire bonding
  - Flip chip
  - Insulation
  - Thermal management
- **Circuits:**
  - Analog
  - Digital
  - Power
  - Wireless
  - Optical
- **Energy Sources:**
  - Batteries
  - Nuclear
  - Fuel cells
- **Passives:**
  - Resistors
  - Inductors
  - Capacitors
  - Oscillators
  - Connectors
- **Reliability:**
  - Failure mechanisms
  - Experimental and modeling results

Those wishing to present a paper at the HiTEC Conference must submit a 300-500 word abstract electronically no later January 22, 2018, using the online submission form at: www.imaps.org/abstracts.htm. A Final Manuscript of 6-8 pages, two-column format is due March 21, 2018, for all accepted abstracts. Please contact Brian Schieman by email at bschieman@imaps.org or by phone at 412-345-3328 if you have questions. A Proceedings DOWNLOAD containing the conference papers will be distributed to all attendees during the Conference. Speakers are required to pay a reduced registration fee.

Student Competition sponsored by the Microelectronics Foundation:

MICROELECTRONICS FOUNDATION
Making Connections. Awarding Innovation.

The Microelectronics Foundation sponsors ***Student Paper Competitions*** in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Students submitting their work and identifying that "Yes, I'm a full-time student" on the abstract submission form, will automatically be considered for these competitions. The review committee will evaluate all student papers/posters and award a total of $1,000 in awards checks at the ATW/Conference. The selected student(s) must attend the event to present his or her work and receive the award. For more information on the student competition, go to www.microelectronicsfoundation.org.

International Microelectronics Assembly and Packaging Society

www.IMAPS.org

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- Speaking and publishing opportunities

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- Participate in discussions through the Memberfuse Community website
- Maintain your professional listing

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In 2017, free downloads will be subject to membership level below. Non-member downloads will be subject to a per-article charge.

2017 IMAPSource Membership Plans:	Number of downloads
Individual/Senior/Lifetime	100
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Associate Corporate	50
Affiliate (International Chapters/Unemployed Members)	50
Student	25
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Press releases in Corporate Bulletin	Up to 1 press release per bulletin (twice monthly)	Up to 1 press release per bulletin (twice monthly)
Member pricing for exhibitor events	Included	Included
JOBS Marketplace	Complimentary job postings	Complimentary job postings
Use of membership mailing list	3x per year	1x per year
IMAPS.org advertising	Complimentary	Member discount
Magazine advertising	One 1/4 page ad incl. annually, plus 15% discount on any additional ad	15% discount
Online Industry Guide	Includes company listing, link to website, product and service categories	Includes company listing, link to website, product and service categories
Global Business Council	Membership included	Membership included
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May-June 2017

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Mini-Systems, Inc.	Craig Tourgee	508-695-0203	ctourgee@mini-systemsinc.com	www.mini-systemsinc.com	back cover

Advancing Microelectronics 2017 Editorial Schedule

Issue	Theme	Copy Deadline	Ad Commitment I/Os Deadline
Nov/Dec	Ceramic: Thick and Thin Film	Sep. 8	Sep. 13

IMAPS HEADQUARTERS

WHO TO CALL

Michael O'Donoghue, Executive Director, (919) 293-5300, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction

Brian Schieman, Director of Programs, (412) 368-1621, bschieman@imaps.org, Development of Society Programs, Website Development, Information Technology, Exhibits, Publications, Sponsorship, Volunteers/Committees

Ann Bell, Managing Editor, *Advancing Microelectronics,* (703) 860-5770, abell@imaps.org, Coordination, Editing, and Placement Management of all pieces of bi-monthly publication, Advertising and Public Relations

Brianne Lamm, Marketing and Events Manager, (980) 299-9873, blamm@imaps.org, Corporate Membership, Membership and Event Marketing, Society Newsletters/Emails, Event Management, Meeting Logistics and Arrangements, Hotel and Vendor Management

Shelby Moirano, Membership Administration, (919) 293-5000, smoirano@imaps.org, Member Relations and Services, Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support

CALENDAR OF EVENTS

	start	end	
2017			
SEPTEMBER	9-13-17	9-14-17	Additive Manufacturing 2017 Huntsville, AL www.imaps.org/additive
OCTOBER	10-9-17	10-12-17	IMAPS 2017 Raleigh, NC www.imaps.org/imaps2017
NOVEMBER	11-7-17	11-9-17	Topical Workshop and Tabletop Exhibit on Thermal Management Los Gatos, California www.imaps.org/thermal
DECEMBER	12-5-17	12-7-17	3D ASIP 2017 - 3D Architectures for Heterogeneous Integration & Packaging San Francisco, CA http://3dasip.org/
2018			
MARCH	3-5-18	3-8-18	Device Packaging 2018 We-Ko-Pa Resort and Casino, Fountain Hills, Arizona www.imaps.org/DevicePackaging
MAY	5-8-18	5-10-18	HiTEC 2018 - High Temperature Electronics Albuquerque, New Mexico www.imaps.org/hitec

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for links to all upcoming events including:

- **full event descriptions**
- **abstract submissions**
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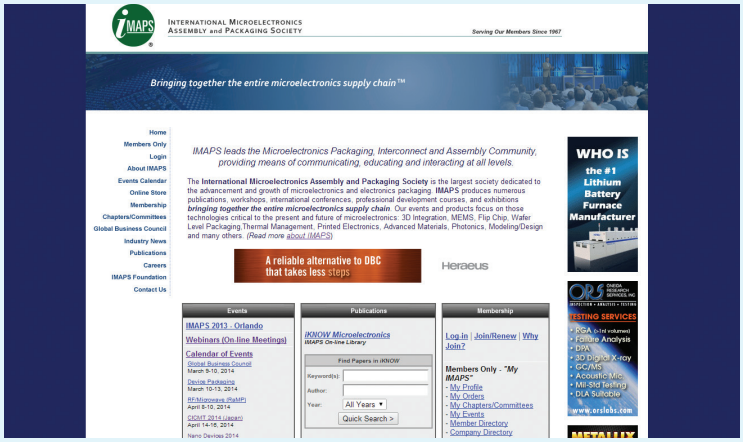
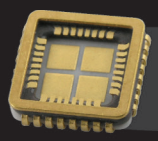
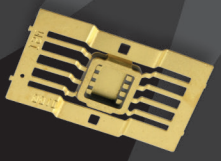
- **event updates**

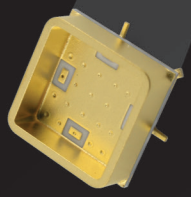


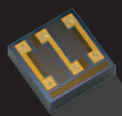
PRECISION PASSIVE COMPONENTS & ELECTRONIC PACKAGES

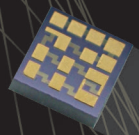
PROVEN RELIABILITY. TRUSTED PERFORMANCE.









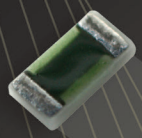


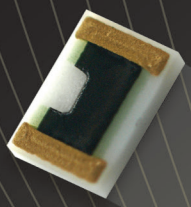
Thick & Thin Film Resistor Products

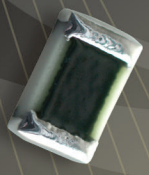
- Faithful scheduled deliveries under 2 weeks
- Values from 0.1 Ohm to 100G Ohm
- Abs. tolerance to ±0.005%, matching to ±0.0025%
- TCR's to ±2ppm/°C, tracking to ±1ppm/°C
- Operating frequencies to 40GHz
- High performance at cryogenic temperatures
- Case sizes to 0101
- Space level QPL's, F.R.-"S", per MIL-PRF-55342
- Zero failures with over 200 million life test hours
- ISO 9001:2000 certified
- Full line of RoHS compliant products
- 24-hour quote turnaround

Electronic Package Products

- Hi Reliability Hermetic Packages:
  - Lightweight glass sidewall flatpacks
  - Metal flatpacks, leadless chip carriers (LCC) and ceramic quad flatpacks (CQFP)
  - Surface mount and plug-in packages
- Hermeticity per MIL-STD-883, Method 1014, Condition A4 (greater than 10^{-9} atm cc/sec)
- Plating per MIL-DTL-45204 and QQ-N-290 for standard packages (unless otherwise specified)
- Custom design available
- RoHS and DFARS compliant







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