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JULY/AUGUST 2017 Vol. 44 No. 4

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IMAPS 2017

October 9-12, 2017 Raleigh Convention Center, Raleigh, NC

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3D ASIP 2017 - 3D Architectures for Heterogeneous Integration & Packaging December 5-7, 2017 San Francisco, CA

March 5-8, 2018

Device Packaging 20188WekoPa Resort and Casino, Fountain Hills, Arizona

HiTEC 2018 - High Temperature Electronics May 8-10, 2018 Albuquerque, New Mexico

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FROM THE GUEST EDITOR



Greg Caswell, Guest Editor



IMAPS at 50

This year IMAPS is 50 years old. I started to think about how important IMAPS (ISHM) was in the growth of the microelectronics industry. The initial symposium in 1967 was called the First Technical Thick-Film Symposium and was created by George Doyle, John Hinchey, Robert Waer, George West and George Anderson. It was attended by 283 engineers and the focus was entirely on advancements in hybrid circuits. The charter members of the society are listed on the IMAPS web site as well as other historical information (see link below).

http://www.imaps.org/leadership/history.htm

In 1984, ISHM pushed ahead with a 2-day symposium and book entitled *Surface Mount Technology*. I had the honor of leading these activities. Sixteen authors wrote chapters and created presentations and from that first book, SMT was created. Since then IMAPS has been a force in leading the industry with respect to the advancement of microelectronics packaging.

Advanced Technology Workshops have helped guide this activity. The first ATW was held on Nantucket Island in 1990 and focused on the new technology called Multi-Chip-Modules. Jack Balde was the technical chair and I was the general chair. This workshop led to the MCM conference in Denver and 8 more ATWs on the topic. Since then over 100 ATWs on numerous technologies have kept IMAPS at the forefront.

We are planning several 50th Anniversary activities for the symposium this fall. We are gathering ISHM/IMAPS history via a Call for History. This can be in the form of hardware, photos, stories, etc. A special input form has been created by Brianne at headquarters for this purpose. The solicitation will come from our society president, Sue Trulli. Please help us with this activity. We will have the hardware on display and a running slide show of the photos and images. Displays are also planned to address each of the 5 decades since the society's inception. My committee consists of Sam Forman, Phil Garrou, Howard Imhof, Tom Terlizzi, Urmi Ray and Sue Trulli. Please provide any thoughts, comments or input on your ideas to any one of us.

At the 50th Anniversary Gala, we plan to invite many folks from around the world who have been influential in the growth and development of our society.

Please join us in celebrating this milestone as we move into the next generation of microelectronics packaging.

See you in Raleigh. Greg Caswell 50th Anniversary Committee







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IMAPS 2017

IMAPS 2016 Best Papers, Student Papers and Best Poster

Best of Track (Advanced Packaging) and Best of Symposium

From Session WA3: Fanout Wafer Level Packaging I

Optimization of Laser Release Layer, Glass Carrier, and Organic Build-up Layer to Enable RDL-first Fan-out Wafer-level Packaging Alvin Lee, Brewer Science, Inc. (Jay Su, Baron Huang, Ram Trichur, Dongshun Bai, Xiao Liu, Brewer Science, Inc.; Leon Tsai, Bor Kai Wang, Aric Shorey, Corning Incorporated; Yu-Min Lin, Tao-Chih Chang, Wen-Wei Shen, Hsiang-Hung Chang, Chia Wei Chiang, Huan-Chun Fu, Yuan-Chang Lee, K. C. Chen, Yu-Lan Lu, Industrial Technology Research Institute)

Best of Track (Advanced Materials) and Best Student Paper

From Session TP4: Materials Solutions for Different Applications

Electrodeposited Copper-graphite Composites for Low-CTE Integrated Thermal Structures Shreya Dwarakanath, Georgia Institute of Technology (Pulugurtha Markondeya Raj, Vanessa Smet, Venky Sundaram, Rao Tummala)

Best of Track (Emerging Applications)

From Session WA1: Medical Applications

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Julianne Grainger, Carlos Segura, Brian Nugent, Philip Parks)

Best of Track (2.5/3D Packaging and Embedded Packaging)

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Best of Track (Modeling, Design, Test and Reliability)

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ptimization of Laser Release Layer, Glass Carrier, and Organic Build-Up Layer to Enable RDL-First Fan-Out Wafer-Level Packaging

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I. Introduction

Forecasts and technology roadmaps from all prestigious conferences have indicated that future electronic appliances will be dominated by mobile, medical, wearable devices and the IoT[1], all of which have several requirements in common: high-speed communication, low power consumption, and multi-function operation. Thus, high I/O density and chip stacking become necessary. To accommodate increasing demand on I/O and chip stacking, 3-D IC stacking supported by through-silicon via (TSV) was first introduced [2], which was mostly adopted by hybrid bandwidth memory (HBM) but was rarely applied to other applications due to its high cost of ownership, risk to IC performance, and complexity of design. Subsequently, a 2.5-D IC packaging scheme was then proposed as the next version, with cost and performance closer to what industry needs [3], in which silicon or glass interposers with through-substrate vias were applied. However, the cost of ownership still could not meet industry's demand.

Hence, several new terms coined by industry leaders to address unresolved issues from 2.5-D/3-D IC packag-

Abstract

With increasing demand for mobile devices to be lighter and thinner and consume less power while operating at high speed and high bandwidth, many equipment suppliers and assembly participants have invested great efforts to achieve fine-line fan-out wafer-level packaging (FOWLP). However, the inherent warp of reconstituted wafers, which can contribute to poor die placement accuracy and/or delamination at the interface of the build-up layer and carrier, remains a major challenge. In this study, the interactions among laser release layer, glass carrier, and build-up layer were evaluated for optimization of redistribution layer (RDL)–first FOWLP as a foundation to move toward fine-line FOWLP.

In this study, a series of experiments incorporating glass carrier, laser release layer, and build-up layers were carried out to determine the optimal setup for RDL-first FOWLP. First, glass carriers (300 mm x 300 mm x 0.7 mm) with coefficients of thermal expansion of 3 and 8 ppm/°C were treated with 150nm laser release layers. After deposition of 0.1 µm of sacrificial material on the glass carrier, 8-µm build-up layers were coated and patterned by lithography to electroplate Cu interconnections with a density of approximately 10% of the surface area. Subsequent to die attachment, molding compound was applied on top to form a 200-µm protective overcoat. The reconstituted wafer was then separated from the glass carrier through a laser ablation process using a 308-nm laser to complete the design of experiments (DOE).

An experiment to study the correlation of glass carrier, laser release layer, build-up layers, and molding compound in RDL-first FOWLP processes is discussed to address full process integration on 300-mm glass substrates. The combination of glass carrier, laser release layer, build-up layer, and molding compound will pave the way for realizing cost-effective RDLfirst FOWLP on panel-size substrates.

Key words

RDL-first, fan-out, laser debonding, and wafer-level packaging

ing were introduced recently, such as embedded waferlevel BGA (eWLB) from Infineon [4], redistributed chip package (RCP) by Freescale [5], integrated fan-out waferlevel packaging by TSMC [6], silicon wafer integrated fan out by Amkor, and fan-out chip-last packaging by ASE [7]. Despite the various advantages claimed for each technology at conferences or in papers, two fundamental fabrication process flows are inherent: chip-first and RDLfirst. More important, it becomes obvious that debonding material and technology are the key enablers to facilitate integration for both process flows.

Chip-first starts with die assembly on an intermediate carrier followed by overmolding and debonding of the molded wafer from the carrier. The redistribution layers and bumps are subsequently applied on the molded wafer. As for the RDL-first approach, the redistribution layers are applied first on an intermediate. Following underfilling material and molding, the carrier is then separated from molded wafer before bump formation.

Because the chip-first approach was reported vigorously in the past few years, this study focuses on the RDL-first approach, which has the advantage of process



Figure 1. Chip-first and RDL-first flows.

simplicity, along with selection of laser release layer and dielectric material. In addition, an RDL-first approach, which allows dies to be placed on redistribution layers to improve yield loss, is an ideal flow for panel-level packaging.

By using the optimal laser release layer, build-up layers, and RDLfirst process flow, cost-effective panel-level packaging can be realized in the future.

II. Experiment

A. Material Properties

The laser release layer is typically designed to easily decompose under laser radiation while still providing high thermal stability for backside processes. In this study, four laser release layers were evaluated to identify material properties that are reliable and applicable for RDL-first FOWLP processes. Generally speaking, the fan-out process includes multiple thermal cycles such as dielectric material curing, metal deposition, and molding compound curing. Thus, the laser release material must have a thermal decomposition (Td) temperature higher than 200°C with the highest possible UV absorption.

One important criterion for a reliable laser release layer is the ability to adhere well to the glass carrier and sacrificial layer applied on top for redistribution layer formation. **Figure 4** shows an illustration of adhesion of a laser release layer to the sacrificial layer and glass carrier. Weak adhesion of the release layer is the root cause of delamination in subsequent backside processes when stress accumulates [8]. To obtain desirable adhesion, performance of the sacrificial layer used along with each of four release layers was evaluated by pull-off adhesion testing, as illustrated in **Figure 5**.

First, a glass carrier was treated with a laser release layer. After thermal curing, a sacrificial layer was then deposited for the subsequent pull-off adhesion test. This process was repeated to collect adhesion data for all four release layers.

The UV laser debonding process in this study is illustrated in **Figure 6**, showing the interface between the glass carrier and the sacrificial layer. A scanned laser beam travels through the glass carrier to reach the laser release layer, usually around 100 to 200 nm thick, to enable rapid decomposition. Whenever the release layer decomposes at the interface, adhesion at the area is minimized to allow the glass carrier to be easily lifted off the surface of the sacrificial layer.

B. Test Vehicle and Experiment Design

To develop an RDL-first WLP process, a test vehicle design was divided into two portions, including a test chip and bottom glass carrier wafer. As shown in **Figure 7**, the test chip size was 9 mm x 9 mm

Release layer	Td (°C)	Туре	Transmittance at 308nm
Α	545	Thermosetting	50%
В	539	Thermosetting	45%
С	<250	Thermosetting	80%
D	<250	Thermosetting	20%

Table 1. Characteristics of Laser Release Layers



Figure 2. Thermo-gravimetric analysis of four release layers.



Figure 3. Transmittance of release layers.



Figure 4. Illustration of adhesion interface.

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Figure 5. Illustration of pull-off test.



Figure 6. Mechanism of laser debonding by UV laser scanning.

with a thinned thickness of 150 μ m. The electroplated copper pillar bumps on the chip were designed as a nearly full-array type, and 3000 I/O pads were within one chip. Copper pillar bumps had a bump size of 2 μ m and were composed of 5 μ m of Cu, 4 μ m of Ni, and 5 μ m of Sn. Bumps were distributed with a bump pitch of 100 μ m.

A 300-mm glass wafer that was 700 µm thick was used as the carrier. An optimum laser release material was chosen from the evaluated results of pull-off test. After coating the chosen laser release layer and sacrificial layer, the corresponding RDL pattern was fabricated onto the bottom glass carrier. As the test chips were stacked on the wafer, test patterns, including daisy chain and Kelvin structure, could be used to evaluate the electrical connectivity. Finally, the full wafer was molded with sheet mold material. Warp issues were also monitored. The experiments were executed to apply different glass wafers with coefficients of thermal expansion (CTEs) of 3 ppm/°C and 8 ppm/°C. The warp was measured after fabricating two layers of RDLs and two layers of passivation and completion of the molding process.

C. Integration Process

The process flow for manufacturing RDL-first fan out is similar to Figure 1. The structure was fabricated on a glass carrier. First, glass carriers (300 mm x 300 mm x 0.7 mm) with CTEs of 3 ppm/°C and 8 ppm/°C were treated with the laser release layers at a spin speed of 2,500 rpm, to achieve a 150-nm film. The release layer was fully cured to survive at high temperature up to 500°C after baking on a bake plate at 300°C for 5 minutes.



Figure 7. Test chip and corresponding RDL pattern on wafer.

After subsequent sacrificial layer deposition, two layers of 3 μ m RDL and 4 μ m passivation were fabricated on the glass carrier to accomplish electrical interconnection. The two layers of RDL and passivation are shown in **Figure 8**.



Figure 8. Optical images of RDL-first FOWLP fabrication: (a) the first RDL and passivation on glass carrier, and (b) the second RDL and passivation on glass carrier.

After wafer-level processing, the test chip was flip-chip bonded onto a wafer with adhesive using a K&S APAMA C2W bonder. Photos of the bonder and bonding process are shown in Figure 8. Sheet-type molding compound was applied in this WLP study. A sheet mold with thickness of 200 µm was laminated on the wafer surface at 130°C for 60 seconds by a Meiki laminator. After lamination, all the wafers were put in a high-temperature oven and postmold curing was performed at 150°C for 8 hours. After curing, all the process evaluation was finished. Three photos of key steps, including wafer-level process, C2W assembly, and molding process, are shown in **Figure 9**.



Figure 9. Images of chip-on-wafer (CoW) bonding: (a) CoW flip-chip bonder, (b) wafer on bonder stage, (c) chips on wafer.

III. Results and Discussion

A. Adhesion Analysis

The results of pull-off adhesion testing for the four release layers were normalized and are summarized in **Table 2**. All four release layers adhere sufficiently to the sacrificial layer needed to protect the passivation and RDL layers. Thus, thermal stability was used as criterion to determine release for following laser debonding evaluation. Both release layers A and B, with Td up to 500°C, were chosen to proceed for further evaluation.

B. Laser Debonding Evaluation

The laser debonding testing was conducted by using a UV laser with a wavelength of 308 nm. During the laser irradiation, the high-energy laser pulses break bonds in the laser-sensitive release layer. Afterward, the laser-sensitive release layer-coated glass carrier is easily lifted off and removed from substrates with zero force. In this case, glass carriers coated with Material A and Material B release-layers were debonded with 200 mJ/cm2 of laser energy and removed successfully from the substrate with zero force.

C. Process Integration (ITRI)

Three warpage situations were measured after two RDL and passivation layers were fabricated, and the molding compound process was performed. Table 1 summarized three warpage values as each step finished. Two types of glass carriers with different CTEs were compared. These results showed that the warpage of the 3-ppm/°C-CTE carrier is comparable with that of the 8-ppm/°C-CTE carrier after second RDL and passivation fabrication. However, the warpage of the 3-ppm/°C-CTE carrier increased rapidly after the molding process and post-mold curing. Figure 12 and Figure 13 show warp measurements of the carriers of both CTE types, 3 ppm/°C and 8 ppm/°C, were 4.5 mm and 0.75 mm, respectively. For this reason, the glass wafer with a CTE of 8 ppm/°C is suitable for further process development. We also checked the interface between the laser release layer and RDL passivation and did not find any delamination or physical warp forming. The laser release layer could hold a stable adhesive strength under warp form.

Finished processes	CTE 3 ppm/°C	CTE 8 ppm/°C
1st RDL and passivation	350 µm	385 <i>µ</i> m
2nd RDL and passivation	485 µm	507 µm
Molding/curing process	4500 µm	750 µm

Table 3. Warpage Measurement Results for Each Process



Figure 10. Images of three key steps of integration process.

Release layer	А	В	С	D
Pull-off adhesion	0.93	0.98	0.94	0.90

Table 2. Summary Table of Pull-Off Adhesion Testing for the Four Release Layers with the Sacrificial Layer



Figure 11. Images of laser debonding results.



Figure 12. Warpage of molded wafer on glass carrier with CTE of 3 ppm/°C.



Figure 13. Warpage of molded wafer on glass carrier with CTE of 8 ppm/°C.

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IV. Conclusion

A 300-mm glass carrier with CTE of 8 ppm/°C was found suitable for RDL-first FOWLP development in terms of better warp performance after the molding process and post-mold curing. As warp could be as large as 4500 µm, although there was no delamination found on release layer B, adhesion from layers underneath to chips in relation to reliability has become an important subject to study in the future.

Acknowledgments

The authors greatly appreciate the support of the ITRI 3-D IC team, SUSS MicroTec, and Corning Incorporated.

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BEST STUDENT PAPER

Iectrodeposited Copper-Graphite Composites for Low-CTE Integrated Thermal Structures

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Abstract

Emerging high-power and high-temperature electronic modules require thick copper structures for power-supply, thermal vias, heat-spreaders, and also as carriers or lead-frames for high-power packages. Such structures should coexist with glass and other low-CTE substrates to meet high-temperature performance, dimensional stability and superior device interconnection reliability with low stresses and warpage. The primary challenge with these packages arises from the coefficient of thermal expansion (CTE) mismatch between the conductors and the substrates. Cu-graphite composites with glass-matched CTE are explored to address this challenge through analytical modeling of properties such as CTE, Young's modulus and thermal conductivity, FEM predictions of glass warpage and stresses, process development to deposit copper-graphite composite films with high graphite loading of 64 vol. %, and warpage measurements using shadow-moiré. Results indicate that Cu-graphite composites can mitigate the warpage and stress issues in high-temperature and high-power packages.

Key words

co-electrodeposition, warpage, low CTE, composites, thermal management, power electronics

I. Introduction

High current associated with high-power devices leads to increased heat dissipation within the package, also hightemperature operation of automotive electronics in harsh environments further aggravates failure mechanisms such as warpage, delamination, cracking and fatigue, reducing the component life [1,2]. Stress management is, therefore, becoming crucial for electronics reliability, especially in devices operating at high power, in harsh environments with continuous operating temperatures of above 150 C.

Glass is a primary candidate substrate for high-temperature and high-power packages while copper is the workhorse conductor for power-supply and heat-spreader to alleviate thermal gradients in these packages. In highdensity and ultra-thin glass packages, these copper structures are the dominating reason for substrate stresses and warpage. Copper is stiffer than polymer dielectrics and has a high CTE of 17 ppm/C, which induces stresses within the package during processing or operation. Advanced composite materials with tailored material properties can enable higher thermal conductivities and lower CTE. Metal matrix composites of aluminum-carbon, copper-carbon fibers, aluminum-silicon carbide have been developed for a wide range of applications requiring thermal management solutions [3,4], through a variety of processes including powder metallurgy and metal-infiltration. Other solutions also involve adding inorganic particles to polymers to reduce the CTE, and increase thermal and electrical conductivity. Therefore, composites are prime materials of interest for low-CTE conductors and heat-spreaders for thermal management. Low-cost manufacturing processes need to be developed to effectively utilize such composites with superior properties.

The CTE of copper can be reduced without compromising thermal conductivity or electrical performance by incorporating fillers such as graphite. Natural graphite is highly anisotropic and has a thermal conductivity ranging from 140-500 W/mK along the axis parallel to the layer planes and 3-10 W/mK perpendicular to the layer planes. Copper-graphite composites combine beneficial properties of high thermal and electrical conductivity of copper and low CTE of graphite. Their anisotropic properties can be used to eliminate local hotspots by functioning as both a heat spreader and thermal isolation layer [5]. Cu-graphite composites have also been developed for thermal cores in a multilayer printed circuit board for GaN RF power amplifier devices [6]. High-performance graphite fibers were fabricated into preforms and infiltrated with Al or Cu alloys. By controlling the fiber shape and composition, the CTE of the composite can be designed to the target value [8].

Coelectrodeposition is an elegant low-cost process to integrate composite structures onto substrates. Composite films with a wide range of particle sizes and distribution can be achieved with electrodeposition. This process is widely explored for a variety of other applications including wear resistant materials, cutting tools with improved toughness, self-lubrication, or other specialty applications. In one such example, solder nanocomposite thermal interface materials (TIMs) have been developed by coplating tin with graphite [7]. The incorporation of particles into metallic coatings is achieved by convection or electrophoretic migration of particles towards the cathodic surface, and mechanical entrapment into the growing metal matrix [8]. Empirical and multi-physics based models that mainly focus on the particle transport towards the cathode are used to understand the co-deposition process [9,10].

This paper explores coelectrodeposition approach to achieve low-CTE Cu-graphite composite conductors for stress and warpage reduction in high-temperature packages. Surfactant concentration, particle concentration and current densities are varied to optimize the co-electrodeposition process. High graphite loading was achieved by varying the plating parameters. Analytical and FEM models are used to quantitatively predict the improvement in properties.

II. Modeling

Analytical models for the CTE, thermal conductivity and Young's modulus are used to predict composite material properties. The modeling incorporates copper and graphite properties compiled in Table 2.

Material	Cu	Graphite
Young's Modulus (GPa)	117	700
Poisson's Ratio	0.33	0.2-0.3
CTE (ppm/oC)	17	2
Bulk Modulus (GPa)	137	700
Shear Modulus (GPa)	48	300
Thermal conductivity (W/mK)	400	140

Table 1 Material Properties

A. Coefficient of Thermal Expansion

Turner's model [15], which considers the mechanical interactions between the particles, Kerner's model [16] and Schapery's model [17], which takes into account the shape and interactions between the particles, are used here to model the CTE. These numerical models along with experimental results from [8] are shown in **Fig. 1**. The experimental values match very closely to the lower bounds of Schapery's model, which indicates that the models present a good approximation to the experimentally calculated CTE. The governing equations for Turner's model is given by Equation (1), Kerner's model by Equation (2) and Schapery's model by Equation (3).

$$\propto_{c} = \frac{(1-0)K_{m} \propto_{m} + 0K_{p} \propto_{p}}{(1-0)K_{m} + 0K_{p}}$$
(1)

$$\propto_c = \propto_m V_m + \propto_p V_p +$$

$$V_{p}V_{m} \left(\propto_{p} - \propto_{m} \right) \frac{\kappa_{p} - \kappa_{m}}{V_{m}\kappa_{m} + V_{p}\kappa_{p} + \left(\frac{2\kappa_{p}\kappa_{m}}{4g_{m}}\right)}$$
(2)

$$\alpha_c = \alpha_p + \left(\alpha_m - \alpha_p\right) \frac{\left(1 - K_c\right) - \left(\frac{1}{K_p}\right)}{\left(\frac{1}{K_m}\right) - \left(\frac{1}{K_p}\right)} \tag{3}$$

where ϕ is the volume fraction, α refers to the Coefficient of Thermal Expansion (CTE), K refers to the bulk modulus, V is the volume fraction and G is the shear modulus. The subscripts c, p and m refer to the composite, particle and matrix, respectively. The values are compiled in Table 2. Kc in Equation 3 was calculated using Hashin's bounds [18]. The models suggest that glass-matched composite CTE can be obtained with a reasonable volume fraction of 0.5-0.6.



Figure 1 Analytical model showing reduction in CTE with increasing vol%. Experimental data is from Ref [8].

B. Thermal Conductivity

The role of interfacial thermal barrier resistance induced by the inclusion of particles is illustrated through the Hasselman-Johnson model as shown in Equation (4) [12-14].

$$K_{c} = K_{m} \frac{2(1-V_{p}) + \frac{K_{p}}{K_{m}}(1+2V_{p}) + 4\frac{K_{p}}{hD}(1-V_{p})}{(2+V_{p}) + \frac{K_{p}}{K_{m}}(1-V_{p}) + 2\frac{K_{p}}{hD}(1+V_{p})}$$
(4)

where K refers to the thermal conductivity, V is the volume fraction, h is the interfacial thermal conductivity in W/m2K (1/h is the Rint of the metal-particle interface), D is the particle diameter. The subscripts c, p and m refer to the composite, particle and matrix, respectively. With common metal-matrix composite systems, the interfacial thermal barrier is thought to arise primarily from phononscattering due to the large elastic property mismatch. Biot number, used commonly to describe the relative interfacial convection resistance at the solid-vapor interface to that inside the solid, can also be used to describe interfacial thermal conduction resistance in particulate composites. The net effect of particle size (d) and interfacial thermal conduction resistance (Rint) is represented in this case as Km Rint/d [12-13]. The composite thermal conductivity as a function of particle volume fraction for various Biot numbers is modeled using Equation (4), and is schematically illustrated in Fig. 2, for a particle size of 1µm. High thermal conductivity is retained with low interfacial thermal resistances (low Biot number) or using larger filler particles.

continued from page 13



Figure 2 Thermal conductivity with different Biot numbers.

C. Elastic Modulus

Young's modulus for rigid inclusions in a rigid matrix can be statistically determined by different numerical models [10]. Hashin-Shtrikman bounds [18] were used to predict the upper and lower bounds for the bulk modulus; the separation is dependent on the modulus ratio of particle to matrix, Ep/Em. Here, the value of m is 5.3 and the bounds are closely matched as shown in Fig. 4. Counto [20] model assumes perfect bonding between the particle and the matrix and is given by Equation (5), Isahi-Cohen [21] model assumes the constituents to be in a state of macroscopically homogeneous stress with uniform displacement in all directions and is given by Equation (6.) The estimated properties are used to predict the warpage and glass stresses.

$$\frac{1}{E_c} = \frac{1 - V_p^{1/2}}{E_m} + \frac{1}{\frac{1 - V_p^{1/2}}{E_m V_p^{1/2}} + E_p}$$
(5)

$$E_c = E_m (1 + \frac{V_p}{\frac{m}{m-1} - V_p^{1/3}})$$
(6)



Figure 3 Numerical model of Elastic Modulus.

D. Warpage

FEM Modeling of integrated thermal structures of Cugraphite composites on glass substrates was carried out using ANSOFT® ANSYS. The composite conductors are modeled as single-sided films and through-package vias to capture the stress-concentration at the via-corners, which are most sensitive to failures. The via diameter and pitch are assumed as 60 and 120 microns respectively. The cross-sectional schematic of the model is presented in Fig. 4. Material properties from Section A and C were used as given in Table 3. Room temperature is assigned as the stress-free temperature for glass while 50 C is assigned to copper. Thermal loading is used to generate stresses at the extreme temperatures of 125 and -55 C. The thermal conductivities of the materials were not taken into account. The stress analysis is presented in Table 4. It can be seen that lowering the CTE lowered the principal stresses in glass by 2-3X. This reduction makes the glass more tolerant to larger defects from TPV fabrication or dicing.

The warpage analysis of single-sided glass, plated with copper and copper-composite films is shown in Fig. 5. The results are summarized in Table 4. Lower CTE of the 60. vol % of Cu-graphite reduced warpage by nearly 3X. With CTE-matched copper, warpage can be completely eliminating, thus enabling more flexibility in package design by eliminating the need for symmetric structures.



Figure 4 (a) Cross-sectional schematic of TPV (b) 3-D meshed model of 1/8th of TPV.

Composite (vol%)	CTE (ppm/oC)	Young's Modulus (GPa)
Copper	17.3	121
Cu-Graphite (0.3)	11.52	294
Cu-Graphite (0.6)	6.98	468

Table 2 Properties from Numerical Model

Principal Stress (MPa)	Copper	Cu-Graphite (0.3)	Cu-Graphite (0.6)
@125 oC	144	102	49
@-55 oC	123	149	80

Table 3 Stress Analysis



Figure 5 Warpage of blanket copper film on thermal cycling.

Warpage (µm)	Copper	Cu-Graphite (0.3)	Cu-Graphite (0.6)
@125 oC	4.20	3.16	1.58
@-55 oC	3.50	2.52	1.26

Table 4 FEM Results For Warpage of Copper and Copper-Composites

III. Experimental Work

A. Principle of Co-electrodeposition

Electrophoretic deposition is chosen as the approach to form low-CTE conductors because of its compatibility with standard microfabrication processes. The inclusion of particles into metal deposits is dependent on several process parameters, including: 1) particle characteristics - particle concentration, surface charge, type, size; 2) electrolyte composition - electrolyte concentration, additives, temperature, pH; 3) current density; and 4) hydrodynamics of electrochemical cells together with electrode geometry [8]. The main mechanisms for particle incorporation into the metal are electrophoresis of the particles towards the cathode and adsorption of the particles at the interface. Ref. [10] proposed one of the first theories on the mechanism of co-electrodeposition as two continuous adsorption steps.

- Physical: A layer of loosely adsorbed particles with a high coverage;
- Electrochemical: Strong adsorption of particles onto the electrode by loss of ionic cloud.

Later models include transport of particles to the electrode by convective-diffusion processes, and also consider a quantitative trajectory analysis of forces acting on particles in the bath [9]. Cationic and anionic surfactants are added to change the surface characteristics of particles and improve their electrophoresis [11]. The concentration of a surfactant around the particle increases the zeta potential which offers a greater force to embed the particles.

Temperature-dependent warpage behavior was studied using shadow-moiré. Two primary factors affect the warpage: 1) built-in stress in the composite film because of electrodeposition; 2) stresses from CTE-mismatch.

B. Materials Used

Graphite flakes of grade 3160 from Sigma Aldrich were used. Cetyl trimethyl ammonium bromide (CTAB) from Sigma Aldrich was used as a surfactant. The schematic of the procedure is shown in Fig 6. Glass slides sputtered on one side with Ti/Cu was used as the substrate. Copper foils were used as the anode. The electrolyte provided by Atotech, Inc was used in this study.



Figure 6 Process-flow to analyze warpage of copper and composite films on glass.

C. Process Flow

The setup used in the electrodeposition is shown in Fig. 7. Current densities were varied as 30-40-50-60 mA/cm2. Graphite loadings of 30 g/L and 50 g/L were used. CTAB concentrations were varied depending on the graphite particle loading. The addition of surfactants decreases the agglomeration of particles so that the amount of effective particles depositing on the electrode would

significantly increase. To reduce the affinity of copper ions towards the cathode, the electrolyte was diluted. The electrolyte comprises of 250 mL of the plating solution diluted with 50 mL distilled water. The electrolyte was stirred used a magnetic stirrer for 3 hrs, each time fillers were added. This prevents agglomeration of fillers at the bottom of the beaker. The plating time for the samples was 50-60 mins. All samples were sintered in forming gas at 450oC to homogenize the composite film and improve mechanical integrity. SEM (Scanning electron microscopy) with EDS (Energy Dispersive Spectroscopy) was performed using Zeiss ultra60 FE-SEM to estimate the carbon concentration in the sample. Substrate warpage was measured by shadow-moiré using Akrometrix's Thermoiré PS200S.



Figure 7 Electrophoretic deposition setup.

The samples for warpage measurements were prepared with a light coat of white spray paint to increase the signal-to-noise ratio. A 200 line-per-inch grating was used. The thickness of the substrates used for warpage measurement ranged from 300 μ m to 1 mm.

IV. Results and Discussion

The cross-sectional images of graphite powder and the copper-graphite composite in Fig. 8 show that the morphology of the fillers in the composite is similar to that of the powder used, proving that graphite gets embedded into the copper matrix.



Figure 8 Graphite powder used (a) and cross-section image of the composite (b).

EDS analysis of composite samples that are plated at 40 mA/cm2 and 60 mA/cm2 is shown in Fig. 9. Elemental analysis showed that the C wt. % increased from 8.4 to 31.9. The EDS maps indicate that carbon is distributed throughout the sample and is not concentrated in pockets. This points out that the current density plays an important role in determining the electrophoresis of the

continued from page 15

particles towards the cathode and adsorption at the interface. All other parameters being the same, a nearly 300% increase in wt. % of carbon was observed on increasing the current density. Similar results were not observed for an increase in surfactant concentration. However, an increase from 56.6 vol. % to 63.9 vol. % of C was seen with an increase in particle loading in the electrolyte, showing that increasing the number of particles in the electrolyte has a positive effect on increasing carbon content in the final composite.



Figure 9 EDS analysis of Cu-graphite composites showing 300% increase in graphite loading with higher current densities.

Warpage measurements of the glass substrates at room temperature indicates residual stresses in glass with both copper and composite films. The warpage across a 2-inch substrate is 33 µm at room temperature and 24 µm at 99oC. The copper blanket film shows a warpage of 37 µm at room temperature and 69 µm at 99oC. This shows that matching the CTE of the composite with the glass substrate reduces warpage and is especially effective at temperatures higher than the stress-free temperature.

In-situ warpage of single-side composite-coated glass substrates was measured during temperature ramping from 25 to 170oC. Substrate warpage variation with temperature is shown in Fig. 10. With increase in vol. % of C from 28 to 63.7, the substrate warpage was reduced by 50%, with corresponding stress reduction, which is directly related to the warpage or curvature. This reduction is attributed to the reduced CTE with high graphite content in the composite film.



Figure 10 Reduction in warpage after increase in concentration of carbon.

V. Conclusions

This paper demonstrates a low-cost electrodeposition process to synthesize copper-graphite composites with above 60 vol. % C incorporation. Modeling and experimental results demonstrate greater than 2X reduction in warpage of copper-composite films. The effect of plating current density and particle loading on the composite properties (carbon concentration, mechanical integrity and uniformity) was characterized with SEM-EDS. Warpage characterization with shadow-moiré was performed to demonstrate benefits of the co-electrodeposited composites. Copper-graphite composites can significantly improve thermal, electrical and mechanical reliability performance, especially in power electronics and automotive ECUs that are shifting towards higher operating temperatures with increased functionality.

Acknowledgment

The authors would like to thank the administrative and research staff at PRC for their help.

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A Brief Early History of Raleigh

Raleigh was founded in 1792 as North Carolina's capital city. The City was named for Sir Walter Raleigh, who attempted to establish the first English colony on the shores of the new world in the 1580s. In 1587, under the direction of Sir Walter Raleigh, John White founded the "Cittie of Raleigh" and then returned to England. Upon White's return in 1590, the colony had disappeared. Today Raleigh is popularly referred to as the "Lost Colony."

Modern Raleigh was originally called Wake Crossroads and it was home to Native American Iroquois, Sioux and Algonquin tribes.

The North Carolina General Assembly decided that Wake Crossroads would be a great spot to set up permanent residence, and purchased a thousand-acre plot of land from local businessman Joel Lane. The tract of land cost \$2756. Sen. William Christmas, a surveyor, was hired to lay out the new city. Initial plans were modeled on Philadelphia's, the nation's capital at the time. And in November of 1792, the North Carolina General Assembly chose the name "Raleigh" for its capital city.



Joel Lane home built in 1769

Completed in 1840, the North Carolina Capitol building is one of the finest and best-preserved examples of the Greek Revival style of architecture. It is a National Historic Landmark and is open to the public.



North Carolina Capitol

On April 26, 1865, at the end of the Civil War, Gen. Johnston surrendered 90,000 of his Confederate troops to Sherman at Bennett farmhouse near Durham. Bennett Farm (Bennett Place) is the site of the largest surrender of Confederate soldiers.



Bennett Place

NC was a state of farmers and is among the South's first industrial areas. Its original mission was to serve as a place for those traveling north and south to stop for a rest. Raleigh remained a small town (in 1800, Raleigh's population was 669) until the 1920s, at which point it began to develop into a commercial nexus in the eastern part of the state. The population of Raleigh grew to 2,674 by 1820, the third largest city in North Carolina, to 2,244 by 1840, the fourth largest city in North Carolina, and to 4,780 by 1860. Fast forward to 2014, Raleigh's population had grown to 439,896.

The agriculture economy switched from cotton to tobacco, and the railroad was built to connect Raleigh to the surrounding rural communities and beyond. Many of the small towns of eastern North Carolina that today remain small towns, were established in these early years of the century, courtesy of the railroad and tobacco.

Along with the business of state government, today education is a major enterprise in Raleigh. In addition to North Carolina State University, Raleigh is home to many other educational institutions, including Shaw University, St. Augustine's College, William Peace University, Meredith College, Campbell Law School, Harris Barber College, Strayer University and Wake Technical Community College. Both Shaw and St. Augustine's were established shortly after the end of the Civil War—in 1865 and 1867, respectively—to educate freed slaves. Shaw was the first such institution established in the country for that purpose.

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Raleigh Theatres

Greater Raleigh offers theaters for everyone. Great artists and award winning venues abound. Duke Energy Center for the Performing Arts, in downtown Raleigh, is home to the Fletcher Opera Theater, Meymandi Concert Hall, Kennedy Theatre, Memorial Auditorium, and Betty Ray McCain Art Gallery.

Experience the shows at area favorite Coastal Credit Union Music Park at Walnut Creek. There are all-day multishows at Bud Light Downtown Live and there are smaller, more intimate shows at the North Carolina Museum of Art's Park Theater.

Led by a class of creative artists and innovators, Raleigh is bursting at the seams with an endless supply of live performing arts and visual arts galleries. Visit nationally-acclaimed presenting organizations such as Carolina Ballet and North Carolina Theatre. Raleigh also has plenty of locally-owned galleries and collegiate arts programs to explore.

Arts in Raleigh aren't just stand-out attractions. They're built into the fabric of the community everywhere you look. A community of dancers, painters, photographers, sculptors and curators have influenced neighborhoods all across the destination.

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Memorial Auditorium

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The Philharmonic Association fosters the love of great music in young musicians through ensemble training in full symphony orchestras, string orchestras and jazz groups that include opportunities to study with professional musicians. Each concert season includes performances from symphonic, string and jazz ensembles with occasional events featuring chamber ensembles.

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JULY/AUGUST 2017

Raleigh Entertainment Districts

SO Years

Raleigh has many personalities, a diverse network of neighborhoods and downtown entertainment districts, each with its own culture and flair. There are districts for strolling along tree-lined sidewalks with art gallery views, districts for shopping, districts for dancing in nightclubs and districts that remind you how much you love cobblestone streets with antique lampposts.

Raleigh's defined streetscapes are walkable and can be experienced the way a local resident would choose to spend time.

Glenwood South

Raleigh's trendiest district abounds with a mix of great restaurants and spirited nightlife. This corner of the city attracts all ages. During the day you will find families strolling the main strip and by night the area surrenders to a good-times street party.

Capital District

Stately buildings and classic architecture line the streets of this busy business district. The NC State Capitol is at the center of a six-acre park that also offers statues, park benches and shaded walkways. Completed in 1840, it originally housed the governor's office, cabinet offices, legislative chambers and the state library. This is where decisions are made and history is honored. In addition to the State Capitol, State Archives, and Governors Mansion this area also houses a number of museums. Don't miss dining under the three-story-tall globe at The Daily Planet Cafe.

Fayetteville Street

A main street on a grand scale, Fayetteville Street epitomizes Raleigh as a sophisticated Southern city, with distinctive restaurants and impressive skyscrapers mingling with restored historic buildings. It stretches from the Duke Energy Center for the Performing Arts to the NC State Capitol.

Warehouse District

See what all the fuss is about by experiencing legendary barbecue, or be part of the see-and-be-seen crowd at one of the nightclubs in a district characterized by old warehouses and historic brick buildings. CAM Raleigh (Contemporary Art Museum) is located in the Warehouse District. Defining "urban hip," the row of massive brick structures and out-of-the-way restaurants and clubs offer those who know a full evening's entertainment. The Flying Saucer Draught Emporium boasts one of the largest beer selections in the city. The Pit Authentic Barbecue is known for its traditional barbecue in a trendy setting.

Moore Square Art District

At the intersection of Blount and Martin Streets in a three-block radius around historic City Market, the district includes commercial and display galleries, anchored by Raleigh's Artspace—a 30,000 square foot historic



Fayetteville Street

building that has 25 dedicated artist studios. Listed on the National Register of Historic Places, Moore Square Park offers a nice getaway for downtown employees looking for a relaxing space in Raleigh's central business district. City Market offers an eclectic collection of independent retail stores and great restaurants surrounded by charming cobblestone streets.

Tip: Downtown Raleigh's Free R-Line Bus

Replete with air-conditioning, plasma TVs and plush seats, the two hybrid-electric buses of Raleigh's free R-Line circulate through downtown all day and into the night. The buses carry tourists and locals, pub crawlers and date-night couples counter-clockwise in a loop around the Capital District, Glenwood South, Warehouse District, Fayetteville District, and Moore Square. You can track the real-time location of the closest bus at http://www.godowntownraleigh.com/get-around/r-line/status.

Courtesy GRCVB/VisitRaleigh.com and Downtown Raleigh Alliance



Raleigh Museums

Raleigh is often dubbed the "Smithsonian of the South," based on the abundance of high-quality free museums, historic attractions and educational institutions. You'll better understand what that means the instant you're warmly welcomed by our smart, savvy locals who have created and proudly carry on a number of unique visitor experiences that define the heritage and culture of our Southern metropolis.

Discover rich history and science through captivating, state-of-the-art exhibits in Raleigh at the North Carolina Museum of Natural Sciences, recognizable by its threestory multimedia globe named the Daily Planet, and the North Carolina Museum of History, which brings our state's diverse history alive with an expansive permanent collection; admission is free at both museums! For all you sports fans: the North Carolina Museum of History is also the location of the North Carolina Sports Hall of Fame.

North Carolina Museum of Natural Sciences

11 W. Jones Street Raleigh, NC 27601 Phone: 919.707.9800, Toll-Free: 877.462.8724

The Southeast's largest natural history museum has four floors of exhibits, live animals, 3D movies, three gift stores and two cafes. The iconic 70-foot-diameter globe at its center houses a three-story theater with live programming and ambient movies on its giant screen. Visitors can observe scientists at work in five glass-walled research labs, and in three Investigate Labs they can perform experiments designed and led by Museum educators. Exhibits include the world's most complete Acrocanthosaurus dinosaur; a juvenile T. rex; six great whales; a 10,000-gallon aquarium; a two-story waterfall; walk-through dioramas; a Naturalist Center with real specimens; a vet window where visitors can watch live procedures and talk to the staff; and a butterfly room that also houses a two-toed sloth. The Museum hosts spectacular new featured exhibits every year and hands-on programs daily. Hours: Mon.-Sat., 9am-5pm; Sun., noon-5pm. Free general admission.



The Daily Planet globe, North Carolina Museum of Natural Sciences



North Carolina Museum of History

5 E. Edenton Street Raleigh, NC 27601 Phone: 919.807.7900 Evolve more than 14 000

Explore more than 14,000 years of NC history, from the state's earliest inhabitants through the 20th century. The award-winning exhibition The Story of North Carolina features fascinating artifacts, multimedia presentations and an interactive format for all ages. Other exhibits highlight the state's military history, sports heroes, decorative arts and more. Programs include family events, music performances and craft demonstrations. The Museum Shop and the restaurant, Pharaoh's at the Museum, are open daily.



Museum of History

IMAPS 2017

North Carolina Sports Hall of Fame

5 E. Edenton Street Raleigh, NC 27601 Phone: 919.807.7900

Located in the NC Museum of History, the NC Sports Hall of Fame exhibit spans more than 3,000 square feet and showcases memorabilia donated by many of the hall's approximately 300 inductees. Learn about these sports legends and the impact of sports in the state. Free admission. Hours: Mon.-Sat., 9am-5pm; Sun., noon-5pm.

If your creative side is calling out, stroll through the beautiful North Carolina Museum of Art—equally perfect for a date night out or a day with the family—or be enriched at the Contemporary Art Museum (CAM Raleigh), the only non-collecting contemporary art museum in the state.

North Carolina Museum of Art

2110 Blue Ridge Road Raleigh, NC 27607 Phone: 919.839.NCMA

One of the premier visual arts museums in the South, featuring a dramatic gallery building, home to a worldclass collection including more than 30 Rodin sculptures and a center for special exhibitions, plus a 164-acre Museum Park. Free admission (fee for some exhibitions and programs). Hours: Tues.-Thurs., 10am-5pm; Fri., 10am-9pm; Sat.-Sun., 10am-5pm.



NC Museum of Art

CAM Raleigh

409 W. Martin Street Raleigh, NC 27603 Phone: 919.261.5920

CAM Raleigh sparks new thinking by creating everchanging experiences that explore what's now and nearing in art and design. Enjoy weekly guided tours every Sun. at 2pm. Release your imagination at the Creation Station. Bring friends every First Friday for food trucks, student docents and entertainment! First Fridays are free from 6-10pm. Call or visit the website for information about exhibitions, programs and special events. General admission: \$5. Hours: Thurs.-Fri., noon-6pm; Sat.-Sun., noon-5pm; Tues.-Wed., by appointment; Mon., closed.

Kids will have a ball at Marbles Kids Museum, where they get a chance to imagine, discover and learn in dozens of hands-on exhibits and educational programs, plus take in a larger-than-life movie at the Wells Fargo IMAX Theatre at Marbles.

Marbles Kids Museum

201 E. Hargett Street Raleigh, NC 27601 Phone: 919.834.4040

Delivering purposeful play in a big way, Marbles allows children to imagine, discover and learn in dozens of interactive exhibits, daily educational programs, field trips, birthday parties, special events and giant-screen IMAX films. For children ages one to 11, and adults. \$5 admission, children under one and members play free. Hours: daily, 9am-5pm (open until 7pm every Thur. and on First Friday). Specifically designed to deliver the world's most immersive movie experience, the IMAX Theatre at Marbles boasts NC's only 3D-capable giant screen. From inspiring educational documentary films to Hollywood's biggest feature films, the theatre makes you feel as if you are in the movie. IMAX rates and show times vary; call or visit website.

Courtesy GRCVB/VisitRaleigh.com and Downtown Raleigh Alliance



A D V A N C I N G MICROELECTRONICS

IMAPS 2017



Scenes from the Past 50 Years!











Cracow Conference





Caswell president's party



Nantucket



First Russia Chapter Meeting





Prague Meeting





Brazil Chapter

JULY/AUGUST 2017

IMAPS 2017



Japan Conference







Taipei Conference



Israel Chapter 2000





Strasbourg



See more onsite at IMAPS 2017 in Raleigh.





IMAPS 2017

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If you are interested in:

 seeing and doing more in Raleigh, N.C., start with the Visitor Information Center (VIC) (C,5); relocating to Raleigh, start with the Chamber of Commerce (C,6)

Points of Interest

- Artspace (D, 5)
 City Market (D, 5)
- O City Plaza (C, 5)
- O City of Raleigh Municipal Complex (B, 4)
- O City of Raleigh Museum (C, 4)
- O Contemporary Art Museum (A, 5)
- Duke Energy Center for the Performing Arts (C, 6)
 - Memorial Auditorium **Fletcher Opera Theater** Meymandi Concert Hall
- Kennedy Theatre O Pope House Museum (C, S)
- Federal Government Complex (E, 4)
- Greater Raleigh Chamber of Commerce (C, 6)

* Raleigh, N.C., Visitor Information Center (C. 5)



Haywood Hall House and Gardens (D, 3)

- ø LL Polk House (D, 1)
- ۲ Marbles Kids Museum/Wells Fargo (MAX Theatre (D, 4)
- ø N.C. Executive Mansion (D, 3)
- 0 N.C. Museum of History (C, 3)
- N.C. Museum of Natural Sciences (C, 3)
- D N.C. State Archives (D, 3)
- N.C. State Capitol (C, 3)
- N.C. State Legislative Building (C, 3)
- Raleigh Convention Center (C, 5)
- Red Hat Amphitheater (8, 5)
- Wake County Courthouse (C, 5)

Transit

- Amtrak Station (A, 5)
- City Bus Terminal (D, 4)

Q R-LINE Stops (route runs counterclockwise) ---- R-LINE route after 6:30pm

Hotels

- Holiday Inn Raleigh Downtown (B, 3) Days Inn Downtown Raleigh (B, 2)
- Raleigh Marriott City Center (C, 5) Residence Inn Raleigh Downtown
- (opening early 2017) (C, 6)
- Sheraton Raleigh Hotel (C, 5)
- 1 Hampton Inn & Suites Raleigh Downtown/Glenwood South (A, 1)

Symbols

- Parking Parking entrance Post office
 - O Visitor information - Flow of traffic - Railroad

Topical Workshop and Tabletop Exhibit on

Thermal Management

November 7-9, 2017 Toll House | Los Gatos, CA

General Chair

Dave Saums DS&A LLC dsaums@dsa-thermal.com Tel: 978-499-4990 Program Chair Vadim Gektin Futurewei Technologies atwprogramchair@gmail.com Tel: 408-330-5352

ABSTRACTS DUE: AUGUST 9, 2017 Early Registration & Hotel Deadline: October 1, 2017

ABSTRACTS ARE SOLICITED IN THE FOLLOWING AREAS:

- Market Drivers: Understanding thermal challenges and business / economic drivers that influence change in electronic systems design and manufacturing – and how these impact thermal design requirements. Developing market trends, market segmentation, cost drivers and reliability factors are examples of topics that set the framework for where and what types of new technical solutions are viable.
- Multi-Die Packaging: Advanced packaging technologies, such as System-In-Package, Multi-Chip Module and Multi-Package Module, stacked-die, etc. provide significant opportunities for miniaturization and performance enhancements. These technologies also can introduce significant thermal and interconnect challenges that must be balanced against those benefits.
- Mobile and Handheld Devices and the Internet-of-Things (IoT): Wearables, mobile and medical devices, small displays, tablets and notebooks are increasingly critical for our interconnected world. These devices often introduce unique component- and system-level thermal management challenges that require novel design approaches and materials.
- Wireless and Telecom Infrastructure: High performance telecom hardware have challenging component and system level requirements that require technical advances to meet the evolving needs for routers, networked systems, base stations, etc.
- Power Semiconductor Thermal Components, Systems, and Solutions: Developments in IGBT thermal management and packaging strongly influence advances in electronic and electrical drive systems. These advances are increasingly important in the Electric Vehicle/Hybrid Electric Vehicle and renewable energy markets.
- Mil/Aerospace: Emerging military and aerospace systems, including avionics, RF, and microwave components and modules for phased array radar, countermeasures, and other systems, require advanced thermal management as well as high-temperature materials and packaging.
- System-Level Cooling: The thermal design of complex systems, such as highperformance computing systems, relies on extensive component- and system-level thermal management analysis to address the broad spectrum of issues that entail a comprehensive system design.
- Data Center Cooling: Data center cooling includes a variety of design optimization activities including cooling provisioning, airflow control, temperature distribution and migration paths that range from forced air convection to system liquid cooling.

- Liquid cooling, Phase-change, and Refrigeration: Advanced cooling methods that use liquid, latent heat and/or active cooling provide opportunities for enhanced performance and design flexibility. Effective designs must balance these advantages against factors including life-cycle cost, reliability and serviceability impact.
- Thermal Interface Materials (TIMs) and Testing: Advanced thermal interface materials that may include organic, metallic and graphitic materials in bulk form as well as nanoscale are enabling significant advances in the thermal management of high-performance processors, memory, telecom, IGBT, RF, and microwave components and systems. Effective testing and reliability methods and standards are critical in determining the suitability of a TIM for a given application.
- CTE-Matching and High Thermal Conductivity Materials: Metallic, ceramic and composite materials have been engineered to exhibit excellent thermal conductivity with controlled coefficient of thermal expansion (CTE) properties to allow for better matching with GaN, SiC, silicon or ceramic materials to reduce thermal stresses in component packaging.

PREPARATION OF ABSTRACT:

Speakers should submit one copy of a two-paragraph abstract describing their proposed 25-minute presentation no later than **AUGUST 9, 2017**. No formal technical paper is required.

Abstracts must be submitted on-line at http://www.imaps.org/abstracts.htm.

A post-conference DOWNLOAD containing the full presentation materials as supplied by authors will be emailed approximately 15 business days after the event to all attendees. Presentation material must be submitted onsite no later than NOVEMBER 9, 2017, and will be included on the post-conference DOWNLOAD.

Questions:

Brian Schieman, bschieman@imaps.org You may also contact the workshop chairs.

www.imaps.org/thermal



Amkor Technology Completes Acquisition of NANIUM TEMPE, Arizona, May 22, 2017—Amkor Technology, Inc. (AMKR) announced that it has completed the acquisition of NANIUM S.A., a world class provider of wafer-level fan-out (WLFO) semiconductor packaging solutions.

The acquisition of NANIUM will strengthen Amkor's position in the fast growing market of wafer-level packaging for smartphones, tablets and other applications. NANIUM has developed a high-yielding, reliable WLFO technology, and has successfully ramped that technology to high volume production.

"Amkor is a leader in wafer-level CSP and high-density integrated fan-out technologies," said Steve Kelley, Amkor's president and chief executive officer. "With the acquisition of NANIUM, we will have an equally compelling value proposition in the low-density fan-out area. NANI-UM is widely viewed as the fan-out technology leader as well as a very capable manufacturer, having shipped more than one billion WLFO packages utilizing a state-of-theart 300mm wafer-level packaging production line."

NANIUM employs approximately 650 people and is based in Porto, Portugal.

About Amkor Technology: Amkor Technology, Inc. is one of the world's largest providers of outsourced semiconductor packaging and test services. Founded in 1968, Amkor pioneered the outsourcing of IC packaging and test, and is now a strategic manufacturing partner for more than 250 of the world's leading semiconductor companies, foundries and electronics OEMs. Amkor's operational base includes 10 million square feet of floor space with production facilities, product development centers, and sales and support offices located in key electronics manufacturing regions in Asia, Europe and the U.S. For more information, visit www.amkor.com.



DuPont Announces 2017 Packaging Innovation Award Winners

Honorees highlight the packaging industry's commitment to sustainability, personalization and solving global challenges



2017 DuPont Awards for Packaging Innovation

Winners



DIAMOND Winner: Fritz™ Water Vest (Solutions Inc., USA):



DIAMOND Finalist: Compostable "Pizza Pod" (Zume Pizza, USA):



GOLD Winner: Peelfit™ Can (CROWN Food Europe, France):



GOLD Winner: Ice Cream Mini Cup 140ml: Closure PP In Mold Label with spoon inside, Cardboard Cup and Alu/PE sealing (FRONERI, Brazil):



GOLD Winner: Vento™: Advanced coffee packaging with integrated degassing system (Amcor Flexibles, Switzerland):



SILVER Winner: Farmacy Beauty – Honey Potion Renewing Antioxidant Hydration Mask (VP+C, USA):



WILMINGTON, Delaware, May 22, 2017 – DuPont has announced its 2017 winners of the DuPont Awards for Packaging Innovation, honoring companies that have demonstrated major advancements in packaging technology to address the diverse and particular needs of consumers in markets around the world.

This year's Diamond Award, the highest honor, was awarded to the Fritz[™] Water Vest, which allows people in developing countries to carry up to 20 pounds of water easily and safely. Judges felt this is an out-of-the-box solution for a significant global problem and was designed with an overwhelming sense of the greater good. The vest is antimicrobial, ergonomic and reusable.

"The DuPont Awards for Packaging Innovation demonstrate how creative, committed and agile the packaging industry is in addressing global issues and consumer needs," said Bernard Rioux, global packaging leader, Du-Pont Performance Materials. "This year's winners included solutions for novel food storage, fermenting food products, premium beauty products, new packaging materials to target millennials and more. This competition brings out the very best of everyone in the packaging industry, and we are thrilled to see innovators raising the bar each year."

Now in its 29th year, the DuPont Awards for Packaging Innovation is the industry's longest running, global, independently judged celebration of innovation and collaboration throughout the value chain and is recognized globally as the leading awards program in the sector. The international competition honors innovations in packaging design, materials, technology and processes. An inde-

continued from page 29

pendent panel of packaging experts evaluated nearly 150 entries from 24 countries and recognized those that excel in the categories of technological advancement, responsible packaging and enhanced user experience. In addition to the award noted above, the judges awarded five diamond finalist award winners, nine gold winners and six silver winners based on "excellence" in one, two or three categories.

"The DuPont Awards for Packaging Innovation is exciting because of the global nature of the competition. It is objective, you don't have to use DuPont materials, and there is no entry fee," said Lead Judge David Luttenberger, CPP, global packaging director of Mintel Group Ltd. "Du-Pont brings a great variety of disciplines of expertise for the judging panel to really get a global perspective across design, engineering, retail, converting, and academia, which helps us hone in on what's important and what's valuable about packaging."

2017 DuPont Awards for Packaging Innovation Winners

DIAMOND WINNER

Fritz[™] Water Vest (Solutions Inc., USA)

DIAMOND FINALISTS

- Compostable "Pizza Pod" (Zume Pizza, USA)
- Cryovac[®] OptiDure[™] Abuse Bag (Sealed Air, USA)
- Light-weight sustainable agrochemical auto-stackable 15L PET containers (Dow AgroSciences, Germany)
- MGI JETvarnish 3D Digital Decoration Process for Folding Cartons & Labels from Marrs Printing & Packaging (MGI, USA)
- Plantic[™] R: Ultra-high barrier renewable and recyclable packaging material (Kuraray [Plantic Technologies Ltd.], Australia)

GOLD WINNERS

- Design realization with breakthrough technology enhancing productivity and less footprint (AMOREPA-CIFIC, South Korea)
- Ice Cream Mini Cup 140ml: Closure PP In Mold Label with spoon inside, Cardboard Cup and Alu/PE sealing (FRONERI, Brazil)
- Insignia Freshtag (Insignia Technologies, UK)
- MosquitoPaQ[™] OUTDOOR ZONE no-bite SPATIAL Repellent Pouch (PPi Technologies GROUP, USA)
- New packaging combining tradition and science (CJ Cheiljedang, South Korea)
- Peelfit[™] Čan (CROWN Food Europe, France)
- PepsiCo's Granola Goes Nuts Cross Directional Laser Scored Flow Wrapper (PepsiCo and Printpack, USA)
 Shah Basta Scoret, Brd Charg (Course Illingia Participation)
- Skol Beats Secret Red Glass (Owens Illinois, Brazil)
- Vento[™]: Advanced coffee packaging with integrated degassing system (*Amcor Flexibles, Switzerland*)

SILVER WINNERS

- Direct Object Printing for Full Package Decoration (Plastipak Packaging, Inc., USA)
- Farmacy Beauty Honey Potion Renewing Antioxidant Hydration Mask (VP+C, USA)
- "FUJI•M•O", Flexible packaging for the inkjetgravure hybrid printing machine (FUJI TOKUSHU SHIGYO CO., LTD, Japan)

- How2Recycle[®], the next generation recycling label for packaging (*GreenBlue*, USA)
- Kellogg's[®] Nutri-Grain[®] Bakery Delights Tactile Packaging (Bemis Company, Inc., USA)
- Lightweight 20-ounce Vitaminwater[®] container with PowerStrap[™] and Active Hinge[™] technologies (*Am*cor Rigid Plastics, USA)

DuPont Performance Materials (DPM) is a leading innovator of thermoplastics, elastomers, renewably sourced polymers, high-performance parts and shapes, as well as resins that act as adhesives, sealants, and modifiers. DPM supports a globally linked network of regional application development experts who work with customers throughout the value chain to develop innovative solutions in automotive, packaging, construction, consumer goods, electrical/electronics and other industries. For additional information about the DuPont Packaging Awards, visit packagingawards.dupont.com or follow DuPont Packaging on Twitter, LinkedIn and YouTube.

Contact:

DuPont Performance Materials Melissa Bruhl, 302-992-2048 melissa.d.bruhl@dupont.com



Ceramic Packaging Solutions For Optimum Performance

Remtec Adds Gold Tin Plated Ceramic Combo Lids to Complement its Ceramic SMT Packages

Norwood, MA, June 2, 2017—Remtec Inc. (www. remtec.com), the leading manufacturer of ceramic substrates, packages and submounts using PCTF[®] (Plated Copper on Thick Film) metallization, has added gold tin plated Ceramic Combo Lids to its line of ceramic SMT packages. Now designers can complement a full line of hermetic, ceramic SMT substrates and packages with high reliability gold tin plated Ceramic Combo Lids, all from a single source.

Remtec has developed a proprietary technique combining PCTF metallization and gold tin plating to produce the high reliability Ceramic Combo Lids. Remtec's Combo Lids provide labor savings via the elimination of manual preform attachment, especially on small profile applications. In addition, a unique gold tin plating technology greatly reduces the amount of solder voids common for lids with tack-welded gold tin preforms, thus resulting in higher production yields.

Remtec's Ceramic Combo Lids are available in two types: a flat gold tin plated lid and a five-sided box or "cavity lid." Both styles exhibit excellent void-free soldering ensuring full hermeticity when used with high reliability hermetic substrates or packages. Remtec's proprietary manufacturing process provides uniform gold tin flow and the ability to vary the thickness according to the needs of the application. Remtec's ceramic lids meet mili-

tary standards and are available in prototype, small lot, and production quantities.

The applications for Remtec's new gold tin plated Ceramic Combo Lids include military, aerospace, avionics and high reliability electronics.

Remtec, a RoHS compliant, ISO 90001:2008 registered and ITAR compliant company, operates a manufacturing facility (totaling 33,000 sq. ft.) in Norwood, MA. Remtec produces custom and semi-custom packaging solutions for sensors and detectors, RF/MW products, DC power electronics, optoelectronics and other high density and power circuitry in commercial, industrial and military industries.

Contact: Mr. Nahum Rapoport Remtec, Inc. 100 Morse Street Norwood, MA 02062 Phone: 781-762-9191 Fax: 781-762-9777 sales@remtec.com www.remtec.com

Editorial Contact: Dean M. Wood 401-225-6789

SIKAMA Reflow Solder

Systems

www.sikama.com

Sikama International Partners with Air Products

Santa Barbara, CA—Sikama International Inc. and Air Products and Chemicals Inc. have partnered to introduce the Electron Attachment Fluxless Reflow System to the electronics wafer level packaging segment.

Air Products has developed the electronics integrated circuit packaging and assembly segment. This novel flux-free soldering technology uses activated hydrogen to remove metal oxides from electroplated solder bumps on semiconductor wafers and permit reflow of these bumps to obtain the proper shape and size for interconnection onto a package or substrate.

We call the technology Electron Attachment for Hydrogen Activation.

Sikama International's UP1200 Electron Attachment (EA) version furnace is a five heat zone, linear tunnel process oven that is capable of handling up to 300 mm wafers and can process 60 wafers per hour. The furnace is designed to be used to remove metal oxides from solder bumps on UBM wafers and solder caps from copper pillar wafers via the electron attachment technology, which activates hydrogen to produce hydrogen anions and then reflow the solder to their final shape in the absence of traditional organic flux or formic acid in vacuum processes. The furnace is capable of operating at temperatures up to 400°C. The wafers achieve a consistent heat profile based on non-contact heating in combination with forced thermal convection and the wafers are conveyed through the furnace via a unique roller transport system. The system may be operated with an ambient pressure with an atmosphere forming gas mixture of 5% H2/95% N2 in the activation zones and nitrogen in the remaining process zones.

Contact:

Sikama International Inc. 118 E Gutierrez Street Santa Barbara, California, 93101 Phone: 805-962-1000 Fax: 805-962-6100 email: sales@sikama.com web: www.sikama.com





CHAPTER NEWS

Your IMAPS Member Benefits at Your Chapter Level

Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar

Central Texas

The Central Texas local chapter of IMAPS had a successful meeting May 9, 2017 with four speakers and pizza. The presentations were:

1. "Graphene for Future Very Large Scale Integration (VLSI)" presented by Greg Yeric, Director, Future Silicon Technology Group, ARM Research

2. "Analog Package Enablers: Choosing an Embedded Technology" presented by Mark Gerber, Director, Engineering and Marketing for Flip Chip and SiP, ASE

3. "Leadless Flip Chip PLGA for Networking Applications" presented by Andrew Mawer, Manager, Packaging Analysis Lab, NXP

4. "Artificial SuperIntelligence (ASI) and the Death of Mankind: What, Me Worry?" presented by Paul Golata, Sr Technical Content Specialist, Mouser Electronics

The next meeting is being planned for August 24, 2017 and will include a factor tour.

Submitted by Bennett Joiner



Greg Yeric, Director, Future Silicon Technology Group, ARM Research



Mark Gerber, Director, Engineering and Marketing for Flip Chip and SiP, ASE



Paul Golata, Sr Technical Content Specialist, Mouser Electronics



Andrew Mawer, Manager, Packaging Analysis Lab, NXP

CHAPTER NEWS

San Diego

Summary of April, 2017 meeting:

Topic: James Webb Space Telescope: Parts, Materials, and Processes

Presenter: Dr. Michael Vernoy—Northrup Grumman Aerospace Systems

James Webb Space Telescope (JWST) is a fascinating tennis court-sized infrared space telescope which will be NASA's premiere space observatory for the next decade. After launch, it will begin to unlock many secrets, including details of the universe's first stars, and of the formation of ours and other solar systems—including ones that could be supporting life. Dr. Vernoy highlighted the challenges of material selection for the segmented mirrors and the sunshields to survive the space environment. While the Hubble telescope has a 2.4 meter mirror, the JWST features a larger segmented mirror—6.5 meter diameter—and will be located near Earth-Sun L2 point. The primary mirror segments are made of Beryllium and then coated with gold. A large sunshield will keep its mirror and four science instruments below 5K (-220C; - 370F).

The sunshield will block heat and light from the Sun and Earth. The 3 major sections of the JWST include an optical telescope element, mirror and its structure, the Spacecraft Element which includes spacecraft bus + sunshield and the integrated science instrument module which holds instruments and other systems. The Spacecraft Bus must support the 6.5 ton space telescope, which itself weighs 350 Kg. It is made primarily of graphite material. The instruments module will have near IR camera, Near Infrared Spectrograph, Mid IR Instrument and Near IR imager + Slitless Spectrograph.

The presentation was a good overview and insight into the challenges of design and architecture of the JWST telescope.



Dr. Michael Vernoy, Northrup Grumman Aerospace Systems

Submitted by Mumtaz Bora



IMAPS 2017 October 9-12, 2017 Raleigh Convention Center Raleigh, NC www.imaps2017.org

Exhibit at IMAPS 2017

The 2017 show is particularly special for IMAPS, as the Society will be celebrating its 50 years of bringing together the entire microelectronics supply chain. The headquarters home of IMAPS – the Research Triangle region of North Carolina – will serve as host for this special edition of the annual symposium. The city of Raleigh and the surrounding region is home to a thriving research community, a bustling technology sector, and excellent visitor amenities.

You will find the important information your organization needs to apply for an exhibit or sponsorship at the link below. Please review the critical information from IMAPS to acquaint yourself with the sponsorship and exhibit opportunities, pricing, and the application process.

IMAPS strives to make the 2017 show better than ever for exhibitors and attendees alike. For up-to-date information on all details related to the show, visit **www.IMAPS2017.org** regularly.

Get the complete Exhibitor Prospectus here:

www.imaps.org/imaps2017/IMAPS2017SponsorExhibitorProspectus.pdf

UPDATES FROM IMAPS



International Microelectronics Assembly and Packaging Society www.IMAPS.org

Events

INDIVIDUAL MEMBERSHIP \$95 annually

Publications

- Membership includes a one year subscription to Advancing Microelectronics
- Access the online Journal of Microelectronics and Electronic Packaging through IMAPSource
- Complimentary IMAPSource downloads
- Enjoy discounts on IMAPS events like the International Symposium on Microelectronics and yearround advanced technical workshops
- Convenient, informative webinars
- Speaking and publishing opportunities

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Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!

Microelectronics Research Portal

IMAPSource transitioned to membership level plans for free downloads on April 1, 2016. The number of free annual downloads included in your membership corresponds to your member type.

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UPDATES FROM IMAPS



International Microelectronics Assembly and Packaging Society www.IMAPS.org

CORPORATE MEMBERSHIPS

Join now!

IMAPS corporate memberships are designed to give your company a competitive advantage in the microelectronics packaging industry. Choose the right membership to meet your exhibition, advertising, discount registration needs and more.

	Premier	Standard
Membership package inclusions	For organizations with more individual members or those seeking more marketing exposure	Our most popular corporate membership package
Number of employees who receive individual membership benefits	No limit to number of individual members with full online access; up to 5 receive print magazine	2
Access to IMAPSource microelectronics research portal	IP recognition allowing unlimited access for all computers in one network	150 downloads via two (2) selected member logins
Press releases in Corporate Bulletin	Up to 1 press release per bulletin (twice monthly)	Up to 1 press release per bulletin (twice monthly)
Member pricing for exhibitor events	Included	Included
JOBS Marketplace	Complimentary job postings	Complimentary job postings
Use of membership mailing list	3x per year	1x per year
IMAPS.org advertising	Complimentary	Member discount
Magazine advertising	One 1/4 page ad incl. annually, plus 15% discount on any additional ad	15% discount
Online Industry Guide	Includes company listing, link to website, product and service categories	Includes company listing, link to website, product and service categories
Global Business Council	Membership included	Membership included
Webinar Sponsorship	30% discount	30% discount
Annual dues	\$2,500	\$750

Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!

UPDATES FROM IMAPS

Premier Corporate Members

IMAPS has introduced a new level of support for corporate members. These companies have decided to participate in our Society at the Premier Corporate Member level. We are extremely grateful for their dedication to the furtherance of our educational opportunities and technological goals.







































MEMBER NEWS

Welcome New IMAPS Members!

January-February 2017

Organization Members Semi-Conductor Laboratory

Individual Members

Yo Adachi Ravi Agarwal Rahul Agarwal Samar Alhihi Sami Alkharabsheh Rafael Akio Alves Watanabe Ingmar Andersson Francoise Angoua Leonel Arana lucile arnaud Richard Barnett Mohammad Bataineh Vincent Belanger Marion Brackstone Chris Brue Jeff Catlin Bertrand Chambion Sri Chaitra Jyotsna Chavali Alex Chow Martin Clarke Lynnette Colby Collin Coolidge Ned Corron Timothy Coyne Ian Dale James Dark Chandrika Dattathri Robin Daugherty Stephen Devenport Vincent DiCaprio V. Dragoi Eric Dunton Kevin Engel Daniel Feery Jeffrey Fitzgerald Ron Fletcher Gregory Fritz Sam Gu

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Advancing Microelectronics **2017 Editorial Schedule**

Issue Theme Copy Deadline	Ad Commitment	I/Os Deadline
Sept/Oct	MEMS and Thermal Management	Jul. 8 July 13
Nov/Dec	Ceramic: Thick and Thin Film	Sep. 8 Sep. 13

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CALENDAR OF EVENTS

2017	start end _		
SEPTEMBER	9-13-17	9-14-17	Additive Manufacturing 2017 Huntsville, AL www.imaps.org/additive
OCTOBER	10-9-17	10-12-17	IMAPS 2017 Raleigh, NC www.imaps.org/imaps2017
NOVEMBER	11-7-17	11-9-17	Topical Workshop and Tabletop Exhibit on Thermal Management Los Gatos, California www.imaps.org/thermal
DECEMBER	12-5-17	12-7-17	3D ASIP 2017 - 3D Architectures for Heterogeneous Integration & Packaging San Francisco, CA http://3dasip.org/
2018			
MARCH	3-5-18	3-8-18	Device Packaging 2018 WekoPa Resort and Casino, Fountain Hills, Arizona www.imaps.org/DevicePackaging
ΜΑΥ	5-8-18	5-10-18	HiTEC 2018 - High Temperature Electronics Albuquerque, New Mexico www.imaps.org/hitec

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