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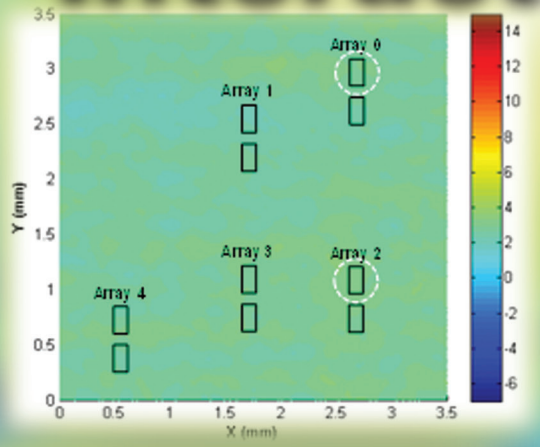
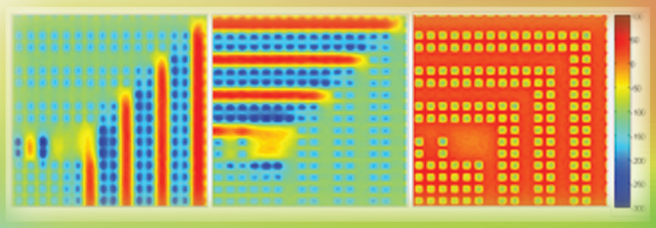
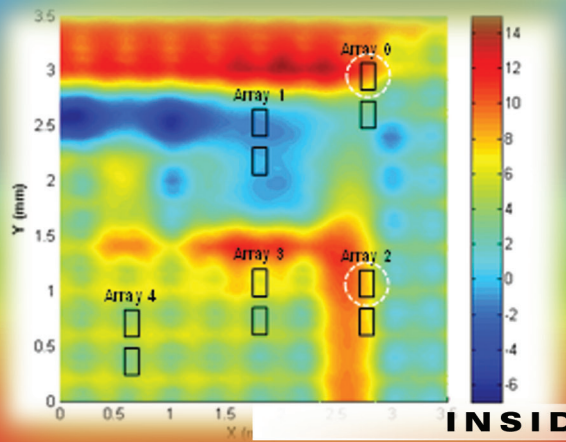
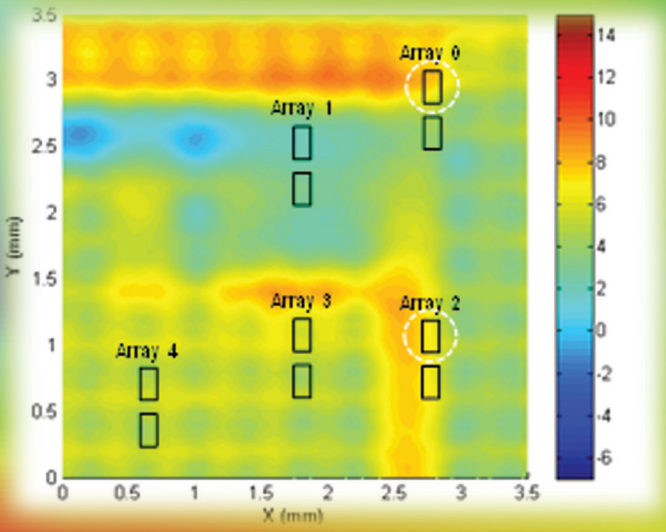
Chip Package Interaction (CPI)









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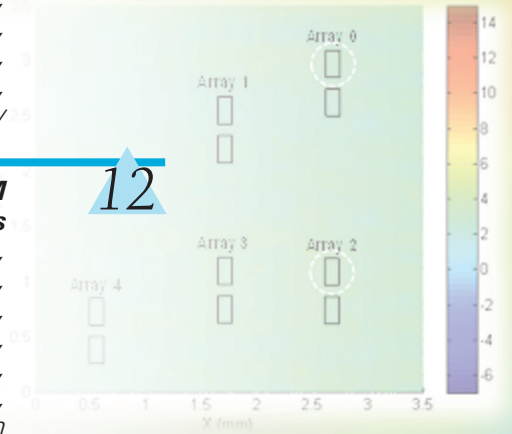

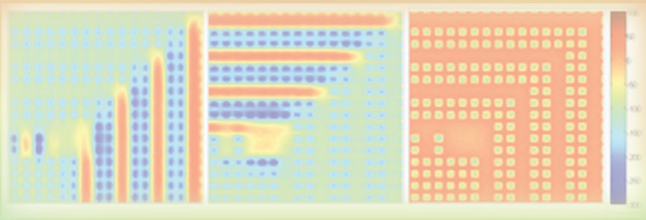

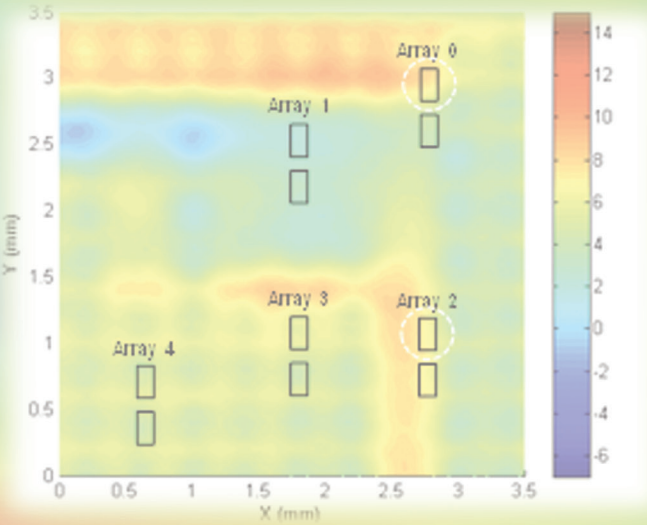

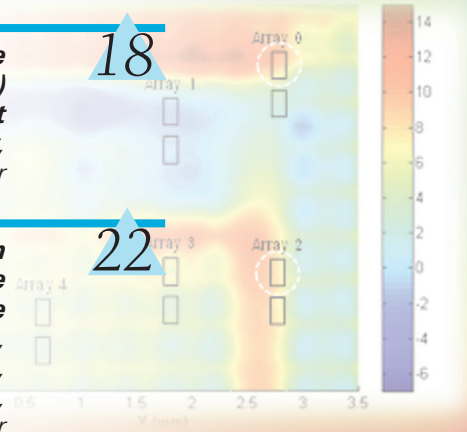

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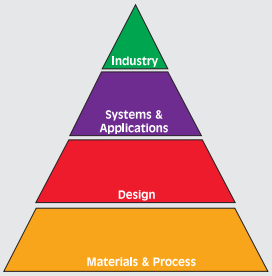

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IMAPS - International Microelectronics Assembly and Packaging Society
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FROM THE GUEST EDITOR

Chip-Package Interaction (CPI): An Industry Perspective

Dr. Urmi Ray
Vice President of Technology
STATS ChipPAC, Inc.

The last decade has seen an "electronics technology revolution" that can be compared to the industrial revolution for manufacturing in the eighteenth and nineteenth centuries. The ubiquitous use of smart phones and smart devices in all aspects of daily life, from entertainment to education, from ride sharing to rock and roll creation – mobile technology has completely transformed the "way we do things." And more interesting (a matter of major social science research), this change affects two-year old toddlers and nonagenarian grandparents. This revolution has opened the doors for fertile fields of innovation in mobile architecture, CMOS chips as well as how we "package and integrate" them. The primary requirements for consumers, (that is us), can be summarized as: light, small and stylish.

The trend towards smaller and lighter packages has created a "perfect storm" of possible CPI catastrophes and how the industry is staying ahead by innovation, forward looking research and smart, rational thinking.

What is this beast "CPI," you may ask. The loose definition goes like this: CPI is the interaction between the semiconductor package stresses and the semiconductor device (typically the CMOS die). Package stresses are caused by thermal, mechanical, or chemical mechanisms. Chip-package interactions contribute to various failure modes during package assembly as well as later in the field.

I would also highlight the different categories of interactions we should worry about. The first and foremost and probably most "known" in the packaging community is the mechanical CPI (mCPI). The typical culprits for this are thermal and mechanical stresses. Examples are CTE mismatch between the CMOS wafer/die and the organic package substrate, and/or the stresses associated with elevated temperatures during package assembly. The exacerbating factors are the use of advanced CMOS nodes where increasingly lower-k dielectric materials used during back end of line (BEOL) interconnect fabrication, extremely thin (sometimes thinner than 100 microns) die processing and handling, harder bumps with the emergence of copper pillar structures and many more. The reliability and yield failure risks are for bump cracking or fatigue, low-k dielectric layer delamination, etc.

The second "less well known" issue is electrical CPI (eCPI). These are the emerging trends with advanced CMOS nodes and ultra-thin wafer processing mentioned before, but now the mechanical stresses and strain could be transmitting to the transistors and sensitive circuits, thereby potentially impacting the performance of the product. The effects are much more subtle and hence difficult and expensive to predict and detect, since they require electrical testing, typically parametric characterization.

One other recent entry in the CPI field is due to the emergence of wafer level packaging (WLP) and fan out wafer level packaging (FOWLP). These package structures have offered unparalleled form factor and cost improvement by eliminating the package substrate. However, now we have lost the buffer layer of the organic package which provided a cushioning effect between the semiconductor die and the main printed circuit board (PCB). This has resulted in additional stresses being transmitted to the die during the surface mount assembly operation (wafer level package to PCB).

In this special issue of *Advancing Microelectronics* magazine we have chosen to highlight groundbreaking work in the different product and technology spaces that are affected by CPI. The 1st article will introduce us to another new threat as we adopt thinner packages and how to plan for staying ahead of the potential pitfalls. While this article focuses on relatively small package sizes, the other three articles are in the "large body size" product category. I hope you will enjoy the diverse perspectives of the 2nd article dealing with complex 2.5D integration of FPGA and high bandwidth memory (HBM) packages, followed by the 3rd article on 14nm CPI integration challenges. And we round off the discussions with the last article dealing with next generation Intel Xeon architecture.

I hope you enjoy this issue and the articles we have compiled for you. Please give us your feedback. What do you want to talk about? What do you want to read in the next issues?

Happy holidays to all of you.

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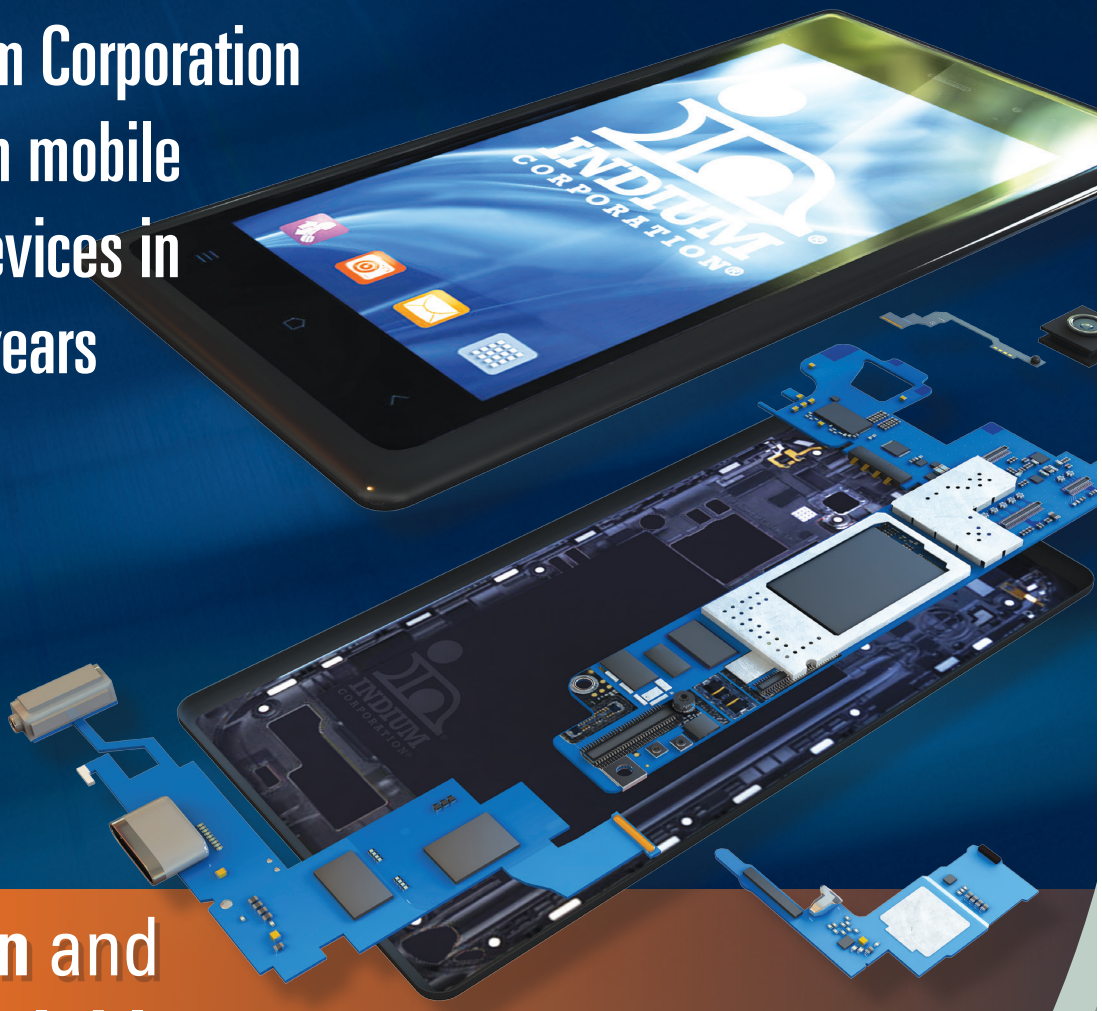

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Electrical Chip-Board Interaction (e-CBI) of Wafer Level Packaging Technology

Wei Zhao, Mark Nakamoto, Karthikeyan Dhandapani, Brian Henderson, Ron Lindley, Riko Radojcic, Aurel Gunterus, Mark Schwarz, Ahmer Syed, Vidhya Ramachandran

Qualcomm Technologies, Inc., 5775 Morehouse Drive, San Diego, CA 92121

and

Urmi Ray, STATS ChipPac Inc., 46429 Landing Parkway, Fremont, CA 94538

Email: weizhao@qti.qualcomm.com

Abstract

Electrical Chip Board Interaction (e-CBI) has emerged as a new risk in chip design as silicon die can directly interact with printed circuit board (PCB) in substrate-less wafer level packaging technology. To assess this risk Qualcomm Technologies, Inc. has converted an existing test chip to wafer level packaging technology. Both the measured data and simulation results show that e-CBI risk is significant and must be carefully managed.

Key words

chip-package interaction, modeling, mechanical stress, underfill, WLP/FOWLP

1. Introduction

Chip packaging is essential in today's semiconductor chip manufacturing, as it enables connections from chip to PCB and prevents physical damage and corrosion. However, there is mismatch in coefficients of thermal expansion (CTE) between silicon die and PCB in most consumer electronics products. The CTE of PCB is usually higher than the CTE of silicon. Accordingly, package materials in a flip-chip chip-scale package (FCCSP), including package substrate, underfill and molding compound, as shown in Figure 1, usually have been carefully chosen to have median CTE values to act as buffers between high CTE PCB and low CTE silicon die to protect ball grid array (BGA) solder joints. Nevertheless, as the package is cooled down from relative high process temperature (150~200°C), to low chip operating temperature (-40~110°C), CTE mismatch driven stress can be significant in both package and silicon die. Without proper design, high stress will lead to reliability issues, such as cracking of flip chip solder joints and delamination of low-κ dielectric layers in silicon die. As a result, mechanical chip-package interaction (CPI) is well-known and rigorously managed by the packaging community [1].

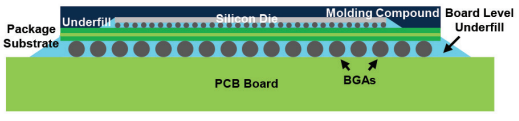

Figure 1. Structure of a FCCSP Package

On the other hand, stress engineering is essential in the state-of-the-art silicon technologies to boost transistor electrical mobility to enhance circuit speed [2]. Giga Pascal level of local stress has been intentionally and carefully introduced around transistors to increase mobility. However, the side effect is that transistors also respond sensitively to other unintentional stress sources, such as the earlier-mentioned CTE mismatch driven package stress. As a result, transistor characteristic deviates from silicon foundry models and wafer probing results, which most often catches chip designers by surprise. We call this emerging risk electrical chip-package interaction (e-CPI) [5].

e-CPI risk materializes in mobile application in recent years partly because silicon dies have been aggressively thinned down to reduce package form factors to meet consumer electronics demand. Naturally, the thinner the silicon die is, the more vulnerable it is to e-CPI risk. Common e-CPI stress sources include flip chip bump, die edges/corners and stacked dies [4], [5]. Those e-CPI stress sources can affect circuits near them by introducing parametric mismatches in analog circuits, and by adding extra overhead to process, voltage and temperature (PVT) corners in digital circuits. For both cases, e-CPI is a hidden price that chip designers may have to pay in terms of performance and/or yield.

So far, our discussions assume unintentional stress originates from package (e-CPI), while ignoring stress from PCB. This is a reasonable assumption for a FCCSP since silicon die in FCCSP is encapsulated by packaging materials and largely shielded from PCB board by package substrate. However, in recent years, there is a trend

to move packaging technology toward wafer level package (WLP) and Fan-Out Wafer Level Package (FOWLP) in order to reduce packaging cost and form factor. The basic structures of WLP and FOWLP packages are illustrated in Figures 2 and 3, respectively. One of the key differences between FCCSP and WLP/FOWLP is the presence or absence of package substrate. Without package substrate, silicon die in WLP/FOWLP will directly interact with PCB board. Evidently, the previous assumption of limited stress impact from PCB is no longer valid for WLP/FOWLP. Now we also have to evaluate the risk from PCB stress and we call this new risk electrical chip-board interaction (e-CBI).

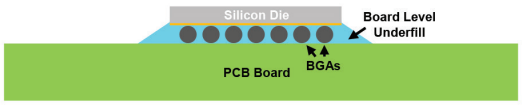

Figure 2. Structure of a WLP Package

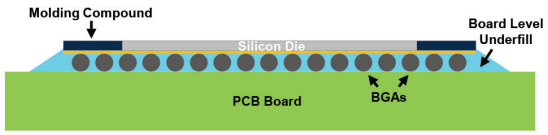

Figure 3. Structure of a FOWLP Package

2. Background

2.1 Piezoresistance Effect

The piezoresistance effect in silicon transistors is the change in channel mobility of a MOS transistor modulated by mechanical stress. Specifically, transistor mobility shift is a weighted average of stress components. There are three stress components. They are in-plane stress components which are either parallel (S_{xx}) or perpendicular (S_{yy}) to the transistor current flow direction, and out-of-plane (S_{zz}) stress component. The relationship between mobility shift and these stress components can be approximated as the equation,

$$\Delta\mu\,(\%) = S_{xx} \cdot P_x + S_{yy} \cdot P_y + S_{zz} \cdot P_z$$

where Δμ is the mobility shift, P_x, P_y, P_z are piezoresistance coefficient values in respective directions [2]. These values can be obtained from band simulations [6] and/or from empirical measurements (4-points bending; Z-axis indenting). Finite element analysis (FEA) simulations can calculate values of stress components. Using the above equation, we can further convert values of stress component to transistor mobility shift.

Since transistor mobility shift is largely proportional to current shift ΔI, especially for long channel transistors, we can track stress change by monitoring transistor current shifts. In our test chips, there are five pairs of transistor arrays which are used as stress sensors. Each pair consists of 16x4 transistors packed in an area of 124 x 241μm as shown in Figure 4. Such arrangement provides high spatial resolution data, while at the same time covering reasonably large areas. The transistors are P-type, which are highly sensitive to stress components S_{xx} and S_{yy}, but not sensitive to S_{zz}.

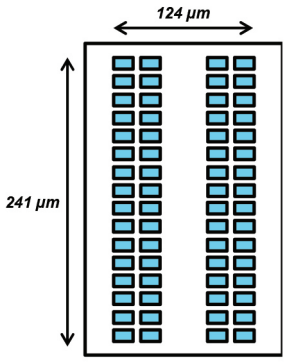

Figure 4. Transistor Arrays as Stress Sensors

2.2 Emerging of e-CBI Risk

Both WLP and FOWLP are wafer level packaging technologies. As discussed earlier, they utilize fewer packaging materials than FCCSP, including package substrate, underfill between silicon die and package substrate, and molding compound. It not only enables cost saving due to its simplified process steps, but also reduces Z-height of the entire package. WLP has already been adopted for many product lines of Qualcomm Technologies, Inc., including power management integrated circuits (PMIC) and RF Transceivers (WTR) chips. The major limitation of WLP is that silicon die size is limited to be within 6 × 6 mm to prevent board-level reliability (BLR) issues of BGA solder joints. Compared to FCCSP, wafer level packaging technologies can afford relatively thick silicon die thickness.

FOWLP is similar to WLP, but it can accommodate a larger die as it allows fan-out and more space for BGA connections. To achieve this, there is a ring of molding compound surrounding silicon die in FOWLP to serve as fan-out areas (Figure 3). It also has more and thicker RDL layers than WLP to enable complex routing for high-end mixed signal/digital chips. Now there is an industry-wide effort to aggressively move toward fan-out wafer-level packaging, even for large high-end chips. As wafer level packaging technologies become a popular choice, e-CBI risk can no longer be taken lightly, and managing it becomes a mandatory requirement for future design success.

2.3 Test Chip

To evaluate e-CBI risk, one of our existing test chips originally designed for FCCSP has been modified and implemented in FOWLP. To simulate a large die, the wafer was diced such that 1 whole die plus 3 partial die were combined to form a single large test chip for packaging. The five pairs of transistor arrays are located within a small area highlighted by the red box in Figure 5. The die thickness of the test chip is 160μm. Since we are interested in the chip-board interaction, the pattern of BGA balls between silicon die and PCB board as shown in Figure 5 is a critical factor. This interaction will be explained in detail in section 3. Note that there are regions and rings in which BGA balls have been depopulated for various reasons.

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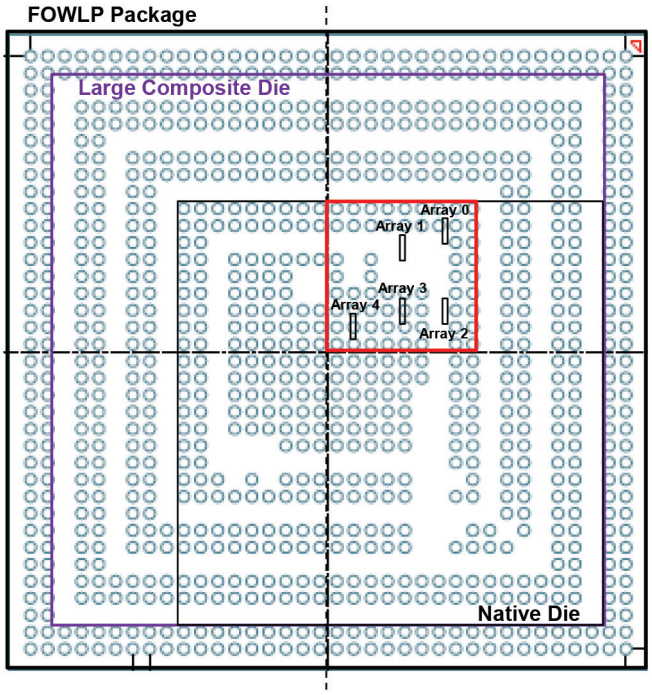

Figure 5. Placements of Transistor Arrays and Patterns of BGA Balls

3. Results and Discussions

3.1 Test Flow

Three steps testing flow have been designed to rigorously monitor e-CBI impacts as shown in Figure 6. The same parts have been measured in each step and part by part comparisons done after all three steps, so that other factors, such as silicon process variations, do not obscure the results.

The first step is the component level socket test, which, due to the package substrate, is usually sufficient for e-CPI analysis. Note that for this study the major stress sources of e-CPI, including flip chip bump, die edges and stacked dies, are not relevant. In this study, the results from the socket test is to establish a baseline for further studying the e-CBI effect introduced in the next two steps.

At the second step, the component has been mounted to PCB, but board level underfill has not been applied. At this step, the distance to neutral point (DNP) stress effect is the dominant stress mechanism. DNP stress largely manifests itself in out-of-plane (S_{zz}) stress component. This can create problems for N-type transistors. Since our stress sensors are P-type transistors and DNP is a well-known effect, we will not further discuss DNP effect and its e-CBI impact in this study.

In the third step, board level underfill has been dispensed between silicon die and PCB. A popular board level underfill compound (UF-A) is used in this study. This material is a common choice for board level underfill because of its good BLR performance. At this step, the CTE mismatch between BGA solder and board level underfill becomes the dominant stress source.

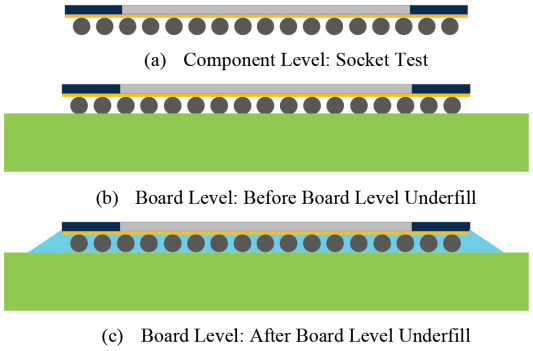

Figure 6. Three Steps Test Flow

3.2 Dominant e-CBI Stress Sources

Even before evaluating the testing results, visual inspections of the parts revealed interesting findings. Distinct dimple patterns at the backside of the parts emerged after board level underfill (Figure 7). Later analysis soon found that these dimple patterns correlate with the patterns of BGA depopulation. More specifically, the dimples occur only when BGA balls have been depopulated. The CTE of board level underfill is usually higher than that of BGA solder. In the absence of the mechanical support from BGA solder balls in the depopulated areas, the board level underfill shrinkage pulled the thin silicon die towards PCB. The FEA models later have verified this phenomenon and reproduced similar dimple. Since silicon die bends toward PCB in the dimple or BGA depopulated regions, tensile stress is created on active silicon surface. This has also been confirmed by FEA models. Figure 8 shows S_{xx}, S_{yy}, and S_{zz} in the upper right quarter of the test chip. While the background or average S_{xx}/S_{yy} is compressive due to the high CTE of board level underfill and PCB, the S_{xx}/S_{yy} stress in the dimple or BGA depopulated regions is tensile. As a result, the largest stress gradient of S_{xx}/S_{yy} is at the transition regions between BGA depopulated and non-depopulated areas. The stress gradient of S_{xx}/S_{yy} also overshadows the stress gradient of S_{zz}. In summary, a new e-CBI mechanism, local die bending induced by BGAs depopulating after dispensing board-level underfill, has been identified.

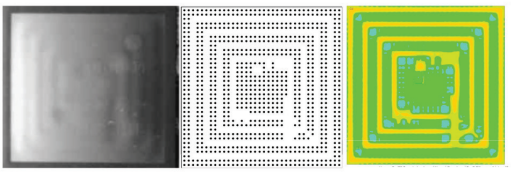

Figure 7. BGA Pattern Driven Local Die Bending, from Left to Right: Visual Dimples, BGA Pattern, and Simulated Strain

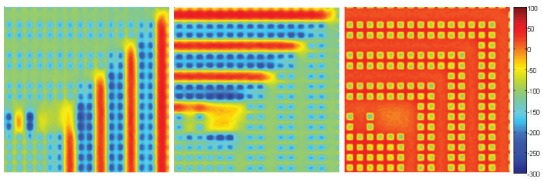

Figure 8. Stress Components in MPa in the Upper Right Quarter Region of the Die

One common question is why this effect is not as obvious in the flip chip bumps depopulation case in FCCSP. Flip chip bump underfill cannot bend silicon die towards package substrate effectively because the combined thickness of silicon die and molding compound cap is usually larger than the thickness of flip chip bump underfill. In this case, the thickness of board level underfill is, on the other hand, larger than the thickness of silicon die, and thus it can bend silicon die toward PCB more considerably.

Another question is if depopulating BGA balls will affect FCCSP packages after board level underfill. This is not likely for two reasons. First, the package thickness of FCCSP excluding BGAs is usually larger than 500µm, compared to the silicon thickness of only 160µm in this case. It is more difficult to create local bending in a thicker package. Second, the bending produces highest stress on package surfaces. Since the silicon die is somewhere in the middle of a FCCSP package, it will have very limited bending stress.

3.3 Silicon Data vs. FEA Simulation Results

3.3.1 Measured Data from Transistor Arrays

As mentioned earlier, there are five pairs of transistor arrays. Each pair has an upper array and a lower array. Table 1 summarizes measured transistor current mismatch values in percentage for each array at three test steps. As expected, the mismatches in some of the arrays increase sharply after dispensing board level underfill.

Array	Pair	Socket Test	Before Board Level Underfill	After Board Level Underfill
0	Lower	1.6	1.7	4.2
	Upper	2.4	2.2	5.9
1	Lower	1.4	1.4	1.6
	Upper	2.2	2.0	6.2
2	Lower	1.9	1.8	3.1
	Upper	1.3	1.4	3.6
3	Lower	2.3	2.4	2.5
	Upper	2.3	2.3	3.8
4	Lower	2.2	2.3	2.1
	Upper	1.5	1.6	1.4

Table 1. Summary of Measured ΔI Mismatch (%)

3.3.2 FEA Simulation Results

Figure 9 shows FEA simulation results of PMOS current shift of the red box region highlighted in Figure 5, before and after board level underfill. The simulation results match well with the measured data. For example, the upper pair of Array 0 and Array 2 as highlighted by white circles are near the transition regions between BGA depopulated and non-depopulated areas, so they will see a sharp increase in mismatch after board level underfill. In contrast, Array 4 sees little change in mismatch as it is in a region with dense BGA balls. These simulation results are confirmed by the measured data shown in Table 1.

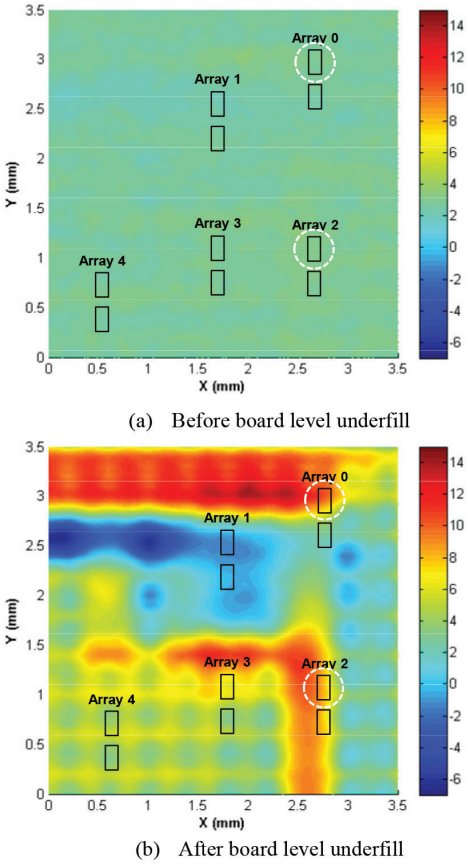

Figure 9. Simulated PMOS Current Shift (%)

3.3.3 Simulation Results vs Measured Data

Figure 10 shows the measured mismatch in the three test steps for the upper pair of Array 0 (left) and Array 2 (right). The mismatches are small for the first two test steps, but show a strong pattern after board level underfill. Figure 11 shows the simulated mismatch after board level underfill. The simulated patterns agree well with the measured patterns.

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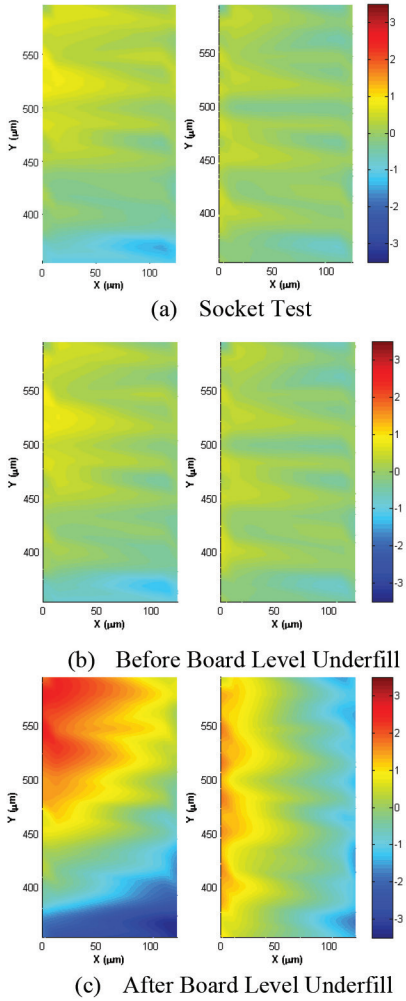

Figure 10. Measured Mismatch (%) in Three Steps

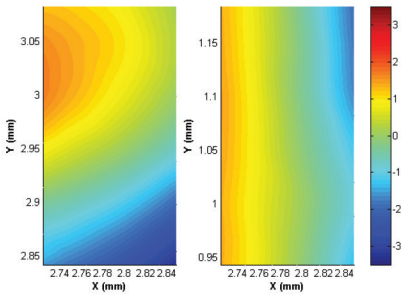

Figure 11. Simulated Mismatch (%) After Board Level Underfill

3.4 Choices of Board Level Underfill

3.4.1 Simulation Results vs Measured Data

To compare results between different underfills, another board level underfill, UF-B, is also tested in this study. UF-B has lower T_g and lower CTE than UF-A. Both the measured data and simulation results show UF-B produces less e-CBI impact than UF-A (Figures 12, 13, 14 and Table 2). This is largely because UF-B has lower CTE, and thus lower CTE mismatch induced stress.

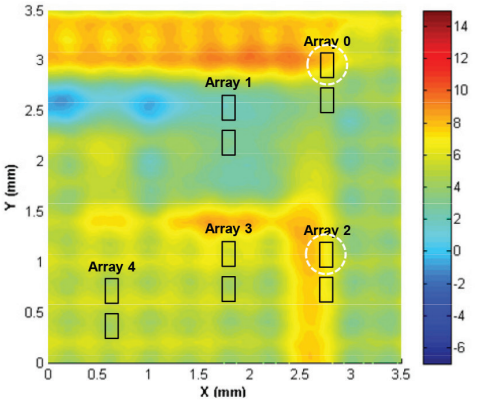

Figure 12. Simulated PMOS Current Shift (%) with UF-B

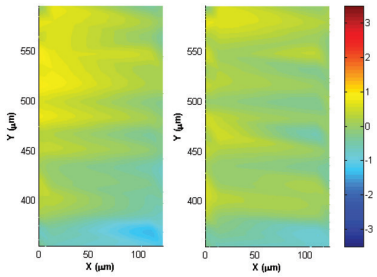

Figure 13. Measured Mismatch (%) with UF-B

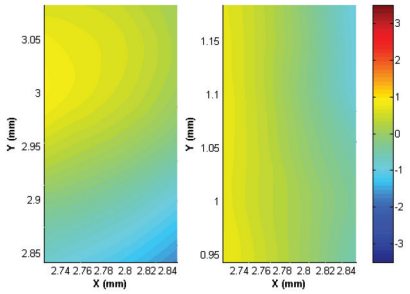

Figure 14. Simulated Mismatch (%) with UF-B

Array	Pair	UF-A	UF-B
0	Lower	4.2	1.8
	Upper	5.9	2.3
1	Lower	1.6	1.2
	Upper	6.2	2.2
2	Lower	3.1	1.6
	Upper	3.6	1.5
3	Lower	2.5	2.0
	Upper	3.8	1.8
4	Lower	2.1	2.7
	Upper	1.4	1.7

Table 2. Summary of Measured Mismatch (%) After Board Level Underfill

3.4.2 Complications of Managing e-CBI

e-CPI and e-CBI as their names imply are interactions between silicon process, circuit design, chip floorplan, package design, package process, and now PCB and assembly process for e-CBI. Their impacts are not predictable when looking in isolation at any of the above domains. Managing them most often requires coordination and often co-design efforts.

For e-CPI in FCCSP, the package substrate isolates the chip from the PCB so that the management of the issue can be contained in the chip component house. On the other hand, for WLP and FOWLP, e-CBI becomes significant. As demonstrated in this work, decisions made at the system houses, such as the choice of board level underfill, can have a major impact on the stress imparted to the die.

It is also not as simple as choosing a board level underfill optimized for e-CBI, since there are trade-offs with other primary purposes of the underfill, such as protecting the BGA balls from damages due to thermal cycling and/or drop shock. Most often this produces conflicting demands which require engineering trade-offs to resolve.

To manage these risks, the industry needs to raise awareness of these interactions in the silicon process, design and packaging domains. Flows and strategies are needed to anticipate these and resolve them in the development phase. Modeling and characterization of both silicon and package are also critical for establishing design rules, process developments and risk assessments. A more complete discussion of these enablements/infrastructures can be found in various papers [3]–[5].

4. Conclusion

e-CBI emerges as a new risk in substrate-less wafer level packaging technology for today's mobile applications. A test chip has been converted to study this new risk. A new e-CBI mechanism, local die bending induced by BGAs depopulating after board-level underfill, has been identified. Both the measured data from transistor arrays and FEA simulation results have demonstrated that it is a real and serious risk. And the choice of board level underfill is critical in determining e-CBI impact.

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2.5D FPGA-HBM Integration Challenges

Jaspreet Gandhi, Boon Ang, Tom Lee, Henley Liu, Myongseob Kim, Ho Hyung Lee, Gamal Refai-Ahmed, Hong Shi, Suresh Ramalingam
Xilinx Inc.
2100 Logic Dr., San Jose, CA 95124
Ph: 408-879-3645; Fax: 408-371-0541
Email: jgandhi@xilinx.com

Abstract

FPGA partitioning and high density integration using interposer-based 2.5D stacked silicon interconnect technology (SSIT) has been pioneering work at Xilinx for several years enabling advanced applications in high performance computing, networking, hyper scale data center and cloud services, etc. With the insatiable demand for acceleration workloads, FPGAs need to be coupled within package memory to enable higher bandwidth, lower power and smaller form factor architecture. 3D stacking-based high bandwidth memory (HBM) has paved the way to realize such applications providing 10X higher bandwidth, 4X lower power vs DDR4. This paper provides an overview of unique challenges involved with 2.5D FPGA-HBM SSIT integration from design, process/package development, test and reliability point of view.

Key words

2.5D, FPGA, HBM, machine learning, packaging, SSIT, TSV

I. Introduction

There is little doubt that this is a new era for FPGAs (Field Programmable Gate Array). While it is not news that FPGAs have been deployed in many different environments, particularly on the storage and networking side, there are fresh use cases emerging in part due to much larger datacenter trends. Energy efficiency, scalability, and the ability to handle vast volumes of streaming data are more important now than ever before. At a time when traditional CPUs are facing a future where Moore's Law is less certain and other accelerators and custom ASICs are potential solutions with their own sets of expenses and hurdles, FPGAs are being deployed as CPU accelerators for an ever-growing range of workloads in machine learning, search engine indexing, encryption, and data compression providing high performance/watt [1]. These parallel data processing and compute-intensive applications are relying on high density FPGA architecture integrated within package memory to provide faster speed, higher bandwidth at lower power.

Xilinx already has a leap forward in new and high growth markets and applications such as datacenter, storage and networking creating high-capacity FPGA devices with second generation 3D SSIT (Figure 1). This technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with several thousand low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs.

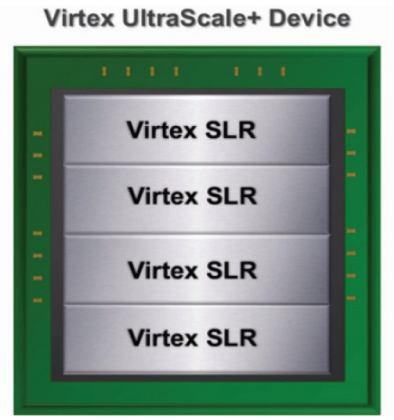

Figure 1. Virtex Ultra Scale+ Device using 3D SSIT.

On the DRAM side, thanks to the advent of High Bandwidth Memory (HBM), the memory wall has been broken to achieve multi-Tbps memory bandwidth at significantly lower power. HBM is a new type of memory integration technology that vertically stacks memory chips via TSVs (thru silicon vias) providing low power consumption, ultra wide communication lanes, faster speed and smaller form factor. Xilinx recently announced HBM-enabled 16nm UltraScale+ FPGAs (Figure 2) built using 3rd generation CoWoS technology co-developed by TSMC and Xilinx and now the industry standard assembly for HBM integration. These heterogeneously integrated packages can deliver 10X bandwidth per HBM stack, 4X lower power vs. DDR4.

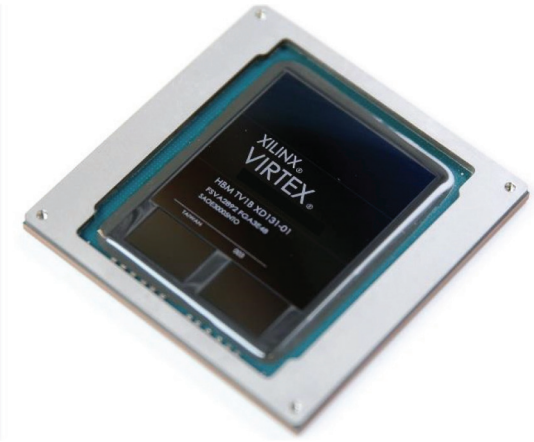

Figure 2. Xilinx Ultrascale+ FPGA-HBM Integration.

Several publications recently have highlighted heterogeneous integration approaches for HBM in SiP applications. AMD's 2.5D Si interposer approach talks about the importance of stiffener ring materials, adhesive, thickness and substrate core type to improve package co-planarity [2]. Cisco/e-Silicon [3] used organic interposer for ASIC and memory integration. The low loss dielectric material used for the organic interposer allows ultra-fine line spacing (Line/Spacing = 6µm/6µm), low transmission loss and high insulation reliability. Intel's Multi-Die Interconnect Bridge (EMIB) [4] is an interposer less approach with claims to have no practical limit to die size and can leverage existing organic substrate manufacturing. Regardless of the pros and cons of each approach, heterogeneous integration of HBM with ASIC, GPU, CPU, FPGA is real and progressing very fast. To the authors' knowledge, Xilinx is the first company to attempt HBM integration with partitioned FPGAs in 2.5D format. This paper provides an overview of unique challenges involved with 2.5D FPGA-HBM SSIT integration from design, process/package development, test and reliability point of view.

II. Interposer Design

The integration of HBM cubes and FPGA dice into a SSIT package begins with the design of the silicon interposer. Physical layout considerations and electrical requirements are of paramount importance. The first physical consideration is the placement of the FPGA dice and HBM cubes on the interposer. This is determined by several factors such as underfill dispensing, thermo-mechanical stress on interposer, interposer size and inter-die signal integrity. There is an optimal die-to-die distance to achieve a uniform and void-free underfill during package assembly which further means the gap has to be small (for single underfill dispense) or large (for multi-pass dispense). As for the stress on interposer, it can be influenced by the amount of open space left on the interposer after the dice are placed. The underfill or mold compound occupying this open space will impact interposer warpage. If the HBM cube dimensions differ from one memory supplier to another, a different interposer may be necessary to satisfy the FPGA to HBM die gap requirements.

Another physical consideration is the ubump pitch on FPGA PHY and HBM PHY. While there is an industry specification (JEDEC) for HBM ubump pitch, the ubump pitch on FPGA is vendor specific. For ease of interposer routing, the ubump pitches across these 2 dice should match in such a way that an integer number of inter-die signal lines can be routed in a uniform fashion between a pair of ubumps. Such uniform routing is also desired from a signal timing point of view. Since the signals between FPGA PHY and HBM PHY are operating at Gbps level, the layout of these interconnect routings in the interposer has to be done carefully so as not to compromise the signal integrity. To optimize these routings, their length has to be kept as short as possible and with low resistance. This usually means placing FPGA PHY and HBM PHY side-by-side facing each other and with a small die gap as discussed earlier. Besides this, allocating sufficient metal routing layers in the interposer will help to achieve optimal routing. In addition to minimizing routing length and resistance, careful shielding of the high speed signal lines is required to minimize electrical cross-talk. Meticulous post-layout simulations of these inter-die signals must be carried out to confirm the electrical specifications. HBM cube comes with a set of direct access (DA) ports which have to be routed to BGA balls. As the name imply, they offer a direct electrical access to the HBM memory and are used by memory vendors to debug any HBM issues (RMA). The design of these ports are vendor-specific and some may operate at high frequencies. Therefore, attention should be given when routing these DA signals through the interposer to BGA terminals. A straightforward routing will be to use a set of stacked vias in the interposer to connect the DA ubumps to the BGAs.

III. Package Design and Process

Packaging solutions for 2.5D FPGA SSIT devices have been developed and demonstrated in Xilinx's last two generations' product (28nm and 20nm). Thermal-mechanical simulation and test vehicle evaluation have provided greater insight into package design with optimized thermal interface material, lid structure, lid adhesive, substrate structure and core/build-up material for robust reliability performance in both component and board levels [6].

With 2.5D FPGA-HBM integration in the current 16nm product, additional design and process requirements have presented new packaging challenges. The major changes are: (i) C4 bump structure moving from eutectic solder bump to Cu pillar bump (CPB) with Pb-free solder; (ii) lid type moving from regular copper forged lid to stainless steel stiffener ring. CPB has advantages for fine pitch interconnect, bump reliability, and pkg. thermal performance, however, high Tg underfill is required which often increases package stress and reliability concern due to increased die-to-package interaction (DPI). Typical failure modes include C4 underfill delamination, FPGA die gap delamination, FPGA ubump voiding, etc. Continued process optimization such as proper underfill material selection (for both ubump and C4 bump), C4 underfill curing, interposer dicing, etc. can help to improve DPI performance. A stainless steel-based stiffener ring is required for FPGA-HBM SSIT device due to a more stringent thermal budget. The implementation of a stiffener ring not only has cost advantages, it also eliminates the thermal interface resistance between lid and die and provides a direct thermal path to the heat sink or other effective cooling solutions.

The combination of CPB and stiffener ring has an adverse impact on package coplanarity also. Efforts are made to not only reduce package coplanarity at room temperature, also reduce package warpage at high temperature (240-260C) in order for system house to properly attach

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the SiP component on the board. Using a thicker and lower CTE core material for the substrate results in major improvement for package coplanarity, however may have an adverse effect on BGA ball board level reliability due to increased CTE mismatch between package substrate and system board material. More studies are currently underway to evaluate this concern. A proper stiffener ring design along with an adequate adhesive material is required to improve overall package coplanarity. In general, a thicker ring with wider foot will help to increase the rigidity of the package and therefore reduce its warpage, however, the thickness of the ring may impact heat sink assembly, while the ring foot width will affect the keep-out area between ring and chip capacitors. All these factors need to be incorporated into the overall package design.

Precise control of bare die parallelism and flatness in the FPGA-HBM package is also required to enable adequate heat sink (or other cooling solutions) attachment and minimize second-level thermal interface resistance. In the current industrial practice, assembly houses often only measure and control lid tilt and package coplanarity as part of the assembly specifications. Parallelism and flatness (either on lid for lidded package or on bare die for stiffener ring package) are mostly being ignored. Efforts are needed with assembly houses to prioritize this measurement and incorporate it in their key performance indicators (KPI) to meet product specifications.

Challenges for Package Coplanarity

The stiffener ring scheme can reduce package coplanarity (COP), but it is not enough for a FPGA-HBM integrated package. The following approaches are used to reduce coplanarity more; lower CTE substrate, stiffener ring type and size etc. Estimated coplanarity results are presented with various parameters. The coplanarity value is predicted by the simulated package warpage result. Figure 3 is the lidless package image used for the simulation. There are 3 FPGA dies and 2 HBM dies on the interposer. The simulated package coplanarity results are presented in Table 1. Wider ring width or thicker ring is better to reduce the coplanarity. Partitioned FPGA die type **(Figure 4)** is better for lower coplanarity than a big single FPGA die as shown in Table 2.

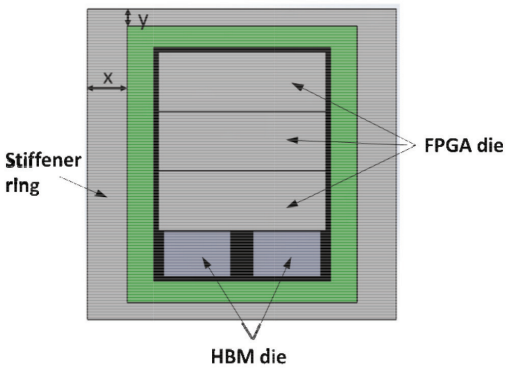

Figure 3. Sample image of FPGA-HBM integrated package: X dimension is the wider side and Y the narrow side of stiffener ring.

Ring thickness (Z, mm)	Ring thickness A- 0.2mm	Ring thickness A	Ring thickness A+ 0.2mm
COP (mil)	12.4	11.5	11.1
Ring width (X, mm)	Ring width A- 1mm	Ring width A	Ring width A+ 1mm
COP (mil)	12.5	12.1	11.5

Table 1: Simulated Coplanarity Results by Stiffener Ring Width and Thickness

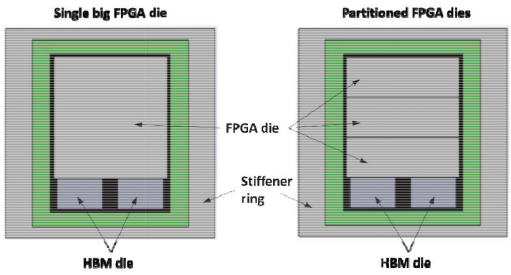

Figure 4. Simple image of FPGA-HBM integrated package by FPGA die types.

FPGA die type	Single die	Partitioned dies
COP (mil)	11.9	11.5

Table 2. Simulated Coplanarity Results by FPGA Die Type

Coplanarity can be also changed by substrate core CTE. Table 3 is the comparison table with substrate core CTE. The substrate with lower CTE core shows lower coplanarity. This result is aligned with measured data (Figure 5) where lower CTE substrate core B shows 1.1mil ~ 1.3mil lower coplanarity than the higher CTE core A.

SBT core	Higher CTE	Lower CTE
COP (mil)	12.1	11.5

Table 3: Simulated Coplanarity Result by Substrate Core Type

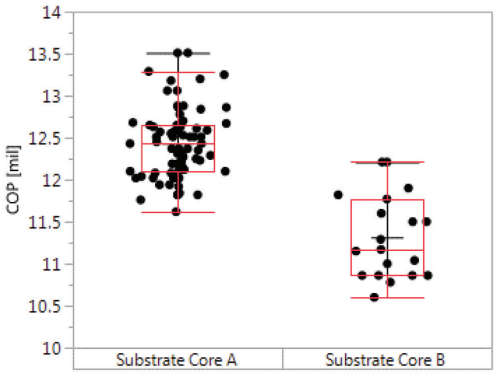

Figure 5. Coplanarity comparison by substrate core.

The coplanarity can also be reduced by ring type. Figure 6 shows the measured coplanarity data with different ring patterns. Pattern A is a general flat pattern while pattern B is a specially designed ring pattern to enhance adhesion. The package with pattern B reduces coplanarity by 0.5mil ~ 0.7mil. Maximum coplanarity can be reduced to 10.8mil.

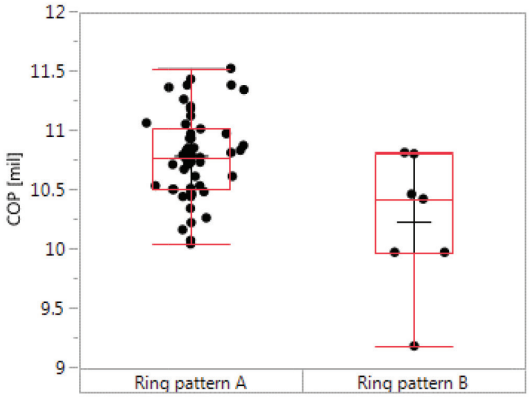

Figure 6. Coplanarity comparison by stiffener ring pattern.

Challenges for C4 Joining

One of the major process challenges for 2.5D HBM is C4 joining. With HBM and the empty area around HBM on the interposer, the CoW or CoC die with HBM and FPGA combined has higher warpage than the die with multiple FPGA dies without HBM. This higher die warpage in turn results in either C4 cold joint or C4 bridging. Compared to the other 2.5D HBM-SoC integrations reported so far, Xilinx 2.5D HBM-FPGA integration has the unique challenge that FPGA slice may cover 2 corners of a super-large interposer (Figure 1) with tighter C4 pitch than HBM. Limited number of C4 are required for HBM DA (direct access) ports and power/ground pins connected directly to substrate BGA pins. Thus, the C4 pitch under HBM can be more relaxed. On the other hand, FPGA slice may have tighter C4 pitch at corners. In addition to the C4 pitch challenge, another different factor is the die warpage behavior. FPGA-2 HBM CoW or CoC die has different warpage curvature than a SoC-4 HBM die. A typical 2.5D HBM-SoC integration either has 4 HBM at 4 corners in a super large interposer, or has 2 HBM in a relatively smaller interposer since there is no partition in SoC die.

To address the C4 joint challenge within the confines of CoW or CoC die warpage, the C4 bump and substrate pre-solder size need to be optimized first. A smaller C4 bump size reduces the risk of C4 bridging, but increases the risk of cold joint, so certainly there is a trade-off here. Reducing CoW or CoC die warpage is another way to prevent C4 joining issues. Table 4 shows the difference in die warpage due to different ubump underfill material. Figure 7 shows typical CoW warpage profile at room and reflow temp.

uBump underfill	UF#1	UF#2
Die warpage (um) at 250C	70	50

Table 4: Actual Cow Die Warpage Results from Two Different Ubump Underfill Materials

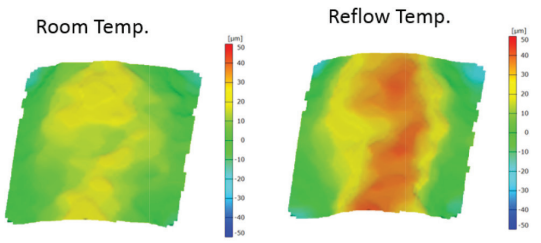

Figure 7. Typical FPGA-HBM CoW die warpage profile at room and reflow temp.

IV. Test Hardware and Mechanical KPIs

The FPGA-HBM package under development, even though it has a similar size as earlier generations, requires several modifications for the test hardware. Optimum stiffener ring footing is required for the test handler to impart sufficient contact force to the package pins during testing. The tradeoff could be reduced space for decoupling capacitors and higher package stress. Another important consideration as touched upon in the interposer design section above is BGA pin mapping. HBM DA port functionality and assignment vary from vendor to vendor so even though HBM is a JEDEC standard, a different substrate design may be required while switching vendors to ensure DA ports are routed and assigned correctly through the interposer connecting to substrate. These considerations must be given serious thought before releasing a test board design.

With a stiffener ring package, die flatness and parallelism are new mechanical KPIs that need to be considered to ensure thermal enhancement. The thickness of TIM (thermal interface material) between component and thermal management solution (heat sink) is one of the critical factors for thermal extraction performance which further depends on package flatness and parallelism. These new KPIs are measured with components before BGA attachment process. Sample is placed on the flat surface and using either optical sensor or mechanical probe, 9 data points of the top die surface profile are obtained. Flatness is defined by subtracting minimum from maximum value among 9 data points and parallelism is defined same way among 5 data points lying on the vertical and horizontal centerlines (data points 2,4,5,6 and 8 in Figure 8). These new KPIs also help external customers understand tolerances required for heat sink design.

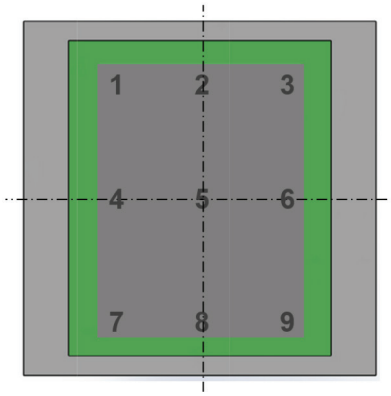

Figure 8. Schematic for die parallelism and flatness measurement.

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V. Reliability

The FPGA-HBM package was subjected to JEDEC MSL4 pre-conditioning where it passed 1000 hrs. HTS (High Temperature Storage) at 150C and 1000 cycles TCB (Temperature Cycle condition-B) at -55 to125C. ubump and C4 bump shape and profile looked normal after these tests (Figures 9, 10 and 11) with no physical abnormalities in the package. More tests are currently in progress.

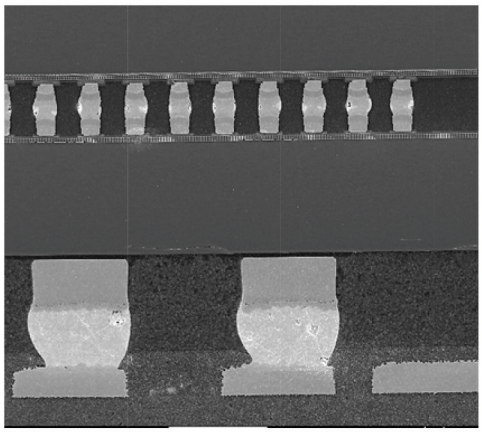

Figure 9. ubump and C4 bump after HTS 1000 hours.

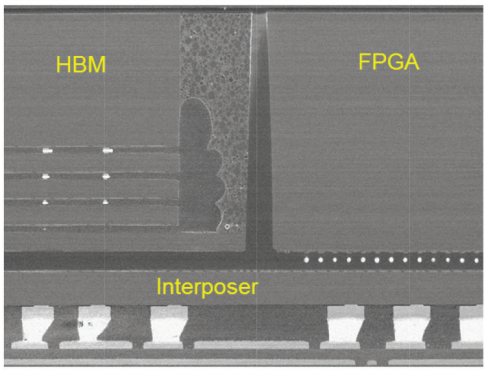

Figure 10. FPGA-HBM cross-sectional view after HTS 1000 hours.

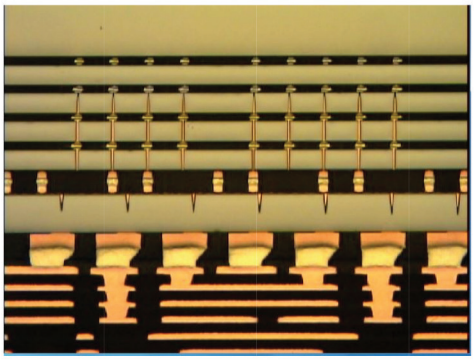

Figure 11. Cross-sectional view after TCB 1000 cycles.

VI. Conclusion

2.5D FPGA-HBM integration involves unique challenges which demand close knit collaboration between memory vendor, design/process/test and external customers. Several important factors were highlighted to achieve high yield, low coplanarity and robust reliability for 55X55mm2 FPGA-HBM heterogeneous package. Importance of design considerations for HBM swap and new KPIs such as package parallelism and flatness measurement were also underscored for a large size stiffener ring only package.

Acknowledgment

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14nm Chip Package Interaction (CPI) Technology Development

Lei Fu, YS Low, Milind Bhagavat, Ivor Barber
Advanced Micro Devices
7171 Southwest Parkway, Austin, TX 78735
Email: lei.fu@amd.com

Abstract

This paper presents the 14 nm chip and package interaction (CPI) challenges and development by using 140 um minimum pitch with SnAg bump in a flip chip BGA package. We evaluated 14 nm back end of line (BEOL) film strength/structure/adhesion with a large die size of 21x21 mm² and optimized bumping technology by passing all the CPI reliability tests (QTC, Precon, UBHAST, TCJ, MSL, and HTS) following the JEDEC standard. We also evaluated assembly with different bump footprint at 140um bump pitch with SnAg bump, and no assembly issues were encountered. Crack stop plays a very critical role in defending the crack propagation into the die active area. In our development, we observed reliability failure with severe test condition TCG (-45°C to 125°C), but passed TCJ (0°C to 100°C) with single wall crack stop on the large die size. With increasing crack stop width which enhanced the mechanical strength of the crack stop, both TCG and TCJ passed. So it is strongly recommended to use a wider crack stop for large dies to eliminate any failures.

Key words

chip package interaction (CPI), ELK, bumping, reliability, back end of line (BEOL), crack stop, test chip

I. Introduction

The increasing demand for advanced electronic devices, high density, high speed, low power consumption and more functions drives the scaling down of IC feature sizes [1]. Advanced CMOS node interconnect structure will have smaller dimensions and more layers to improve layout density, but will degrade interconnect RC delay which dominates the performance of the device. The semiconductor industry is now focusing its efforts on implementing extremely low K (ELK) porous dielectric materials (k < 2.5) into the back end of line (BEOL) to reduce the interconnect capacitance and cross-talk noise and enhance circuit performance [2]. Lower mechanical strength of ELK, along with increased die size, difference in effective coefficient of thermal expansion (CTE) between die and substrate, and the use of higher stiffness lead free solder increasingly contribute towards ELK layer cracking. In light of these developments, the industry has dedicated tremendous resources in modeling and experimental development work to understand the interaction between chip and package. Chip package interaction (CPI) became one of the critical reliability issues that needed to be addressed to avoid electrical or mechanical failure in products. When addressing CPI challenges, different areas have to be considered, ranging from silicon BEOL design and processing, bumping design and process, package assembly process, assembly bill of material (BOM), and substrate technology. As the industry faced several CPI-related failures over the last decade, CPI qualification became one of the prerequisites for technology qualification before a product tape-out.

This paper presents the 14nm CPI challenges and development by using 140 um minimum pitch with SnAg bump in a flip chip BGA package. We reviewed the state of the art of Far BEOL (FBEOL) work done by foundries, and assess CPI risk by using smaller UBM to meet 140um bump pitch assembly requirements. We evaluated 14nm back end of line (BEOL) film strength/structure/adhesion with a large die size of 21x21 mm² and optimized bumping technology by passing all the CPI reliability tests (QTC, Precon, UBHAST, TCJ, MSL, and HTS) as per the JEDEC standard. We also evaluated assembly with a different bump footprint at 140um bump pitch with SnAg bump without any assembly issues. Crack stop plays a very critical role in preventing crack propagation into the die active area. In our development, we observed reliability failure with severe test condition TCG (-45°C to 125°C), but passed TCJ (0°C to 100°C) with single wall crack stop on the large die size. With increasing crack stop width which enhanced the mechanical strength of the crack stop, both TCG and TCJ passed. Therefore we strongly recommend using a wider crack stop with large die to eliminate any reliability failures.

CPI Test Vehicle Configuration

In order to evaluate CPI risk and reliability concerns from a technology point of view, a CPI test vehicle (TV) must be designed and verified before any product tape out at each technology node. CPI test configuration must be included by using the same BEOL stacks, same ELK material, same BEOL process, same bump technology, same substrate technology, same assembly process for the production of the same Si node. In general, CPI TV with rep-

resentative of 14nm product lines must be designed. CPI TV die size should cover most of the future products' die sizes as a larger die size imposes higher CPI related-risk. In order to test the chip to package integrity, CPI TV must include several CPI macro structures that are electrically testable. For CPI risk assessment, it is well known that the distance to neutral point (DNP) is a critical factor. It is also widely known that higher DNP imposes higher CPI risk, so most of the CPI macro structures are predominantly located near the four die corners and periphery of the die. In each Si technology node, there are various package types planned to meet different market segment requirements. CPI evaluation cannot cover all the cases. So the worst case scenario has been defined in die size and the package selection to represent the highest CPI stress. The CPI macro structures inside the CPI TV are sensitive enough to measure any structural integrity impact during package assembly or reliability testing. In our 14nm CPI development, a 14nm TV with die size of 21x21 mm^2 with 140um bump pitch of SnAg bump has been selected. 40x40 mm^2 substrate has been used in our CPI technology qualification. JEDEC standard tests (Precon, UBHAST, TCJ, MSL, and HTS) are used as criteria for the CPI technology qualification. Quick thermal cycling (QTC) has been used to assess CPI margin for ELK material.

Results and Discussion

1. FBEOL review

During early development of BEOL with ELK dielectrics along with lead free bumping technology, ELK crack called white bumps were encountered as rigid lead free bumps would transfer more stress to weak ELK layers causing ELK crack underneath the bump [3]. Figure 1 shows a typical example of white bump. In order to solve the issue, foundries spent a lot of effort to improve the ELK mechanical properties with improving BEOL process or new higher strength ELK materials. There have been

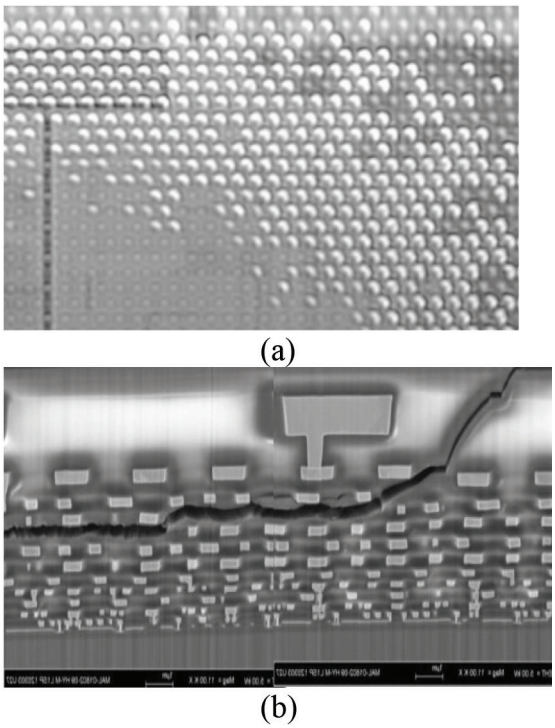

Figure 1. Images of ELK cracks: (a) CSAM pictures of white bumps indicating ELK crack; (b) FIB X-section showing ELK cracking.

improvements made in ELK strength, however ELK process is still marginal and ELK cracking is still encountered in some cases. In order to improve the CPI margin, many studies have been done including passivation thickness, polyimide thickness, under bump metallization, CTE of substrate, and FBEOL. Simulation and DOE have shown that by using thicker Aluminum terminal metal and two layers of passivation, the CPI risk reduced significantly [4]. So foundries have now implemented this dual passivation layer with Al terminal metal to enhance CPI reliability (Figure 2). Our 14nm CPI TV have implemented these FBEOL structures.

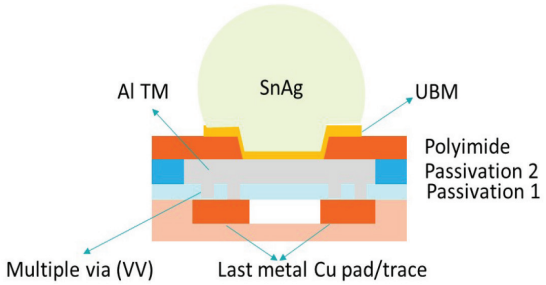

Figure 2. Dual passivation of FBEOL to reduce ELK stress.

2. Bump pitch effect and bump selection

With the shrinking of the transistor feature size, I/O count increases significantly. Therefore bump pitch must also be shrunk at the same time to allocate all the I/O and signal pins on the die. Simulation has shown that ELK stress reduces with reduced bump pitch. Figure 3 is the simulation summary of normalized max. ELK stress at different bump pitches indicating that smaller bump pitch will have a lower ELK stress which in turn lowers the CPI risk. It is well known that with bump pitch smaller than or equal to 130um, Cu pillar bump must be used to avoid a solder bridging issue. SnAg bumps are usually used with the bump pitch larger than or equal to 150um bump pitch. In our CPI TV, 140um bump pitch has been used and SnAg bump was selected for CPI evaluation due to the lower CPI risk and cost compared to Cu pillar.

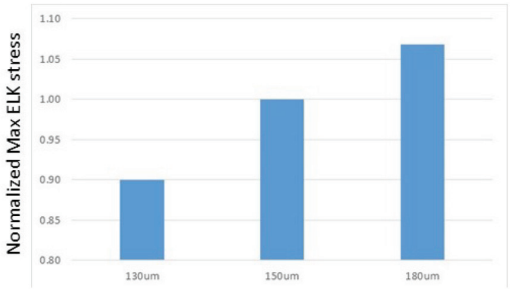

Figure 3. Normalized max ELK stress at different bump pitch.

3. Assembly development

Most CPI TVs use mixed bump pitch consisting of tight bump pitch at periphery area and larger bump pitch at center area. This arrangement can meet the requirement to assess CPI risk, but can't be used for the assembly development for production. So a new assembly TV is needed to development the assembly process before production.

continued on page 20

continued from page 19

In our 14nm CPI development, we combined both functions for CPI risk and assembly development. We applied a uniform 140um bump pitch across whole die area. In the regular product design, staggered bump pitch or regular vertical and horizontal pitch is used. In order to evaluate the impact of the bump pitch pattern, we designed the bump footprint with staggered bump pitch at the 1st and 4th quadrant, vertical and horizontal pitch at the 2nd and 3rd quadrant. Figure 4 shows the bump footprint.

The assembly results showed that there is no anomaly encountered during our assembly development. Both bump patterns (array and staggered) have not caused any issues like underfill voids, solder bridging and delamination. Figure 5 is the CSAM picture after assembly. Figure 6 is the X-ray picture of the bump after assembly. The results gave us very high confidence for using SnAg solder bump with appropriate bump size on our 14nm products.

4. Crack stop effect

Unlike bare silicon dies, thermal deformation of packaged dies can be directly coupled to Cu/low-k or ELK interconnects, inducing very high local stresses to drive fracture and delamination, especially when there are some defects existing such as dicing induced cracks, embedded process defects or poor low k/ELK adhesion. The maximum stress is always at the die corners. One of the typical CPI failures is inner layer dielectric (ILD) delamination at the die edge or die corner. ILD delamination is caused due to dicing defects like microcracks and poor adhesion or mechanical strength of low-k/ELK dielectric materials under the thermal load of the processes like flip-chip assembly process or thermal cycling tests.

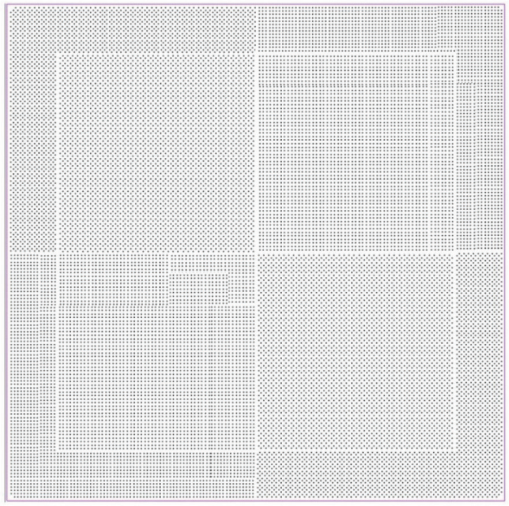

Figure 4. 14nm CPI TV bump footprint.

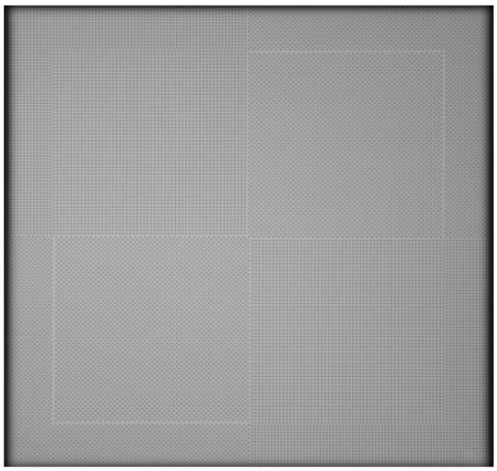

Figure 5. CSAM picture of 14nm CPI TV after assembly.

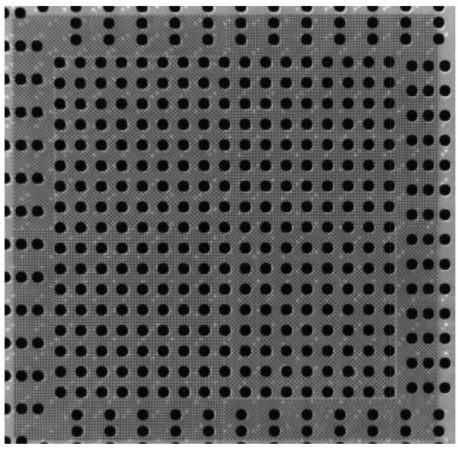

Figure 6. X-ray image of bump after assembly.

It is very difficult to eliminate dicing defects even with laser dicing. A major challenge is how to prevent cracks initiated at the die edge or corner from dicing to propagate into the active die area under the thermo-mechanical stresses. In dies with SiO_2 as BEOL dielectrics, the toughness of the dielectrics is higher than that of Si, so the die itself often presents the weakest point and cracks can propagate into the interior of the chip. With the introduction of low-k/ELK dielectrics, the fracture toughness has been substantially reduced and is significantly lower than that of Si. It is much easier to induce defects like microcracks during dicing. Those tiny cracks can develop and propagate into the active die area and cause failure under thermal-mechanical stress. One approach to prevent cracking at the die edge or die corner is to apply patterned metal structures called crack stop around the perimeter, especially reinforced at the die corners: crack stop toughness must be strong enough to avoid reliability issues. The criterion is

$$G < G_{crackstop} \qquad (1)$$

G is the energy release rate at the die edge or corner, which can be simulated from FEA modeling. $G_{crackstop}$ is the crack stop toughness, which can be measured by four-point bending method. The crack stop must be designed to have minimal impact on the die size and must be manufacturable for high volume production.

In our TV, a single wall crack stop has been selected as the worst case for the test. Two reliability test conditions, TCG (-45°C to 125°C) and TCJ (0°C-100°C), have been applied for the test. The test results showed that there are no failures for TCJ test with passing 3K cycles, and we start to see failures from TCG600 and more failures showed up at TCG1.2K. CSAM picture (Figure 7) shows that delamination occurred at the die corner. FIB cross-section analysis of the delamination area indicated that the crack has broken the crack stop and propagated into the active area and caused electrical failure.

Test results proved that micro-cracks developed and propagated into the active area under the aggressive test

condition, and single wall crack stop is not strong enough to prevent the crack growth. Since the TV passed the TCJ3K test, but failed at TCG which means CPI reliability margin is not good enough. In order to improve the reliability, one way is to improve the dicing process, which can help reduce the dicing defects and size of the cracks,

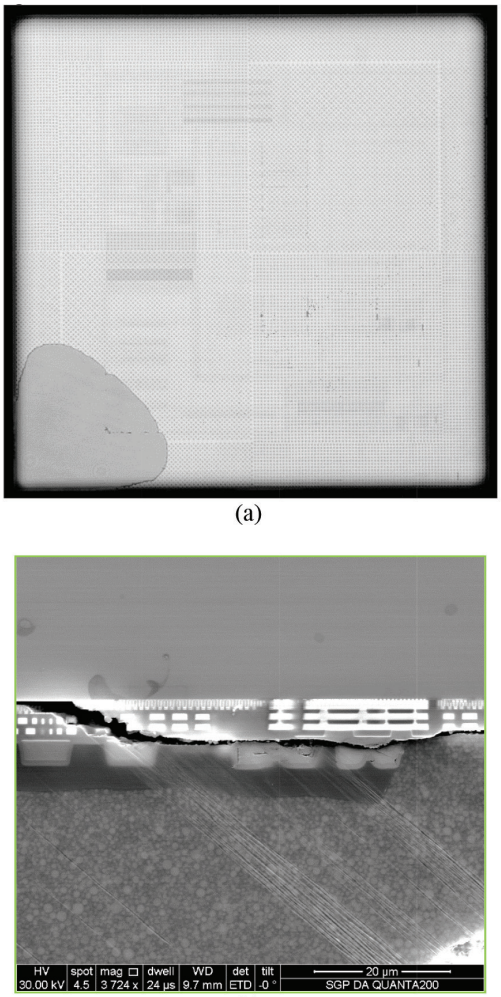

Figure 7. CSAM picture showing (a) corner delamination; and (b) FIB-x-section picture showing crack, broken crack stop and propagation into active area.

but cannot eliminate those minor defects. Another way is to use stronger crack stop with increasing $G_{crackstop}$. So in our product design, two metal walls crack stop have been applied. Crack stop toughness increased significantly to provide enough margin for the product reliability.

5. CPI qualification results

Quick thermal cycling test (QTC) has been widely used in the semiconductor industry to evaluate ELK margin for CPI. The parts built without underfill (UF) and run through thermal cycling test (-40°C TO 60°C). Data without white bumps is the critical criteria for the QTC test. Normally we use 20 cycles as the release condition for CPI. The more cycles passed represents stronger ELK dielectric material and overall more robust structure. Representative CSAM picture in **Figure 8** after QTC 20 cycles shows no white bumps.

Reliability Test	Reference Standard	Sample size	Results	Conclusion
ATC (Accelerated Temp Cycling)	AMD spec	45	0/45	Pass
Preconditioning +	JESD22-A113	693	0/693	Pass
Temp Cycling, Cond. J	JESD22-A104D	231	0/231	Pass
Temp Cycling, Cond. G	JESD22-A104D	231	0/231	Pass
Unbiased HAST	JESD22-A118	231	0/231	Pass
High Temp Storage	JESD22-A103	231	0/231	Pass

Table 1. Reliability Test Condition and Result Summary

The standard JEDEC tests with selected conditions (Preconditioning, TCG, TCJ, UBHAST, HTS) are used for our 14nm product qual. Table 1 lists the tests and conditions, sample size and test results. Samples have passed all the test specs. The test results proved that our current design rules, bump selection and assembly process are good to go for our production.

Summary

In our 14nm CPI technology evaluation, we developed 140um bump pitch with SnAg bump CPI TV and assessed crack stop effect on CPI reliability with large die size. The

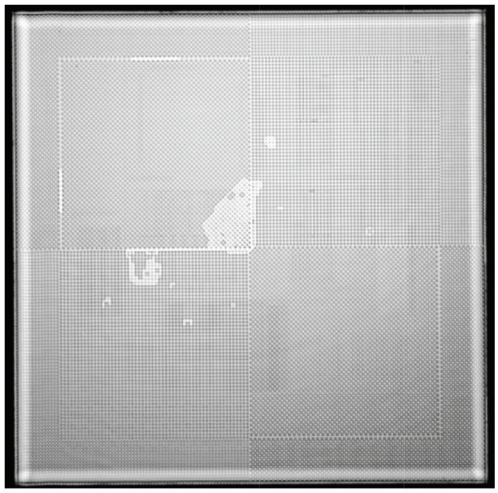

Figure 8. CSAM picture after QTC 20 cycles showing no white bumps observed.

results proved that dual passivation with Al terminal metal can provide strong support to eliminate ELK crack with smaller bump size of SnAg avoiding solder bridging during assembly. With less CPI reliability margin of single wall crack stop, double wall crack stop is strongly recommended for product with large die size to provide protection for the dicing defects to propagate. CPI qualification passed with all the design rules, BOM selection and assembly process.

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Next Generation Xeon Server Package Architecture

Raja Swaminathan, Ram Viswanath, Sriram Srinivasan, Arun Chandrasekhar
Intel Corporation, 5000 W Chandler Blvd, Chandler, AZ 85226, USA
Phone: 480-552-6882, Email: rajasekaran.swaminathan@intel.com

Abstract

The semiconductor industry is moving towards more and more integration to provide more functionality and add value to the processor, thereby enabling better user experience. This integration can come in 3 categories: On-die integration, On-package integration, and On-board integration. On-board integration is the typical method being used for several generations and on-die and on-package integration architectures are getting more focus due to better performance and reduced power. The key vector to enable on-die/package architectures is reduced cost and maximum features for a given substrate and socket form factor. Silicon features are also moving at a faster pace compared to the board technology. This paper details a novel package (PoINT) architecture as well as the key technology challenges that were resolved to successfully enable this architecture.

Key words

PoINT, patch, interposer, mid-level interconnect, packaging, low temperature solder

I. Introduction

The IO feature set requirements for server packaging have been escalating at >20% CAGR for the past few years. This, coupled with the fact that the package pinout needs to be routable in a PTH-based PCB restricts the pitch scaling at the package and socket level. To circumvent this problem, we introduce a novel package architecture PoINT (patch on interposer) in this paper.

PoINT involves splitting [1] a monolithic package substrate into a high-density component (patch) on which the silicon is assembled and low-density component (interposer) that couples this to the socket/board, without compromising product performance. This involves two levels of interconnect, FLI and MLI. The MLI decouples the package scaling from the PCB scaling and allows a more optimal cost structure for the final product. The high-density substrate provides required density for silicon fan-out at the lowest possible cost. The low-density substrate with its coarser density acts as a translation layer between the high-density substrate and the socket. The technology decouples the silicon/die/substrate requirements (referred to as first-level interconnect) from the substrate-board interface (second level interconnect) by invoking a mid-level interconnect (HD substrate to LD substrate).

With the selection of optimized material properties and design rules, this technology enables a path for improved product performance as well as minimizing cost.

II. Package Architecture and Technology Challenges

A. Package Architecture

Figure 1 shows the cross section of a typical PoINT package. The patch is a thin core substrate with high density design rules in the buildup layers that support IO escape from the die as well as distributes power to the die. The interposer is comprised of laminated metal layers with a pre-peg dielectric material (similar to a high end motherboard construct, but with tighter design rules) manufactured using a subtractive process. The interconnect between the patch and interposer is referred to as the Mid-Level Interconnect (MLI) and has a pitch sufficiently large to support the coarser design rules on the interposer needed for IO escape through BGA.

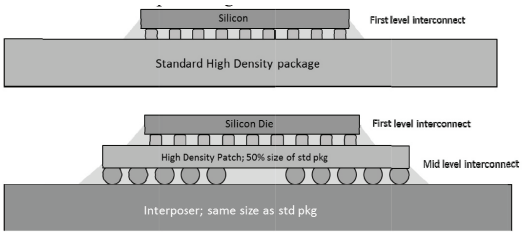

Figure 1. Standard and PoINT package cross-section view illustrating the stack-up and architecture differences.

In the analyses described in this paper, the standard package had a 7-x-7 stack-up (7 top and bottom build up layer on an 2-4L core architecture) while the PoINT architecture had 6-2-6 stack up for the patch on standard core with 10-12L interposer. Figure 2 shows the top view of the substrate only for the standard and PoINT architectures.

Figure 3 details the interconnect hierarchy differences between the standard package and PoINT architecture. The signal integrity implications of the more discontinuous PoINT architecture and enablers to resolve differences are highlighted in Section E.

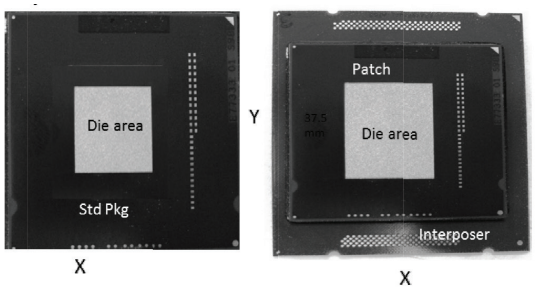

Figure 2. Top view of the substrate only for the standard package vs. PoINT architectures. The interposer dimensions are same as the standard package dimensions.

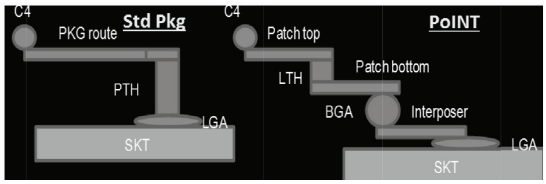

Figure 3. Interconnect hierarchy differences between standard and PoINT package architectures.

B. Assembly Challenges and Enablers

The typical PoINT process flow includes attaching die to the patch followed by attaching the patch to the interposer. The key challenges in enabling the patch to interposer attach for large die sizes is to have a wide enough MLI process window to accommodate the large warpage difference between the die+ patch (dominated by silicon CTE (co-efficient of thermal mismatch) of ~3ppm/°C) and the interposer (CTE typically of the order of ~17-20ppm/°C). Figure 4 shows the schematic dynamic response of a typical die + patch BGA package as a function of temperature and empirical test vehicle data validating the schematic.

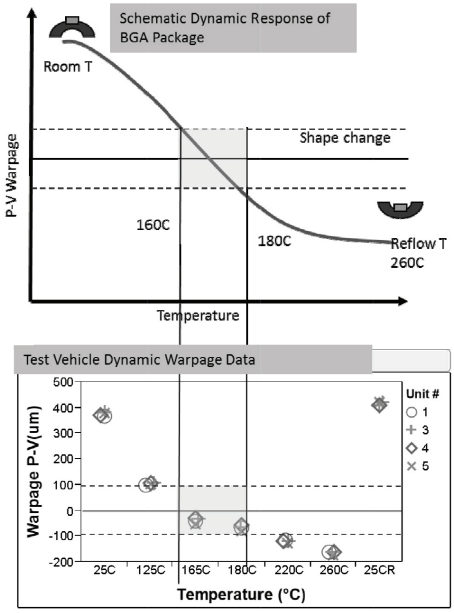

Figure 4. Schematic dynamic response of BGA package and test vehicle data for large die-patch ratio showing warpage transition region.

The key invention that enabled the successful patch-interposer attach process was to tune the attach temperatures to take advantage of the shape cross-over at ~ 160-180°C. This led to the invention and development of a low temperature solder (LTS) chemistry specifically tuned for this MLI attach process. Figure 5 shows the solder joints comparison between a standard reflow process and LTS reflow process, highlighting the non-wets in the standard process vs. good solder joints in the LTS process.

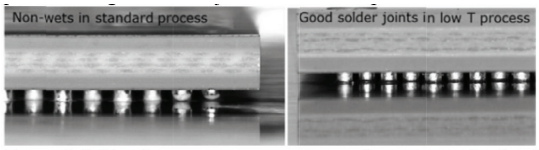

Figure 5. Solder Joint geometry comparison between standard and LTS reflow process.

Figure 6 shows the cross-section of the MLI joint with this new LTS solder post assembly and reliability, indicating successful joint formation and stability.

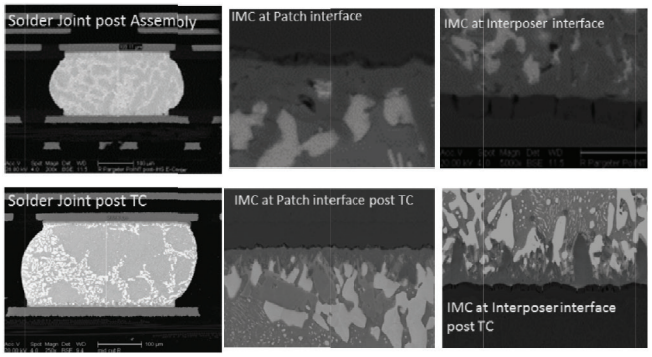

Figure 6. Cross sections detailing solder joint quality and interfacial IMC (patch and interposer) post assembly and temp cycle.

C. PoINT Physical Design Optimization

PoINT, by the nature of its architecture, has two substrates in place of one which poses a design challenge that required careful optimization of netlists, IO length matching between patch and interposer and drove new processes and tools to ensure synchronization between the parallel patch and interposer designs. The tighter MLI ball pitch (that wouldn't be available on a standard package) allowed the design teams to distribute power uniformly under the patch around the MLI cavity to not cause any power hot spots. The tighter MLI pitch also enabled more vertical connections [2] in the power islands under the die to reduce resistance further (details in next section). Figure 7 shows a sample schematic of MLI pattern optimization for power and IO domains. This required careful silicon-package co-design to optimize IO floor plans so there is wider power entry to the die.

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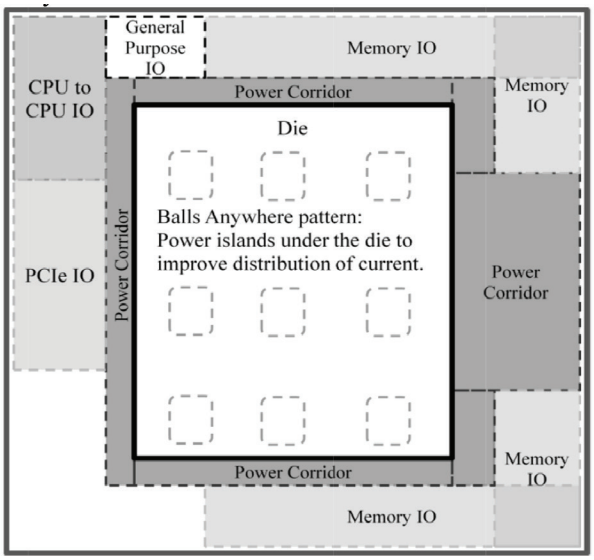

Figure 7. Sample schematic of MLI ball pattern optimization for power and IO.

D. Power Delivery Challenges and Enablers

The voltage drop for the incoming power supply from the mother board was projected to be higher on PoINT architecture relative to standard package construct due to the more resistive path in the PoINT architecture that could have resulted in potential loss in product performance. An MLI pattern typically includes a cavity to enable an air gap to support the air core inductor designed in the patch. The reader is directed to reference Burton et al. [4] on air core inductor and how it supports Intel FIVR architecture. The MLI ball pattern optimization involved including Vin (input voltage) balls for the power delivery supply within the MLI cavity and optimizing the ACI designs in the patch + MLI cavity for best FIVR efficiency (Figure 8). Further improvements in power were achieved by increasing Cu thickness on power routing layers in patch and interposer.

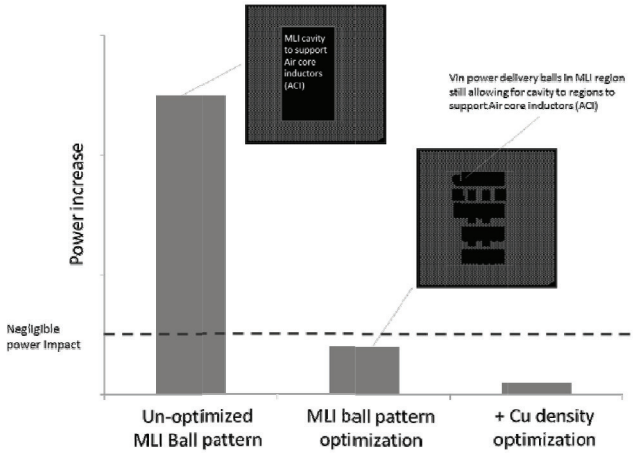

Figure 8. PoINT MLI ball pattern optimization to mitigate power increase.

In addition to meeting the power requirements, the AC noise was optimized (in a constrained patch form factor) to meet platform specifications by improving assembly design rules (and associated thermo-mechanical KOZs for integrated heat spreader, see Figure 10) that allowed placement of more die side capacitors within a given area.

E. Signal Integrity Challenges and Enablers

Due to the two-level interconnect partitioning, PoINT architecture was challenging from an IO design perspective since it involves routing on two different substrates (patch and interposer) which also have different impedance values [4]. Typically, longer routing lengths contribute to more insertion loss and cross talk between adjacent traces. Significant silicon-package co-design, including silicon IO floor planning to move on-die memory ports closer to the socket pin field, MLI pattern optimization resulted in minimizing the routing length considerations. The impedance discontinuities could have led to degradation in IO margins. The cross talk challenge was solved by innovating on socket/package pin patterns and novel micro-via architectures in the patch and interposer (Figure 9).

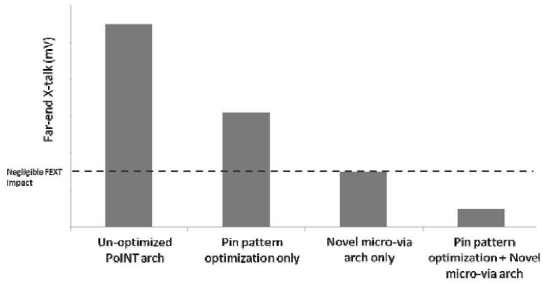

Figure. 9 PoINT architecture optimization to mitigate cross-talk increase.

The impedance discontinuity challenge was solved by impedance tolerance improvements with materials/process optimization resulting in improved eye height and width margins for all signaling interfaces.

F. IHS Design and Socket Optimization

Novel integrated heat spreader (IHS) designs (Figure 10) were also developed to mitigate package warpage during enabling and socket loading. This design involved IHS feet landing on patch and interposer, as well as I-shaped feet landing on the interposer to maximize coupling all the way to the package edges without compromising on the loading mechanism (ILM+ heat sink) KOZs. The Z-heights of the interposer, patch and IHS also have to be carefully tuned to minimize the overall system z-stack and enable transparency to end customers and compatibility with earlier platforms.

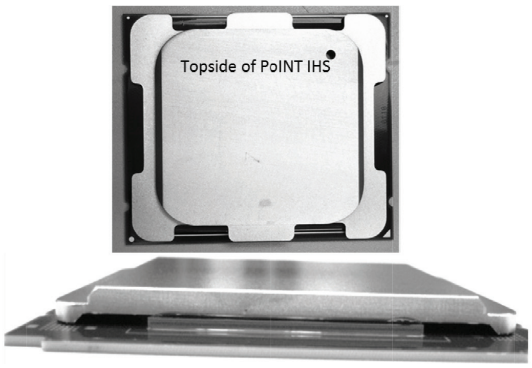

Figure 10. Novel IHS design optimized for PoINT architecture (top and cross-sectional views).

With the IHS optimization, we were able to keep the interposer (thinner than standard package) warpage within the package warpage specification required for robust socket loading (translated as socket contact force). Figure 11 shows similar socket normal contact forces (gf) for various warpage values between standard and PoINT architectures.

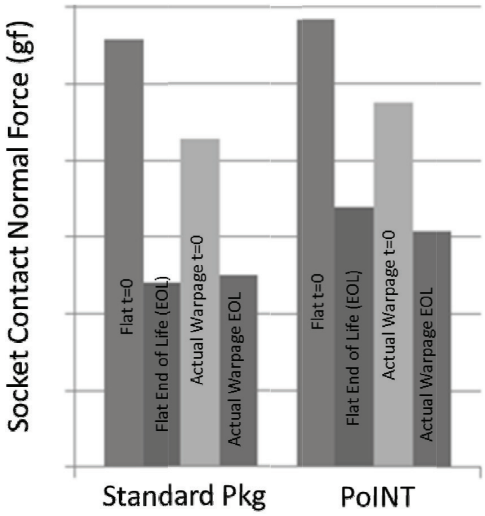

Figure 11.

III. Conclusion

This paper introduced the novel PoINT package architecture that involves splitting a monolithic package substrate into a high-density component (patch) on which the silicon is assembled and low-density/cost component (interposer) that couples this to the socket/board. We also detailed the key assembly challenges and inventions (LTS based process) to address the warpage challenges. Significant design optimizations enabled superior product performance.

Acknowledgment

The authors would like to acknowledge the following people for their valuable contributions: Amar Vuppala, Michael Carroll, Krishna Bharath, Wei-Lun Jen, Zhichao Zhang, Rajen Sidhu, Khine Han, Srikrishnan Venkataraman, Farzaneh Yahyaei-moayyed, Zhichao Zhang, Bhanu Jaiswal, Kemal Aygun, Dan L Stuart, Kaladhar Radhakrishnan and Feroz Mohammad.

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iMAPS 2018

Save the Date

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The 2017 3D ASIP Conference opens with a choice of one of three morning tutorials on Tuesday, December 5: (*1) The Evolution of High Density Packaging; (2) Fan Out Packaging Evolution and Complexity; or (3) Introduction to Solder Flip Chip with an Emphasis on Cu Pillar.* The general conference sessions follow on Tuesday afternoon, Wednesday and Thursday, December 5-7.

Sessions:

Micro Bumping and Copper Pillar Technology; Equipment & Materials; 2.5/3D Enabled Applications; Military and Aerospace; Advanced Assembly Technology; FOWLP; and Image Sensor Technology

Keynotes:

World Level Packaging Concepts "Wafer, Wafer – Who's Got the Wafer?"

Jim Walker, WLP Concepts

High Density Interconnects: Migrating from Concept to Mainstream

Brandon Prior, Prismark

Impact of Design on Advanced Packaging

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Lifetime Achievement Award
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Microelectronics Foundation

Dr. Woong-Sun Lee, Hynix Semiconductor, Inc., hit a hole-in-one on the sixth hole during the Microelectronics Foundation David C. Virissimo 2017 Memorial Fall Golf Classic at IMAPS 2017 on October 9 at Lonnie Poole Golf Course, NC State University, Raleigh.

Congratulations, Dr. Lee!

Scenes from IMAPS 2017

A busy Exhibit Hall - the best of the Symposium

Presidential Gala honoring current and past Presidents, Officers, Award Recipients and long-time volunteers.

Scenes from IMAPS 2017

Silent Auction to benefit the Microelectronics Foundation – decisions-decisions!

Global Business Council Marketing Forum

IMAPS 2017

…and the WINNER of the 50/50 Raffle was

Michael Benson of 5N PLUS at which point he donated his winnings back to the Microelectronics Foundation.

Thank you, Michael!

RTP High School was invited to spend the day at the Symposium. The student members of Terror Bytes interacted with exhibitors, had lunch, demonstrated their robot and received a check for $2,000.

A great day for all!

IMAPS/ACerS 14th International Conference and Exhibition on

Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT 2018)

18-20 April 2018
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ABSTRACTS DUE: NOVEMBER 30, 2017

Goal
The Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT) conference brings together a diverse set of disciplines to share experiences and promote opportunities to accelerate research, development and the application of ceramic interconnect and ceramic microsystems technologies. This international conference features ceramic technology for both microsystems and interconnect applications in a dual-track technical program. The Ceramic Interconnect track focuses on cost effective and reliable high performance ceramic interconnect products for hostile thermal and chemical environments in the automotive, aerospace, lighting, solar, defense/security, and communications industries. The Ceramic Microsystems track focuses on emerging applications and new products that exploit the ability of 3-D ceramic structures to integrate interconnect/packaging with microfluidic, optical, micro-reactor and sensing functions. Tape casting, thick film hybrid, direct write and rapid prototyping technologies are common to both tracks, with emphasis on materials, processes, prototype development, advanced design and application opportunities.

Ceramic Interconnect Track
Conventional thick and thin film ceramic technologies are being revolutionized and extended through the development of low temperature co-fired ceramics, photo patterning, and embedded passive component materials and processes. These have contributed to increased circuit density, enhanced functionality, and improved performance that are being adopted for leading edge applications in wireless and optical communications, automotive, MEMS, sensors, and energy. Data communications and the Internet are driving the demand for bandwidth, sparking demand for optical communication equipment and new interconnect and packaging applications that perform at 40 Gb/sec and beyond. In under-the-hood electronics for automotive, engine/transmission control, communications, and safety applications continue to drive the growth of ceramic interconnect technology, while collision avoidance systems are creating interest in low loss ceramic materials for frequencies approaching 100 GHz.

Ceramic Microsystems Track
Enabled by the availability of commercial ceramic, metal and embedded passives materials systems, and the rapid prototyping capabilities of the well established multilayer ceramic interconnect technology, three dimensional (3-D) functional ceramic structures are spawning new microsystems applications in MEMS, sensors, microfluidics, bio-devices, microreactors, and metamaterials. These new devices and applications exploit the ability to integrate complex 3D features and active components (e.g., valves, pumps, switches, light pipes, and reaction chambers).

In addition, the Ceramic Microsystems track of the CICMT conference targets new developments in microsystems that include fabricating 3-D micro device structures enhanced with sol-gel, advanced printing and patterning technologies, high temperature materials technologies, and emerging applications like energy harvesting. Many of these innovative applications are taking advantage of the unique ability to integrate the thermal, chemical, mechanical and electrical properties of these multicomponent ceramic-metal systems.

Special Features
- Invited keynote and international presentations on the current status ceramic technology and future system directions.
- A focused exhibition for suppliers who support the use of the technologies.
- A technical poster session to promote student participation.
- Social events to promote new contacts.

IMAPS/ACerS 14th International Conference and Exhibition on

Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT 2018)

Planned Session and Paper Topics Include:

Ceramic Microsystems	Ceramic Interconnect
Markets and Applications • MEMS Technology and Markets • Batteries and Fuel Cells • Biological and Medical • Chemical and Biochemical • Photonics **Materials and Properties** • Materials Integration and Nano-materials • Thermal Management and Reliability • Piezoelectric Materials • Optoelectronics **Processing and Manufacturing** • MEMS Manufacturing Technology • Industrial Automation and Rapid Prototyping • Nano-technology/Integration • High Temperature Microsystems **Devices** • Sensors and Actuators • Micro-reactors • Fluidic Devices • Biomolecular and Cell Transport Systems • Energy Conversion Systems **Characterization and Reliability** • Materials and Process Characterization • Systems Reliability, Lifetime, and Failure Estimation • Reliability of High-Performance Microsystems **Design, Modeling, and Simulation** • Thermal and Heat Transfer • Computational Fluid Dynamics	**Markets and Applications** • Automotive • Aerospace • Lighting/Solar • Wireless/Communication • Medical Electronics **Materials and Properties/Functions** • Dielectric and Magnetic Materials • Embedded and Integrated Passives • Microwave/mm Wave Characterization • Zero-shrink Ceramic Systems **Processing and Manufacturing** • LTCC and Multilayer Ceramics • Roll to Roll and Continuous Manufacturing • Direct WRite and Drop on Demand • Advanced Thick Film Processing • Fine Structuring Technologies **Devices** • Circuits, Antennas, and Filters • Embedded Structures and Components • Optical Devices and Optoelectronics **Characterization and Reliability** • Characterization of Green Tapes • Life Testing, Quality Issues • RF Performance **Design, Modeling, and Simulation** • High Frequency Design Software • Design Rules

Integrated Ceramic Technology
Advanced Packaging Technology • Next Generation Packaging Technologies • Packaging and Integration in BioMEMS • Packaging Issues for MEMS Devices • Technologies for Microsystems Components and Substrates • Packaging Standard for Microsystems • Environmental Issues, Lead Free Systems • Cost Reduction

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Notice of Acceptance: January 5, 2018

Please send your 1000+ word abstract electronically ***ON/BEFORE NOVEMBER 30***, using the on-line submittal form at: www.imaps.org/abstracts.htm. Full written manuscripts are not required; however, ***speakers will be invited to submit full papers for peer-review and publishing with IMAPS or ACerS Journals. IMAPS-accepted papers will be assigned DOIs, archived into IMAPS Microelectronics Research Portal (www.IMAPSource.org), and fully citable.*** All papers will be presented and published in English. All speakers are required to pay a reduced registration fee. If you are having problems with the on-line submittal form, please email Brian Schieman bschieman@imaps.org.

Registration and Hotel Reservations *(Details SOON)*

INDUSTRY NEWS

DuPont 3D Printing Filaments are Now Available for Purchase in the United States, Canada and Mexico

WILMINGTON, Del., Sept. 21, 2017 — DuPont Performance Materials (DuPont) is pleased to announce that customers can now purchase DuPont™ Hytrel® thermoplastic elastomer and DuPont™ Zytel® nylon-based filaments for 3D printing in the United States, Canada and Mexico through Coex LLC.

DuPont 3D printing products allow users to achieve the true benefits of 3D printing (greater design freedom, light weight, reduced product development cycle times) allowing for rapid functional prototyping, parts production, tooling and customization in all sectors of the industry, such as automotive, electronics, footwear, consumer goods and others.

With Hytrel® available in two different hardness levels (Hytrel® 3D4000FL with a shore D of 40 and Hytrel® 3D4100 with a shore D of 60) for 3D printing, customers will be able to make flexible functional parts that combine resiliency, heat and chemical resistance with strength and durability. Mechanical properties of 3D printed parts in all directions using Hytrel® grades are comparable to injection molding.

With Zytel® 3D1000FL, customers will be able to make strong and stiff functional parts. Along with superior strength, parts printed with Zytel® product also have high heat deflection temperature, low warpage, low sensitivity to moisture and excellent surface aesthetics.

DuPont™ Hytrel® thermoplastic elastomer filaments for 3D printing

DuPont™ Zytel® nylon-based filaments for 3D printing

Proven over decades of use, DuPont™ Hytrel® thermoplastic elastomers and DuPont™ Zytel® nylons offer high quality, reliability and performance in various applications in a wide range of industries. For additional information on DuPont's offerings in the 3D printing market, visit www.3DPrintingSolutions.DuPont.com. Order your Zytel® and Hytrel® products for 3D printing at www.coexllc.com.

"We are very excited that customers in North America can now purchase DuPont high-performance materials in filament form for 3D printing through Coex LLC," said Rahul Kasat, business development leader, DuPont Performance Materials. "We continue to get very positive feedback on ease of printing and performance of these products from customers across multiple industries."

About DowDuPont Specialty Products Division

DowDuPont Specialty Products, a division of DowDuPont (NYSE: DWDP), is a global innovation leader with technology-based materials, ingredients and solutions that help transform industries and everyday life. Our employees apply diverse science and expertise to help customers advance their best ideas and deliver essential innovations in key markets including electronics, transportation, building and construction, health and wellness, food and worker safety. DowDuPont intends to separate the Specialty Products Division into an independent, publicly traded company. More information can be found at www.dowdupont.com.

Contact:
Melissa Bruhl
302-992-2048
Melissa.D.Bruhl@dupont.com

Integra Technologies Announces the Purchase of CORWIL Technology

Integra Technologies, LLC, a world leader in integrated circuit test and related services, announced today that it has acquired CORWIL Technology Corporation (CORWIL). CORWIL provides high quality and responsive semiconductor die prep, assembly and test services focusing on Hi-Rel, fast-turn and wafer processing markets. Founded in 1990 and based in Milpitas, CA, CORWIL is the premier U.S. provider of full back-end assembly services and is a key partner with leading medical, Mil/Aero and commercial semiconductor companies.

The combination of the two companies will provide a single point of contact for an extremely broad array of semiconductor die prep, assembly, test and evaluation services supporting the Military, Avionics, Space, Medical, Automotive and Fabless Semiconductor markets.

"We are very excited about the combination of Integra and CORWIL," said Brett Robinson, President and CEO of Integra Technologies. "The combination provides our mutual customers with one of the largest U.S.-based semiconductor die prep, assembly and test offerings in the in-

dustry." Mr. Robinson added further, "Integra has been an employee-owned company since 2008 and we are pleased to welcome our new employee-owners from CORWIL."

Matt Bergeron, President of CORWIL Technology, commented, "I was happy to see that Integra was selected as our new parent/partner. It provides a great assurance to our customers (especially those in the Hi-Rel market), employees and suppliers that they will be in good hands."

CORWIL will continue operations in Milpitas, California with existing employees, management team and product/service offerings.

For more information, please contact:
Kent Wade
Integra Vice President Sales
316-630-6821
kent.wade@integra-tech.com
www.integra-tech.com
or
Matt Bergeron
CORWIL President
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About Integra Technologies

Integra Technologies, an employee-owned company, is one of the largest independent test labs in the U.S. and Europe. Integra's operation has been satisfying customers for over 30 years by providing a wide variety of IC test and related services including: Test Development, Final Test, Characterization, Wafer Probe, Qualification (HTOL, HAST, Temp Cycle), DPA, CSAM, FA, Upscreening, MIL-STD testing, counterfeit detection, obsolescence management and DMEA Trusted processing. Integra has one of the largest and most experienced test engineering organizations offering support for every device technology including RF, Mixed Signal, Digital, Linear and Analog. Integra provides 24x7 high or low volume capacity and has demonstrated industry leading quality and on time delivery performance.

For more information about Integra, please visit www.Integra-Tech.com.

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Kester Launches Robotic Cored Wire

ITASCA, IL, October 6, 2017 — Kester is proud to announce the launch of 268 Flux-Cored Wire, a zero-halogen wire optimized for robotic soldering applications. With its unique chemistry system, 268 provides consistent workability performance for both robotic and manual soldering in the electronics industry, with performance equivalent to conventional halogen/halide-based systems. 268 provides a clean release which prevents occurrences of bridges and protrusions, even in narrow-pitch automated drag soldering. The use of 268 results in a clear post-soldering residue without the need for cleaning.

For additional information on this product including technical and safety data sheets, please visit http://www.kester.com/products/product/268-flux-cored-wire.

For any questions or additional information, please contact: Chad Showalter, Global Product Manager at cshowalter@kester.com.

Kester is a global supplier of assembly materials for the Electronic Assembly and Semiconductor Packaging industries. Kester is focused on delivering innovative, robust and high-quality solutions to help our customers address their technological challenges. Kester's current product portfolio includes soldering attachment materials such as solder paste, soldering chemicals, TSF (tacky solder flux) materials, and metal products such as bar, solid and flux-cored wire. Kester is an Illinois Tool Works (ITW) company. ITW is a Fortune 200 company that produces engineered fasteners and components, equipment and consumable systems, and specialty products. It employs approximately 49,000 people, and is based in Glenview, Illinois, with operations in 57 countries.

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High Temperature Resistant, NASA Low Outgassing Approved Epoxy for Die Attach Applications

Formulated for die attach applications, Master Bond EP17HTDA-1 is a one component epoxy that can also be used for bonding and sealing. "EP17HTDA-1 has the ideal viscosity and flow for die attach applications," said Rohit Ramnath, senior product engineer. "It has a high glass transition temperature (Tg) and also offers excellent electrical insulation properties, even at elevated temperatures and low exotherm upon curing." This system features an excellent die shear strength of 24-27 kg-f and can be used in a typical die size ranging from 4-400 mm2.

EP17HTDA-1 has exceptional temperature resistance with a service temperature range of -80°F to +600°F [-62°C to +316°C] and a Tg of 195-205°C. This compound boasts thermal conductivity of 9-10 BTU•in/ft2•hr•°F [1.30-1.44 W/(m•K)]. It withstands a variety of chemicals including acids, bases, salts, fuels, oils and many solvents.

As a one part system, EP17HTDA-1 does not require any mixing for use and is curable in the temperature range of 300-350°F in short durations. It bonds well to a wide variety of substrates, such as metals, ceramics, plastics and composites. Upon curing, it delivers a tensile lap shear strength of 2,400-2,600 psi and a tensile strength of 9,000-10,000 psi. It also has minimal shrinkage upon curing.

While EP17HTDA-1 is well suited for electronic and related applications, it can also be used in vacuum situations as it passes NASA low outgassing testing. This epoxy is available for use in 10 cc and 30 cc syringes and has a shelf life of 3-6 months when stored at 40-50°F.

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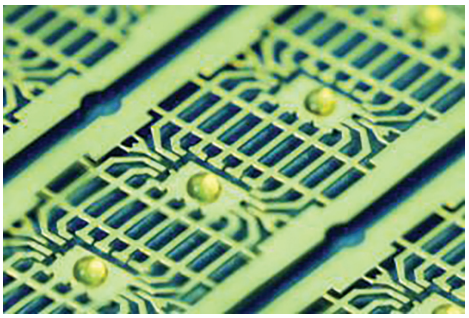

Master Bond Die Attach Adhesives

Master Bond EP17HTDA-1 is a one part epoxy system for die attach, bonding and sealing applications that features high temperature resistance, thermal conductivity and NASA low outgassing approval. Read more about Master Bond's die attach adhesives at https://www.masterbond.com/industries/die-attach-epoxy-adhesives or contact Tech Support. Phone: +1-201-343-8983 Fax: +1-201-343-2132 Email: technical@masterbond.com.

Toughened, Two-Component Epoxy Features Enhanced Dimensional Stability and a Long Working Life

Developed for potting, sealing, encapsulation and casting applications, Master Bond EP110F8-5 is dimensionally stable and has low shrinkage upon cure. This system features superior electrical insulation properties including a volume resistivity exceeding 1015 ohm-cm, a dielectric constant of 2.91 at 1 KHz and a dissipation factor of 0.009 at 1KHz. "EP110F8-5 is an easy to use, heat curing epoxy that is ideal for applications where dimensional stability, electrical insulation properties and thermal cycling resistance are required," said Rohit Ramnath, senior product engineer.

This two-component epoxy has a very forgiving one to two mix ratio by weight with a moderate mixed viscosity of 7,000-11,000 cps and good flow properties. It requires an elevated temperature cure at 250-300°F in 4-6 hours. EP110F8-5 has a very long pot life of 2-3 days at room temperature.

EP110F8-5 is a rigid system with a Shore D hardness of 70-80, but also maintains excellent toughness and offers an elongation of 40-60%. Its toughness imparts an ability to withstand thermal cycling as well as impact and vibration. In fact, it passes 10 thermal shock cycles of -55°C to +125°C. With a compressive strength of 18,000-20,000 psi, EP110F8-5 adheres well to a wide variety of substrates, including metals, composites, glass and many plastics. It resists exposure to water, oils and fuels.

It is serviceable over the wide temperature range of -100°F to +300°F [-73°C to +149°C]. Part A of EP110F8-5 is tan in color and Part B is brown. This system is available for use in 1/2 pint, pint, quart, gallon and 5 gallon container kits.

Master Bond Epoxies with Dimensional Stability

Master Bond EP110F8-5 is a two-part epoxy system for potting, sealing, encapsulation and casting applications with convenient handling, reliable electrical insulation properties and dimensional stability. Read more about Master Bond's dimensionally stable adhesives at adhesives at https://www.masterbond.com/properties/dimensionally-stable-epoxy-adhesives or contact Tech Support. Phone: +1-201-343-8983 Fax: +1-201-343-2132 Email: technical@masterbond.com.

About Master Bond

Since its founding in 1976, Master Bond has been committed to developing epoxies, silicones, light curing systems and other specialty adhesives that meet specific customer requirements. Master Bond manufactures over 3,000 grades of specially designed formulations that are widely used across a variety of industries including electronic, medical, aerospace and optical.

Contact:
James Brenner, Marketing Manager
Email: jbrenner@masterbond.com
Tel: +1-201-343-8983
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RUDOLPH TECHNOLOGIES

Rudolph Technologies Launches New Truebump™ Technology at SEMICON Taiwan 2017

The Dragonfly System now features fast, accurate and repeatable 3D bump metrology

Wilmington, Mass., September 11, 2017—Rudolph Technologies, Inc. (NYSE: RTEC) announces new Truebump™ Technology on the Dragonfly™ Inspection System. Truebump Technology provides fast, accurate and repeatable three-dimensional (3D) metrology for all advanced packaging bumping applications, from copper (Cu) pillar, to microbumps, and even large C4 bumps. With the Dragonfly system, the advanced packaging industry now has premier high-volume 2D inspection and 3D bump metrology on a single platform. The first Dragonfly system with Truebump Technology has shipped to a major IC manufacturer in the United States.

"Truebump Technology combines multiple 3D metrology techniques to provide faster, more accurate, and more repeatable measurements of the 3D features that are critical in advanced packaging technologies," said Matt Wilson, senior director of inspection product manage-

INDUSTRY NEWS

ment, Rudolph Technologies. "As 2D and 3D dimensions decrease, the tolerances for manufacturing become tighter, and device stacking continues to drive an increase in functionality. Because these 3D connections are so vital for reliability, the bump height measurements need to be absolutely accurate."

Wilson continued, "A single wafer may contain 50 million bumps, each with multiple data points, creating massive amounts of data. The Dragonfly system's integrated connection with Discover® analytics software gives users tools to visualize data, correct coplanarity variations, and improve yields."

Truebump Technology is three times faster and 25 percent more repeatable than Rudolph's previous generation tool. The Dragonfly system's high volume throughput combined with industry leading accuracy and repeatability enable further adoption of stacked devices in advanced packaging applications that fuel today's drive for thinner and lighter products that deliver more capability in a smaller form factor.

For more information about Rudolph's systems and software, please visit www.rudolphtech.com.

About Rudolph Technologies

Rudolph Technologies, Inc. is a leader in the design, development, manufacture and support of defect inspection, lithography, process control metrology, and process control software used by semiconductor and advanced packaging device manufacturers worldwide. Rudolph delivers comprehensive solutions throughout the fab with its families of proprietary products that provide critical yield-enhancing information, enabling microelectronic device manufacturers to drive down costs and time to market of their devices. Headquartered in Wilmington, Massachusetts, Rudolph supports its customers with a worldwide sales and service organization. Additional information can be found on the Company's website at www.rudolphtech.com.

Contacts
Investors:
Michael Sheaffer
978.253.6273
mike.sheaffer@rudolphtech.com
Trade Press:
Amy Shay
952.259.1794
amy.shay@rudolphtech.com

Your IMAPS Member Benefits at Your Chapter Level

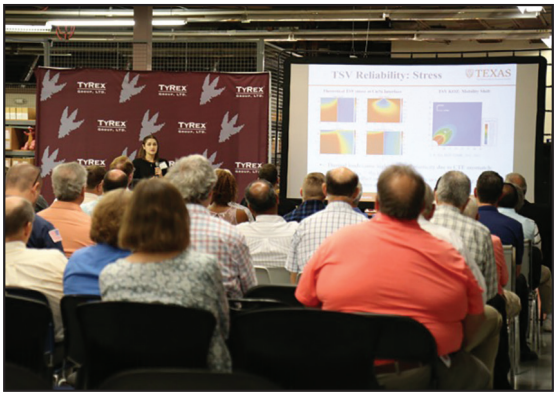
Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar

Central Texas

The Central Texas Chapter of IMAPS in conjunction with SMTA had a very interesting meeting August 24 at TyRex Group. The meeting included a factory tour of three of the business groups that are part of TyRex. One the tours was focused on the 3-D printing business. In addition to the tour, there was a presentation: "Understanding the 3D Printing Ecosystem," by Martin Johnson, Business Development Vice President. The other three presentations were: "Scaling Effect of Through-Silicon Via (TSV) on Stress & Reliability for 3D Interconnects" by Laura Spinella, PhD, UT-Austin Microelectronics Research Center, "Silicon Photonics Prototyping" by Dr. Swapnajit Chakravarty, Senior Research Scientist, Omega Optics, and "CT Teardown of the New Samsung S8+ Smart Phone" by Dr. Bill Cardoso, President, Creative Electron.

The next meeting will be the local annual Expo on October 10, 2017.

Factory tour of the 3-D printing facility at TyRex Group.



Presentation by Laura Spinella, PhD, UT-Austin Microelectronics Research Center, on Through-Silicon Vias.

Advanced Technical Workshop on

Advanced Packaging for Medical Microelectronics

www.imaps.org/medical

January 23-24, 2018

Handlery Hotel, San Diego, California

General Co-Chairs:
Susan Bagen, MST | Kedar Shah, Verily Life Sciences

Organizing Committee:
Steve Annas, Samtec | Matt Apanius, SMART Microsystems | Caroline Bjune, Draper |
Rick Elbert, Cicor | Tim LeClair, Cerapax | Vern Stygar, Asahi Glass Company

Program and Registration Online – Exhibits/Sponsorships Still Available

Overview: The International Microelectronics Assembly and Packaging Society (IMAPS) will host an Advanced Technical Workshop in San Diego on ***Advanced Packaging for Medical Microelectronics*** on January 23 and January 24, 2018. The workshop will bring together technologists in semiconductor packaging with life science experts interested in applying advanced packaging methods to enable the next generation of medical microelectronic devices. The workshop will provide a venue for presentations and discussions focused on traditional and emerging packaging technologies for wearable, portable and implantable devices, medical instrumentation, and life sciences consumables. Attendees and Exhibitors will be exposed to a wide variety of disciplines to encourage new products, discussions and collaborations. This two-day event will draw invited experts in medicine, sensing, microelectronics, and semiconductor packaging. Session are planned on:

Implantable Devices	Diagnostic and In Vivo	Portable and Wearable	Technology
Pacemakers and Defibrillators	Interventional Catheters	Remote Diagnostics	Biosensors and MEMS
Neurostimulators	Pillcams	Defibrillators	Batteries and Energy Harvesting
Deep Brain Stimulation	Ultrasound and Imaging	Point of Care	Biocompatible Materials
Drug Delivery	Lab-on-Chip	Patient Monitoring	Encapsulation/Hermeticity
Cochlear Implants	Micro Reactors	Ambulatory Care	HDI Flex and Packaging
Retinal/Ophthalmic	Surgical Devices	Hearing Aids	Wireless Communications
Electroceuticals and Injectables		Neurostimulators	Reliability
		Prosthetics	

Program and Registration will be available at: www.imaps.org/medical

Priced at $550 for IMAPS members, $650 for non-members, and $300 for speakers, attendance will be limited to maintain a workshop atmosphere. Workshop will feature panel discussions for increased open engagement and networking. 20 tabletop spaces are available this year to allow for more company participation. For further information and to submit abstracts or to register, visit www.imaps.org/medical or email bschieman@imaps.org.

*i*MAPS New England – 45th Symposium & Expo

The Largest Regional Symposium Dedicated to

Microelectronics, Assembly and Packaging

Boxboro Regency Hotel & Conference Center

Boxborough, Massachusetts

May 1, 2018

EarlyBird Exhibitor Registration is Open!!

The Technical Program is Being Assembled

Visit www.imapsne.org

The New England Chapter

Call for Papers & Posters

- 2D-3D & Beyond
- Medical Device Packaging
- RF & Microwave Innovative Technologies
- Wire & Die Bonding, Flip Chip, Bumping, TSV
- SMT & Electronics Assembly-Packaging
- Thermal Management Materials & Designs
- Military, Defense & Space Microelectronics
- High Temperature Electronics
- MEMS Sensors & Nano Technology
- Wearables - Consumer Applications
- Advanced Semiconductor Packaging
- Printed Electronics - Additive Manufacturing
- Nanoelectronic - Optoelectronic Packaging
- New & Emerging Materials-Technologies

Please e-mail your 250 word abstract to:

Dmitry Marchenko, BAE

dmarchenko@gmail.com

Deadline for Submission – December 31, 2017

visit www.imapsne.org for updates

Announcement and Call for Abstracts

International Conference and Exhibition on

High Temperature Electronics (HiTEC)

www.imaps.org/hitec

May 8-10, 2018

Hotel Albuquerque
Albuquerque, New Mexico USA

Abstract Deadline: January 22, 2018

Overview: HiTEC 2018 continues the tradition of providing the leading biennial conference dedicated to the advancement and dissemination of knowledge of the high temperature electronics industry. Under the organizational sponsorship of the International Microelectronics Assembly and Packaging Society, HiTEC 2018 will be the forum for presenting leading high temperature electronics research results and application requirements. It will also be an opportunity to network with colleagues from around the world working to advance high temperature electronics.

Abstracts being requested include the following topics:

- **Applications:**
  - Geothermal
  - Oil well logging
  - Automotive
  - Military/aerospace
  - Space
- **Device Technologies:**
  - Si, SOI
  - SiC
  - Diamond
  - GaN
  - GaAs
  - Contacts
  - Dielectrics
- **MEMS and Sensors:**
  - Vibration
  - Pressure
  - Seismic
- **Packaging:**
  - Materials
  - Processing
  - Solders/Brazes
  - PC Boards
  - Wire Bonding
  - Flip Chip
  - Insulation
  - Thermal management
- **Circuits:**
  - Analog
  - Digital
  - Power
  - Wireless
  - Optical
- **Energy Sources:**
  - Batteries
  - Nuclear
  - Fuel Cells
- **Passives:**
  - Resistors
  - Inductors
  - Capacitors
  - Oscillators
  - Connectors
- **Reliability:**
  - Failure mechanisms
  - Experimental and modeling results

Those wishing to present a paper at the HiTEC Conference must submit a 300-500 word abstract electronically no later January 22, 2018, using the online submission form at: www.imaps.org/abstracts.htm. A Final Manuscript of 6-8 pages, two-column format is due March 21, 2018, for all accepted abstracts. Please contact Brian Schieman by email at bschieman@imaps.org or by phone at 412-345-3328 if you have questions. A Proceedings DOWNLOAD containing the conference papers will be distributed to all attendees during the Conference. Speakers are required to pay a reduced registration fee.

Student Competition sponsored by the Microelectronics Foundation:

The Microelectronics Foundation sponsors ***Student Paper Competitions*** in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Students submitting their work and identifying that "Yes, I'm a full-time student" on the abstract submission form, will automatically be considered for these competitions. The review committee will evaluate all student papers/posters and award a total of $1,000 in award checks at the ATW/Conference. The selected student(s) must attend the event to present his or her work and receive the award. For more information on the student competition, go to www.microelectronicsfoundation.org.

International Microelectronics Assembly and Packaging Society

www.IMAPS.org

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- Convenient, informative webinars
- Speaking and publishing opportunities

Connections

- Local chapter membership and activities
- Post resumes and search for jobs in the JOBS Marketplace
- Participate in discussions through the Memberfuse Community website
- Maintain your professional listing

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In 2017, free downloads will be subject to membership level below. Non-member downloads will be subject to a per-article charge.

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Press releases in Corporate Bulletin	Up to 1 press release per bulletin (twice monthly)	Up to 1 press release per bulletin (twice monthly)
Member pricing for exhibitor events	Included	Included
JOBS Marketplace	Complimentary job postings	Complimentary job postings
Use of membership mailing list	3x per year	1x per year
IMAPS.org advertising	Complimentary	Member discount
Magazine advertising	One 1/4 page ad incl. annually, plus 15% discount on any additional ad	15% discount
Online Industry Guide	Includes company listing, link to website, product and service categories	Includes company listing, link to website, product and service categories
Global Business Council	Membership included	Membership included
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IMAPS has introduced a new level of support for corporate members. These companies have decided to participate in our Society at the Premier Corporate Member level. We are extremely grateful for their dedication to the furtherance of our educational opportunities and technological goals.

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Steven Clark
Erwin Cohen
Jingru Dai
Evgeny Demenev
Vincent Dessard
Whitney Durham
Glenn Farris
Sabine Fiedler
Jaspreet Gandhi
Alexandre Garcia
Robert Gernhardt
Georg Glaser
Marco Guevremont
Jing Yan He
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Daijiro Ishibashi
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Joseph Joseph
Frederick Kalinian
Inder Kanikella
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Gerard Klaasse
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Nicholas Kratzmeier
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Find out more information at http://jobs.imaps.org/home

CHAPTER CONTACTS

CHAPTER NAME	CONTACT	E-MAIL
Angel	Leadership recruitment in progress	Interested? Contact Brianne Lamm blamm@imaps.org
Arizona	Sean Ferrian	sean@ferrian.com
California Orange	Bill Gaines	William.gaines@ngc.com
Chesapeake	Lauren Boteler	Lauren.m.boteler.civ@mail.mil
Carolinas	Leadership recruitment in progress	Interested? Contact Brianne Lamm blamm@imaps.org
Central Texas	Rick Prekup	rprekup@iondsn.com
Cleveland/Pittsburgh	John Mazurowski	jmazurowski@eoc.psu.edu
Empire	Benson Chan	chanb@binghamton.edu
Florida	Mike Newton	Mike@Newtoncyberfacturing.com
Garden State	Leadership recruitment in progress	Interested? Contact Brianne Lamm blamm@imaps.org
Greater Dallas	Sam Forman	sam.forman@m-coat.com
Indiana	Larry Wallman	lwallman@sbcglobal.net
Metro	Scott Baldassarre	Scott.Baldassarre@L-3com.com
New England	Jon Medernach	jon.medernach@mrsisystems.com
NorCal	David Towne	dtowne@comcast.net
Northwest	Leadership recruitment in progress	Interested? Contact Brianne Lamm blamm@imaps.org
San Diego	Iris Labadie	iris.labadie@kyocera.com
Viking	Mark Hoffmeyer	hoffmeyr@us.ibm.com
Germany	Ernst Eggelaar	ee@microelectronic.de
France	Florence Vireton	Imaps.france@imapsfrance.org
United Kingdom	Andy Longford	Andy.longford@imaps.org.uk
Taiwan	Wun-Yan Chen	wunyan@itri.org.tw
Nordic	Terho Kutilainen	treasurer@imapsnordic.org
Benelux	Katrien Vanneste	Katrien.vanneste@elis.ugent.be
Italy	Marta Daffara	info@imaps-italy.it
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Mini-Systems, Inc.	Craig Tourgee	508-695-0203	ctourgee@mini-systemsinc.com	www.mini-systemsinc.com	back cover

Advancing Microelectronics 2018 Editorial Schedule

Issue	Theme	Copy Deadline	Ad Commitment I/Os Deadline
Jan/Feb	Device Packaging Conference and Fan-out Wafer Level Packaging	Nov. 8	Nov. 13
Mar/Apr	RF/Microwave, High-Frequency, High-Reliability	Jan. 8	Jan. 15
May/Jun	Heterogeneous Integration – System in Package (SiP)	Mar. 8	Mar. 13
Jul/Aug	IMAPS 2018 (Pasadena) Show Issue	May 8	May 14
Sep/Oct	Advanced Materials and Additive Manufacturing	Jul. 6	July 13
Nov/Dec	Chip Package Integration (CPI)	Sep. 7	Sep. 13

IMAPS HEADQUARTERS

WHO TO CALL

Michael O'Donoghue, Executive Director, (919) 293-5300, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction

Brian Schieman, Director of Programs, (412) 368-1621, bschieman@imaps.org, Development of Society Programs, Website Development, Information Technology, Exhibits, Publications, Sponsorship, Volunteers/Committees

Ann Bell, Managing Editor, *Advancing Microelectronics,* (703) 860-5770, abell@imaps.org, Coordination, Editing, and Placement Management of all pieces of bi-monthly publication, Advertising and Public Relations

Brianne Lamm, Marketing and Events Manager, (980) 299-9873, blamm@imaps.org, Corporate Membership, Membership and Event Marketing, Society Newsletters/Emails, Event Management, Meeting Logistics and Arrangements, Hotel and Vendor Management

Shelby Moirano, Membership Administration, (919) 293-5000, smoirano@imaps.org, Member Relations and Services, Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support

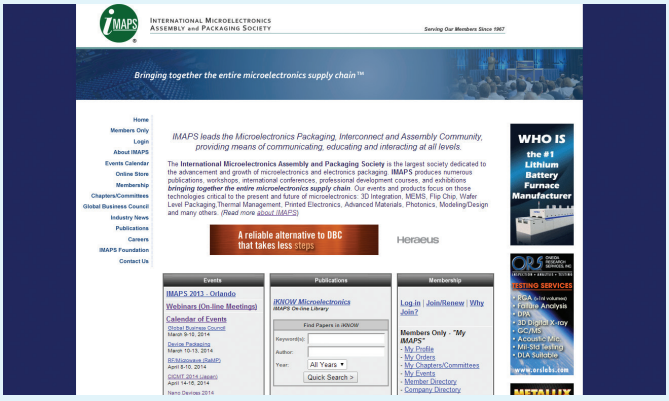
CALENDAR OF EVENTS

	start	end	
2017			
NOVEMBER	11-7-17	11-9-17	Topical Workshop and Tabletop Exhibit on Thermal Management Los Gatos, California www.imaps.org/thermal
DECEMBER	12-5-17	12-7-17	3D ASIP 2017 - 3D Architectures for Heterogeneous Integration & Packaging San Francisco, CA http://3dasip.org/
2018			
JANUARY	1-23-18	1-24-18	Adv Packaging for Medical Microelectronics San Diego, CA www.imaps.org/medical
MARCH	3-5-18	3-8-18	Device Packaging 2018 We-Ko-Pa Resort and Casino, Fountain Hills, Arizona www.imaps.org/DevicePackaging
APRIL	4-18-18	4-20-18	CICMT 2018 (PORTUGAL) University of Aveiro Aveiro, Portugal www.imaps.org/ceramics
MAY	5-1-18	5-1-18	IMAPS New England - 45th Symposium & Expo Boxborough, MA www.imapsne.org
	5-8-18	5-10-18	HiTEC 2018 - High Temperature Electronics Albuquerque, New Mexico www.imaps.org/hitec
OCTOBER	10-8-18	10-11-18	IMAPS 2018 - Pasadena Pasadena, CA www.imaps.org/imaps2018

Visit www.imaps.org

for links to all upcoming events including:

- **full event descriptions**
- **abstract submissions**
- **exhibition information**
- **event updates**



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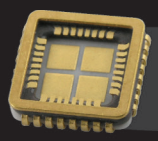

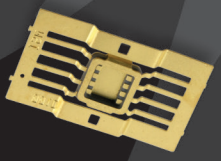

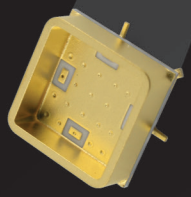

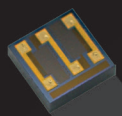

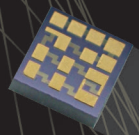

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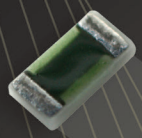

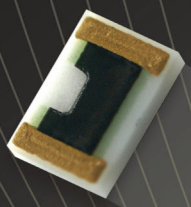

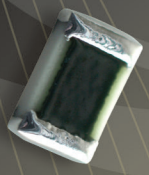

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