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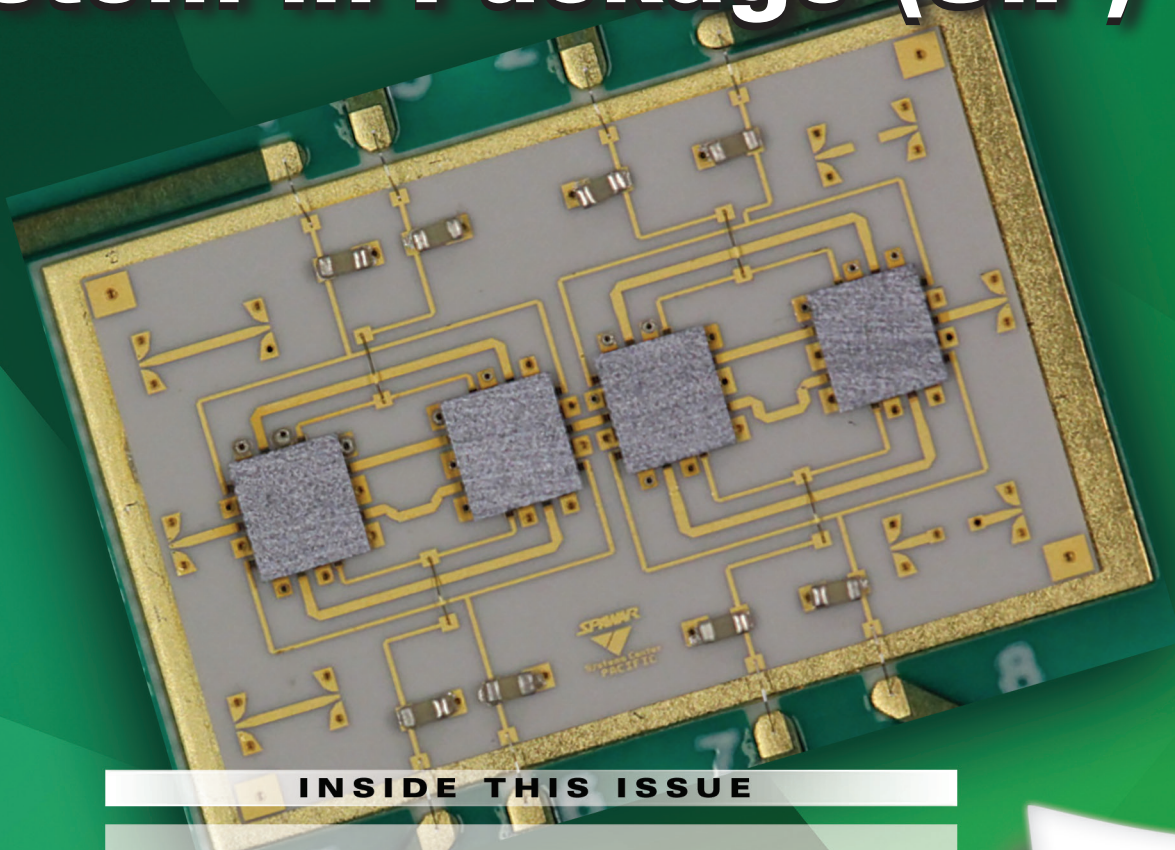
MICROELECTRONICS

EVERYTHING IN ELECTRONICS BETWEEN THE CHIP AND THE SYSTEM!

MAY/JUNE 2018

Vol. 45 No. 3

Heterogeneous Integration – System in Package (SiP)



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PASADENA

51st International Symposium on Microelectronics

October 8-11, 2018

Pasadena Convention Center



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The 51st International Symposium on Microelectronics is being organized by the International Microelectronics Assembly and Packaging Society (IMAPS). The IMAPS 2018 Technical Committee seeks original papers that present progress on technologies throughout the entire microelectronics/packaging supply chain. The Symposium will feature 5 technical tracks, plus our Interactive Poster Session, that span the three days of sessions on:

TRACK 1: SiP/SiM (System Solutions)	TRACK 2: Wafer Level/Panel Level (Advanced RDL)	TRACK 3: High Performance / High Reliability	TRACK 4: Flip Chip/2.5D/3D/ Optical (Advanced Package)	TRACK 5: Advanced Process and Materials (Enabling Technologies)
PLANNED SESSIONS: • System Design & Integration • CPI and Modeling • Embedded/High Voltage • Optical / Automotive • Wearable / Test	PLANNED SESSIONS: • Wafer-level Fan Out • WLCSP • Advanced Fan Out • Panel-level Fan Out • MEMS & Sensors	PLANNED SESSIONS: • High Reliability in Defense and Aerospace • MM Wave / High-speed Packaging • RF / Wireless Components • High Reliability in Bio/Medical • High Reliability in Extreme Environments	PLANNED SESSIONS: • Large Body / Small Body FC • 2.5D Technologies • Optical • BUMP & Interconnect • 3D Technologies	PLANNED SESSIONS: • Substrate Technology • Polymer Materials & Processes • Novel Materials & Processes • Advanced Wirebond • Advanced Equipment & Additive Manufacturing
TRACK 6: INTERACTIVE POSTER SESSION - "Posters & Pizza Lunch"				

PROGRAM AVAILABLE SOON: www.imaps2018.org

EXHIBITS FILLING FAST! *Phase II Application Period for Returning IMAPS 2017 Exhibitors Opened February 15th*
Phase III Open Application Period Begins at 12PM Eastern April 2nd

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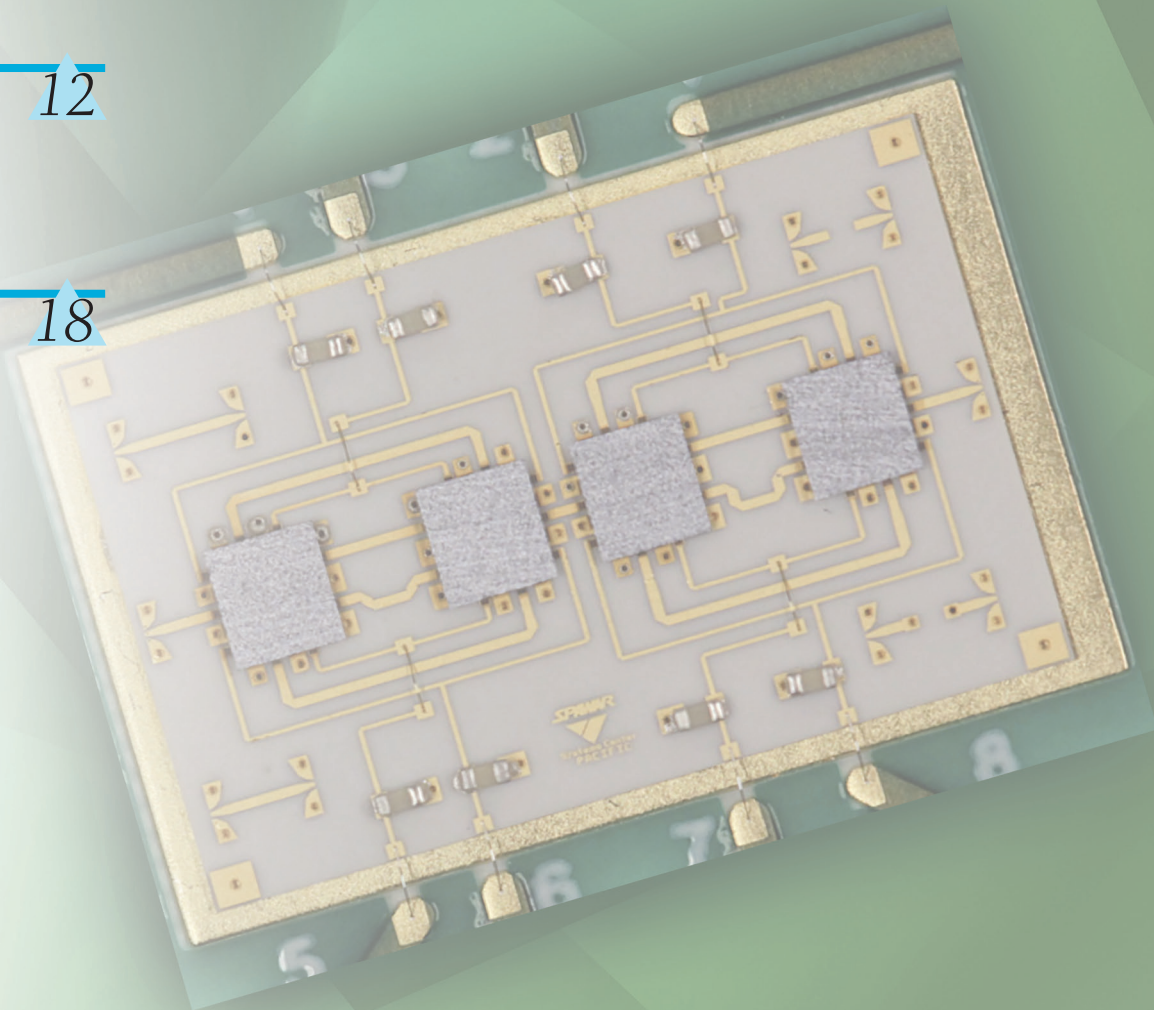
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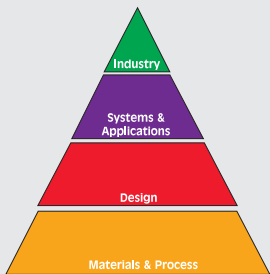
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4-bit E-band phase shifter module
with 4 flip-chip SP4T



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May 1, 2018 Boxborough, MA

HiTEC 2018 - High Temperature Electronics

May 8-10, 2018 Albuquerque, New Mexico

Topical Workshop & Tabletop Exhibition on Wire Bonding

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Nozad Karim
Vice President of SiP/Systems
and Electrical Engineering,
Amkor Technology

Advanced System in Package Technologies

The term advanced System in Package (SiP) covers two broad industry segments of microelectronic system design and system integration in a package. The current trend is to integrate a full system or subsystem into an extremely miniaturized (smaller X, Y, Z dimensions) package structure with high system functional performance, mechanical reliability, and thermal management as well as high yield manufacturability. Advanced SiP terminology is an umbrella term to cover a variety of SiP subsets such as laminate/glass/ceramic/silicon/leadframe-based SiP, fanout SiP, heterogeneous integration, 2.5D/3D SiP and modules.

The need for SiP has driven the entire semiconductor, packaging, design chain and supply chain industries to develop advanced technologies that can address the increasing requirements for cost reduction, size reduction and performance enhancement for electronic systems. As a result, the industry is experiencing close cooperation across the entire SiP food chain from material, substrate and manufacturing equipment suppliers, silicon foundries, design houses, integrated device manufacturers (IDMs), fabless, original equipment manufacturers (OEMs), and electronics manufacturing services (EMS) to outsourced semiconductor assembly and test (OSAT) suppliers. This type of high-level collaboration and knowledge sharing is expediting an exponential growth in the advanced SiP market and creating reliable and cost-effective system solutions.

In addition to the size reduction, horizontal components placement (on-board integration) has been moving toward on-package integration using vertical stacking and interconnections and replacing pre-packaged active components with silicon bare dice, low capacitive interconnect structures to reduce power and enhance signal integrity. Advancements in laminate technology from finer line and spacing, smaller via diameter and sub 100- μm thick laminate stack-up, reduction in mold cap thickness with very low particles size for mold underfill, and fine pitch flip chip (FPFC) to copper pillar technology have all made their way into mass production. Laminate-based SiP technology is in a front-runner position and the most popular SiP solution for cellular, Internet of Things (IoT), power, automotive, networking and computing system integrations.

Filters and passive components have become a dominant part of radio packaging with the next generation of 5G technology possibly requiring 50+ filters. This huge increase in passive components quantities is limiting package size reductions. Integrated passive components in silicon or glass is one way to reduce the number of

filters and passive components in a system. Wafer Level Packaging (WLP) has experienced good progress as an alternative solution to the laminate-based SiP. Millimeter wave radio design with beam forming and array antenna will be used in several varieties of advanced SiP products for 5G cellular systems. Millimeter electromagnetic wave design imposes new challenges for system designers as well as components and SiP packaging engineers.

In this issue, we have chosen three papers that characterize microelectronic system design and system integration in package challenges.

The first paper explores 3D integrated passive devices (IPDs) on glass substrates, illustrating a 3D RF front-end filter design with high-Q solenoid inductors using a conformal copper (Cu) plating method, through glass vias (TGVs) and Cu silicon-nitride (SiN) Cu metal-insulator-metal (MIM) capacitors. Glass substrates have a low dielectric constant, high resistivity, high modulus of elasticity, and adjustable coefficient of thermal expansion (CTE), making them a good solution for passive component size reductions.

The second paper compares different wafer level packaging approaches for producing low RF-loss interposers and populating them using die-to-die (D2D) or die-to-wafer (D2W) bonding of the monolithic microwave integrated circuit (MMIC) components on gallium arsenide (GaAs) with the RF passives produced on an interposer, followed by wafer-level encapsulation. The authors compare RF performance of the D2W mounting and the encapsulation before the Si interposer is thinned for TSVs to the interposer thinning prior to the mounting.

The authors of the third paper developed a low-cost 4-bit passive phase shifter using commercial off-the-shelf components as an integral part of a phase array to be used in millimeter-wave communications. The schematic of the phase shifter utilizes four single-pole, four-throw (SP4T) MMICs in series mounted on a thin two layer alumina substrate using a coplanar waveguide transmission line. The authors also provide a technology comparison with other state-of-the-art E-band and W-band phase shifters including InGaAs, CMOS and microelectromechanical systems (MEMS) designs.

In 2017, IMAPS established a new System in Package conference totally focused on SiP technology developments and solutions, technology and business trends. The next System in Package (SiP) Technology Conference and Exhibition is planned for June 2019 in Monterey, California.



Advanced System-in Package (SiP) Conference and Exhibition 2019

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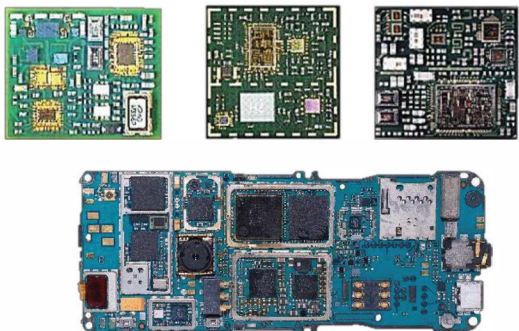
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For more details and to participate, contact Brian Schieman at bschieman@imaps.org

You do not want to miss this one....



Preliminary Program

Opening Keynotes: SiP business and technology trends; SiP challenges for consumer, industrial, automotive and networking products

Technical sessions: System integration challenges for cellphone, IoT, consumer, automotive, computing and networking products

Start up sessions

Interactive Panel sessions

Table top exhibits

And much, much more

3D IPD on Thru Glass Via Substrate using Panel Manufacturing Technology

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Abstract

As electronic products become smaller and thinner with an increasing number of functions, the demand for high density and high integration becomes stronger. Glass has many properties that make it an ideal substrate for high integration substrates such as: ultra high resistivity; adjustable thermal expansion (CTE, co-efficient of thermal expansion) high modulus; low dielectric constant; low dielectric loss; and manufacturability with large panel sizes.

Multi-bands with carrier aggregation, Wi-Fi/GPS coexistence, and LTE-U make RF front end more and more complicated. 3D IPD (integrated passive devices) on glass substrate technology could be an advantage solution including reducing power consumption and small form factor.

This paper presents a demonstration of 3D RF front end filters using 3D solenoid inductors with through glass vias (TGV) and Cu-SiN-Cu MIM structure on a Gen1 glass substrate (300mm x 400mm) panel format using a color filter manufacturing line for flat panel display. For inductors, drastic performance (size and low resistance therefore high-quality factor) improvements have been demonstrated by technology evolutions from 3D solenoid using TGV with a conformal Cu plating method, achieving low resistance of 3.1mohm per 70um diameter TGV on a 400um thick glass panel. This low-resistance TGV with 2.7mOhm/sq TGV connections on both sides of the glass substrate, a record high inductor quality factor of 39 was obtained at 2.5GHz using five and half turn inductor of 7.9nH inductance. For capacitors, we have successfully integrated a Cu

MIM (metal-insulator-metal) structure by using 15um thick Cu plates and dielectric, resulting in a high capacitance density of 0.26nF/mm² for RF applications. By integrating TGV inductor-first and MIM capacitor-next, high-performance and high-density LC components are synthesized to perform as RF front end filters such as low-pass filters, diplexers, triplexers, and multiplexers.

The 3D inductors, Cu MIM, LC resonators and filters were successfully integrated using glass panel manufacturing infrastructure for the first time. Process characterization and process control monitors were evaluated at the panel level to address high-volume and high-yield manufacturability of RF filters with unprecedented filter performance in terms of insertion loss and out of band rejections in smaller form factor than any other technologies have achieved so far. Furthermore, the TGV filters were mounted on electrical evaluation boards as well as JEDEC standard testing boards to check any device-level, chip-level, and board-level reliabilities associated with glass or TGV materials as well as their interaction with Cu, SiN, polymer inter layer dielectric materials, and solder joints, showing no performance degradations during thermal cycling, drop shock, bending, or high-power testing situations.

Key words

3D IPD, TGV, MIM capacitor, silicon nitride, capacitance density, 3D inductor, Q-factor

I. Introduction

As electronic products become smaller and thinner with an increasing number of functions, the demand for high density and high integration becomes stronger. Glass has many properties that make it an ideal substrate for high integration substrates such as: ultra high resistivity; adjustable thermal expansion (CTE, co-efficient of thermal expansion); high modulus; low dielectric constant; low dielectric loss; and manufacturability with large panel sizes. In RF front end (anywhere between the antenna and amplifiers), there are many passive circuits required to provide the best filtering solutions for the multi-band multi-standards. Figure 1 shows a block diagram of a RF front end. Figure 2 shows picture of a RF front end module in a current smart phone. The filtering solution at the

RF front end requires the lowest insertion loss with wide frequency range bands-grouping LC filters, combined with specific band selecting narrow band acoustic filters. Figure 3 shows filter topologies for low-pass filters composed of multiple inductors (L) and capacitors (C), depending on insertion loss and rejection requirements. The low pass filters have been used for power amplifier (PA) modules, filtering out harmonics from the PA. More recently, with the commercialization of carrier aggregation, diplexer (low pass + high pass filters), triplexer (low pass + mid band pass + high pass filters), and multiplexers are becoming more important. The multiplexers are filtering groups of bands (B1, B2, ..., B40) using multiple lumped elements (L and C). Figure 4 shows a current diplexer and triplexer using LTCC technologies.

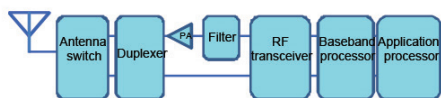


Figure 1. Block diagram of a RF front end.

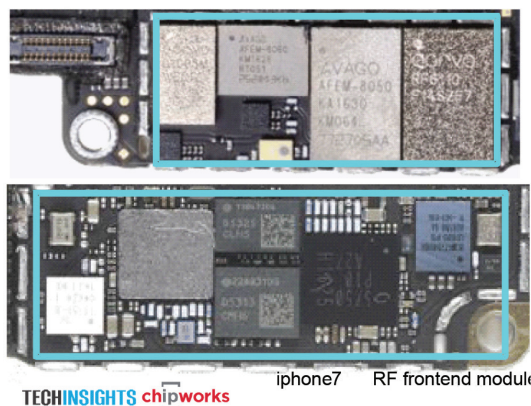


Figure 2. Current solution of RF a front-end module in a smart phone.

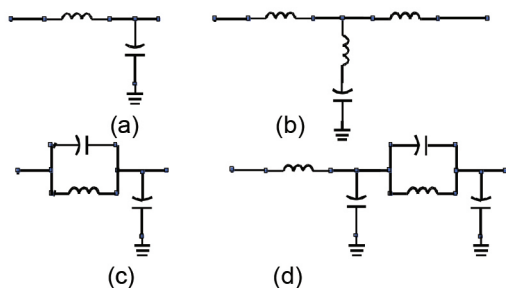


Figure 3. LC-based low-pass filters composed of (a) 1L+1C, (b) 3L+1C, (c) 1L+2C, (d) 2L+3C components.



Figure 4. Current multi bands filters using LTCC.

We have developed 3D IPD using solenoid inductor and MIM capacitor in an 8 inch wafer size glass substrate [1]. Figure 5 shows a 3D IPD chip overview, solenoid inductor model and capacitor model. A result of measurement of inductance of three and half turn inductor was 5nH at 1GHz, and the quality factor was 61.

Figure 6 shows a co-planer waveguide with a comparison of silicon and glass in the high frequency region. The loss is significantly lower in glass substrates than it is in silicon substrates shown in Figure 7. This low loss given by the insulating properties of glass offers the important ability to achieve high Q-factors in filter applications.

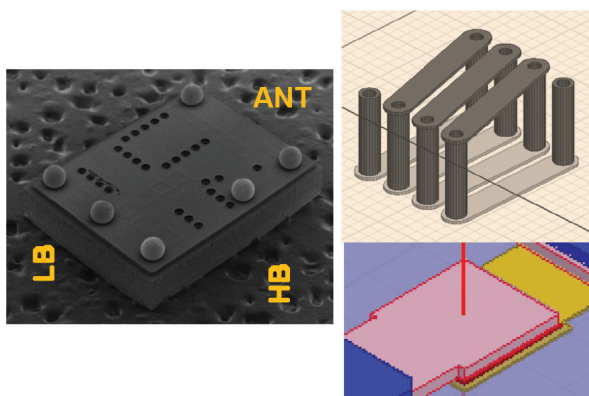


Figure 5. 3D IPD using a solenoid inductor and MIM capacitor.

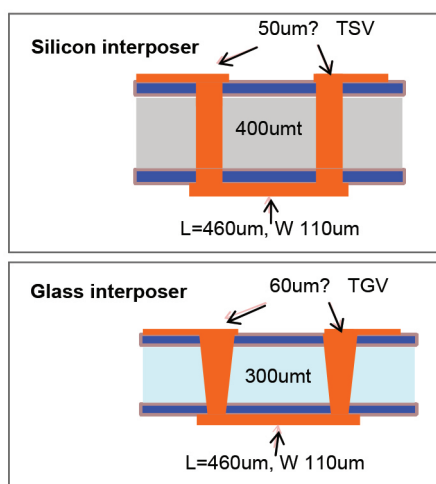


Figure 6. Co-planer waveguide test vehicle.

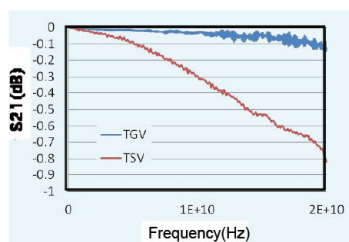


Figure 7. Measurement result of transmission (S21).

This work will mainly focus on the recent achievements in design and technology demonstration for both high-Q L components using panel Manufacturing Technology platform.

II. TGV Passives Process

TGV glass process

Over the past several years, there have been significant advances in the ability to provide high quality vias in glass substrates. The work described here utilized glass with a thickness of ~0.4 mm and through glass via (TGV) diameter of 85 um.

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TGVs of 200 μm in pitch were formed on alkali-free glass by Asahi Glass corporation with Focused Electrical Discharging Method (FEDM). Mainly it consists of two steps of that focused and controlled electrical discharging created locally molten regions of glass, and finally it induced dielectric breakdown together with internal high pressure by Joule heat and ejection of glass[2].

Figure 8 shows the result of TGV formation for 300 μm thick glass. In the case of TGV for 300 μm thick glass, the top diameter is approximately 60 μm and the bottom diameter is approximately 40 μm . The TGV side wall was smoothed by fine polishing because the process using electrical discharging made glass locally heated and melted by high temperature.

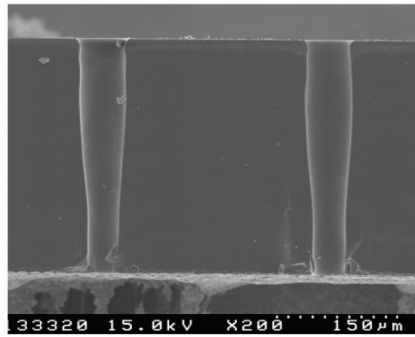


Figure 8. Cross sectional view of via formation FEDM.

TGV IPD (integrated passive devices) integration

The process flow of TGV and IPD integration is shown in Figure 9. First of all, TGVs of 85 μm in diameter and 150-200 μm in pitch were formed on a 400 μm thick alkali-free glass wafer.

50nm Ti and 1000nm Cu layers were deposited as Cu seed materials. Then the TGV sidewall and front side and backside metal layers were formed with 15mm Cu thickness by conformal electroplating. By this time, functional 3D TGV inductors and capacitors were formed.

The conformal plating method has great advantage of process time of plating. The key requirement for conformal plating method is coverage of the seed metal layer in the vias. [3].

In Figure 9 our sputtering system was at an optimized angle for 400 mm deep via metalized on a Gen1 glass substrate (300mm x 400mm) panel format. Figure 10 shows profile after seed layer deposition. Figure 11 shows the result of X-ray inspection after seed layer deposition. Conformal Cu via in 300x400mm panel format was successfully achieved by electroplating shown in Figure 12. Figure 13 shows an X-ray image of conformal plating with 15mm thick Cu. The X-ray inspection shows that TGV interconnects were successfully formed for an inductor.

A thick dielectric polymer layer was laminated on the glass panels as RDL passivation film using photosensitive polyimide followed by a low temperature cure of 210 degrees Celsius. Redistribution lines were patterned with negative dry film photo resist. Cu RDL line of 15 mm thickness was deposited by Cu-electroplating followed by photo resist and Cu seed layer removal.

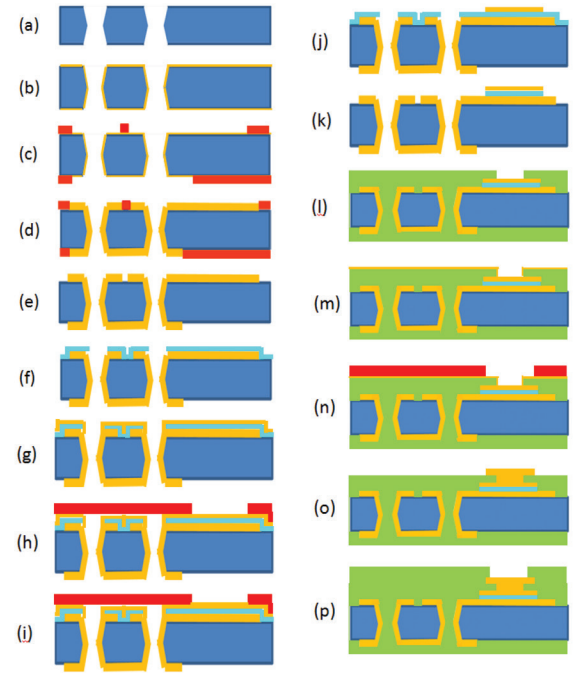


Figure 9. TGV IPD process flow: (a) starting TGV glass wafer; (b) seed layer deposition front side, backside and inner hole; (c) inductor formation by patterning; (d) plating front side, backside, and TGV sidewall simultaneously; (e) seed layer etching; (f) inorganic membrane deposition for capacitance; (g) seed layer deposition front side; (h) lithograph for upper electrode formation; (i) plating for upper electrode of capacitance; (j) remove resist pattern and seed layer etching; (k) inorganic membrane etching; (l) front side and backside interlayer dielectric pattern; (m) seed layer deposition for Pad metal; (n) lithograph for Pad formation. (o) plating for final Cu interconnects and pads; (p) solder resist formation around the I/O pads.

The TGV IPD panels were then ball-attached on the solder mask openings and diced individually using laser dicing methods.

Figure 14 shows resistance distribution of conformal TGV. Average resistance of via is 2.7mohm [4].

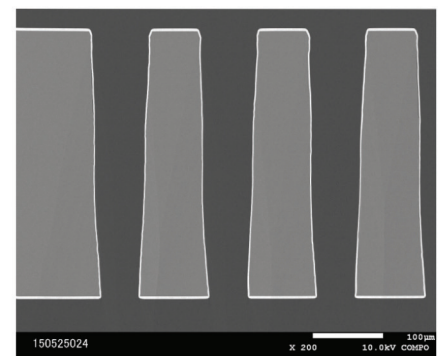


Figure 10. Profile of fabricated TGV after seed layer deposition.

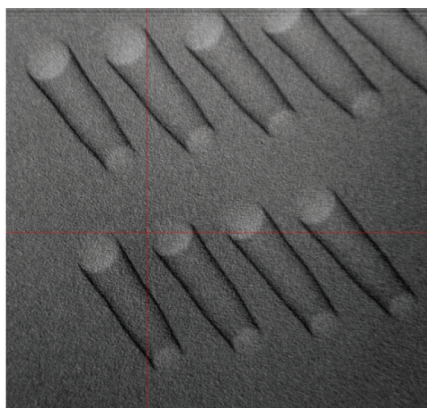


Figure 11. X-ray inspection result after seed layer deposition.

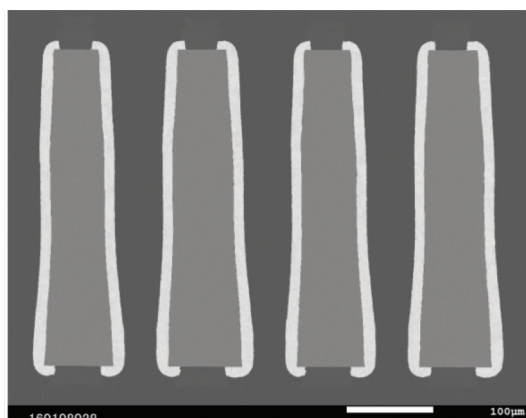


Figure 12. Fabricated Cu wiring by SAP.

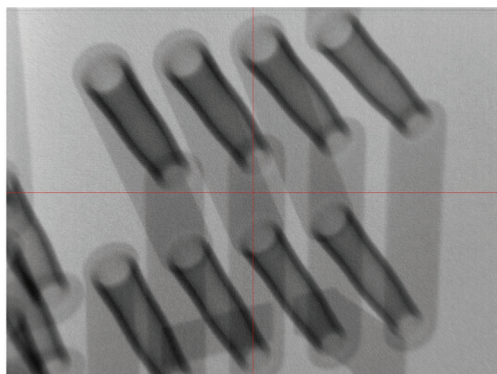


Figure 13. X-ray image of fabricated TGV for an inductor.

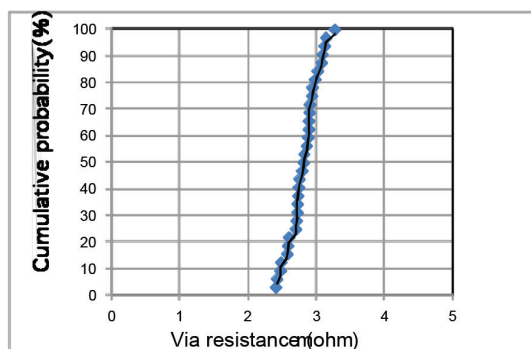


Figure 14. Resistance distribution of conformal TGV.

Figure 15 shows appearance of capacitor TEG (test element groups). The X-section of MIM structure is shown in Figure 16. Figure 17 shows a SEM picture of a fabricated MIM capacitor. Figure 18 shows the capacitance density of a MIM capacitor. Average capacitance density is 0.26 nF/mm².

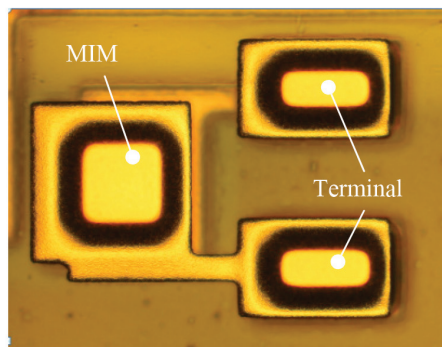


Figure 15. Capacitance of TEG.



Figure 16. X-section of MIM structure.

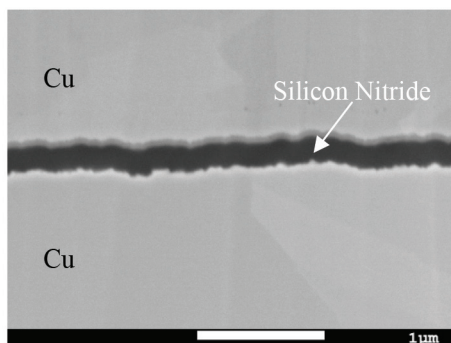


Figure 17. SEM image of a fabricated MIM capacitor.

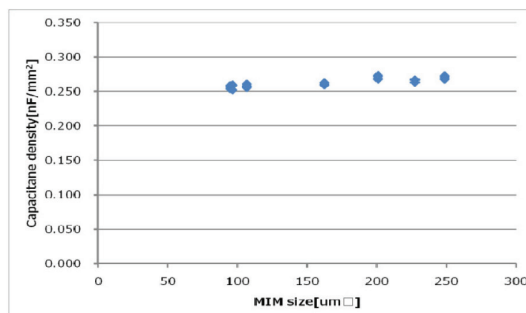


Figure 18. Capacitance density of a MIM capacitor.

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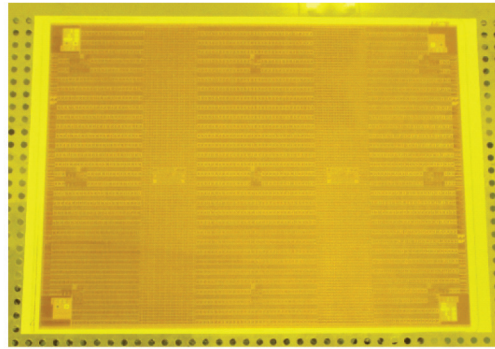


Figure 19. Fabricated Gen1 300x400mm panel.

Figure 19 shows the appearance of a fabricated 300x400mm panel until final I/O pad formation. There are not any problems to fabricate Gen1 Glass substrate (300mm x 400mm) panel format. Furthermore, manufacturing processes to form glass in thin large sheets of high quality is mature and gives an opportunity to reduce cost through economies of scale.

High frequency characteristics

High frequency characteristics were measured by a vector network analyzer. Figure 20 shows measurement test element groups (TEG) for high frequency. For the 400 μ m thick glass panel, we measured an inductance of 7.9nH at a frequency of 1 GHz and a peak Q factor of 39 at a frequency of 2.5GHz, while for the 300 μ m thick glass panel, we measured an inductance of 6.2nH at a frequency of 1 GHz and a peak Q factor of 68 at a frequency of 2GHz.

Glass has a number of attributes that make it an excellent substrate for RF applications. Since glass is an insulating material, its electrical properties provide a low loss substrate for high-Q inductors. The ability to generate well-formed through vias has been demonstrated.

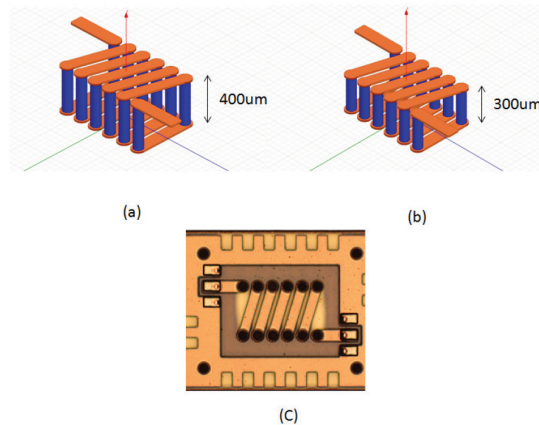


Figure 20. Measurement of TEG of five and half turn inductor.

Conclusion

This paper presents a demonstration of 3D RF front end filters using a 3D solenoid inductor and capacitor with through glass vias (TGV) on a Gen1 Glass substrate (300mm x 400mm) panel format. For inductors, drastic performance (size and low resistance therefore high-quality factor) improvement has been demonstrated by technology evolutions from 3D solenoid using TGV with conformal Cu plating method, achieving low resistance of 2.7mohm per 70 μ m diameter TGV on a 400 μ m thick glass panel. Additionally, we measured a capacitance density of 0.26nF/mm² for a large panel size. For the 400 μ m thick glass panel, we measured an inductance of 7.9nH at a frequency of 1 GHz and a peak Q factor of 39 at a frequency of 2.5GHz, while for the 300 μ m thick glass panel, we measured an inductance of 6.2nH at a frequency of 1 GHz and a peak Q factor of 68 at a frequency of 2GHz. Therefore the TGV IPD process enables production of RF modules with a Gen1 glass size.

Acknowledgment

The authors would like to thank Asahi Glass Corporation for supplied glass substrates with TGVs.

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Investigation of Wafer Level Packaging Schemes for 3D RF Interposer Multi-Chip Module

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Abstract

Very small RF modules can be realized through heterogeneous integration of GaAs MMIC (monolithic microwave integrated circuit) onto a low loss Si sub-mount, with high density routing lines realized by advanced patterning. In this paper we investigate how to integrate MMIC active devices on GaAs with the RF passives produced on an interposer, using Si wafer process technology. High resistive silicon substrates are required to minimize RF losses. The interposer is thinned below 100 μm to reveal Cu TSVs from the back of the interposer, while the front side is covered entirely with a silicon capping wafer for shielding the device. We compare different wafer level packaging approaches for producing the low RF-loss interposers, and populating them using die-to-die (D2D) or die-to-wafer (D2W) bonding of the MMIC components, followed by wafer level encapsulation. Two D2W approaches are compared. In the first approach the D2W mounting and the encapsulation happens before the Si interposer is thinned for TSV reveal. To avoid damage during thinning of the wafer, thicker substrates with deeper TSV of 150 μm or more are required. In a second approach, the thinning of the interposer is done prior to the mounting. Initial electrical data showed that the approach yielded proper RF performance, but further yield optimization is required.

Key words

high resistive silicon, integrated passive devices, RF interposer, through silicon via, wafer level bonding

I. Introduction

High quality RF MMIC components are commercially produced on small substrate size GaAs wafers in specialized fabs. The GaAs technology for high performance RF active devices are combined with mainstream CMOS 200 mm Si wafers technology, using heterogeneous integration of MMIC components on a Si interposer. In this work, the passive RF components (like filters and matching circuits) are integrated on the Si interposer. We aim to integrate the MMIC and Si interposer for RF applications in the range of 5 to 40 GHz.

The heterogeneous integration of the MMIC on the silicon interposer can be done at die level or on a 200 mm wafer base using the 2.5D and 3D integration[1] technologies that are well established on 200 mm Si wafers. The MMIC dies are then populated on the 200 mm interposer. The interposer consists of several metal levels for the passive devices, and TSVs that enable the backside contacting/mounting. The entire system is capped with a silicon wafer with 350 μm deep cavities over the MMIC.

II. Device Description

Figure 1 schematically shows the target structure with a MMIC that is mounted on the Si interposer. TSVs on the MMIC device make the connection between front of the interposer and front of the MMIC. The interposer itself consists of a TSV level, two metal levels connected by a vertical interconnect (via), and a metal-insulator-metal capacitor structure between the 2 metal levels. The top layer is finished with aluminum bond pads for probing, and Cu/Ni/Sn micro-bumps for bonding the MMIC device. A sealing ring is also designed in this Cu/Ni/Sn layer and is used to bond to the silicon cap wafers.

The cap wafer consists of 350 μm cavities to fit over the MMIC dies. The entire surface of the cap is metallized with a Cu layer to bond to the Cu/Ni/Sn sealing ring on the interposer.

In order to minimize RF losses arising from the electromagnetic coupling between the passive devices and Si substrate, high resistive silicon is used and the silicon surface is passivated using a semi-insulating poly-silicon (sipos) [2,3] layer. In previous work[4] the line loss of co-planar waveguides (CPW) on different substrates was evaluated. Losses could be minimized to 0.34dB/mm at 40GHz for high resistive wafers with a 75nm sipos layer. The non-passivated or high resistive Si wafers suffer from a much higher loss of 1.5 and 6 dB/mm, respectively.

The electrical response of the passive components, CPW lines, and TSV on the interposer, were evaluated over the frequency range up to 40GHz, and used to build a component library for filter design.

III. Fabrication of Front Side Layers of the Si Interposer

The fabrication process of the interposer wafer starts with the deposition of a 75nm sipos layer to passivate the surface of the 5 kohm-cm high resistive Si wafer. A 1 μm SiO₂ layer is deposited on the sipos, and 20 μm diameter TSVs are etched through these layers and further into the silicon substrate to a depth of 85 μm to 100 μm . TSVs are filled with an oxide liner, tantalum barrier (120 nm), and Cu seed (900 nm). The TSVs are further filled using bottom-up Cu plating[5].

On top of the TSV, at least one metal interconnect layer is processed using Cu damascene technology. One metal layer suffices for a simple interposer with CPW line inter-

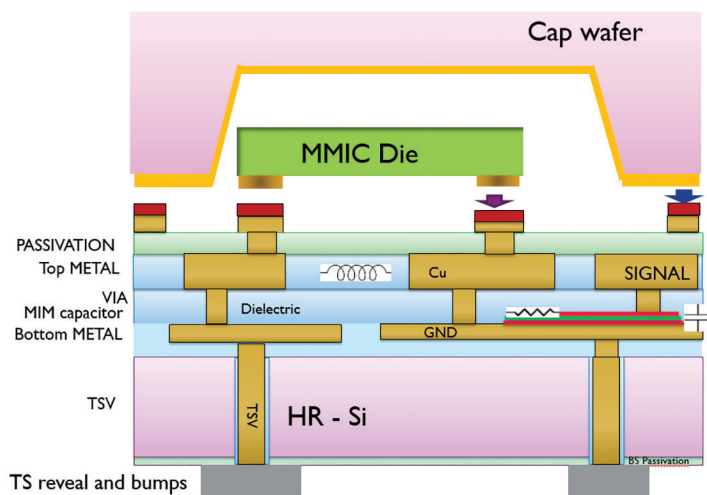


Figure 1: Schematic cross-sectional view on the device.

connects. An interposer with matching circuits, or filters made of inductors and capacitors, needs at least one extra metal level, and a metal-insulator-metal capacitor structure. The top metal is a 2 μm thick Cu layer. This top layer is made extra thick to minimize resistance. It serves as the main conducting layer for the coils and RF lines. The stack is then passivated by a $\text{SiC}/\text{SiO}_2/\text{Si}_3\text{N}_4$ passivation stack.

Aluminum bond pads connect to the top Cu layer through an opening etched in the passivation stack. Another passivation opening is done for connecting the micro-bumps. These bumps are made of 2 μm Cu, 1 μm Ni, and 5 μm Sn layers and are 80 μm wide. In the same process a 100 μm wide Cu/Ni/Sn sealing ring is formed around the dies, for bonding to the cap wafer.

After front side processing is completed, the wafer will follow different routes, depending on the packaging flow selected.

IV. Die and Wafer Level Packaging Options

We compare different assembly options for the mounting of the MMIC and cap on the interposer. The simplest approach is the die-to-die bonding of both MMIC dies and the cap. The downside of this approach is that it is less scalable to large volumes, because dies need to be handled individually. Wafer level approaches involve extra process complexity but potentially reduce on the amount of package manipulation and parallelize the bonding steps.

A. Package level assembly

Once front-side processing is completed, the wafers continue for thinning, TSV reveal, and backside pad processing.

The thinning is done by edge trim, followed by wafer bonding to a blanket Si wafer using Brewer Bond BB305 glue[6]. The glue material is compatible with temperatures up to 300°C. After bonding, the device wafer is thinned by wafer grinding, stopping 5 to 10 μm before the TSV is reached. The final TSV reveal is done by silicon wet etch. The etch is selective to the oxide liner that covers the TSV bottom and sidewall. A 200 nm Si_3N_4 passivation layer is deposited by CVD at low temperature (200°C). This Nitride, the SiO_2 TSV liner, and barriers are then opened

by dry etch using a litho mask that only reveals the TSV top. The backside processing is either finished by processing of Aluminum probing pads, or by Cu/Ni/Sn micro-bumps. The wafer is now ready for debonding from the carrier and ready for dicing.

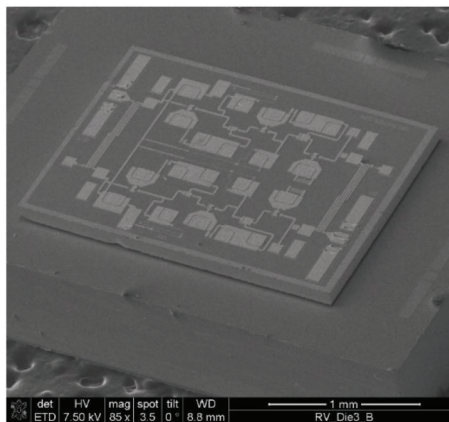


Figure 2: An MMIC mounted on an Si interposer die.

The first evaluation of RF performance of mounted components was performed on die level. Figure 2 shows the D2D mounting of a GaAs Low Noise Amplifier (LNA) to a silicon interposer. Figure 3 compares the response of an unmounted LNA (left) with a mounted LNA, probed from the backside of the interposer.

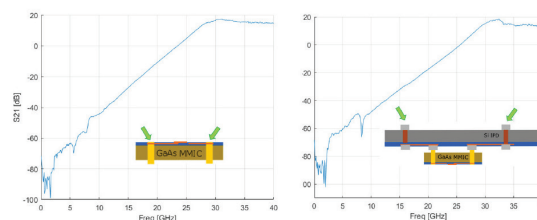


Figure 3: Amplification of RF signal from the LNA without interposer, and on the interposer as measured from backside of interposer.

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B. Interposer thinning at LAST

The first D2W packaging approach starts from the full thickness front side finished wafer described in section III. We mount the MMIC dies on this full thickness interposer wafer. Bonding conditions were determined using micro-bump daisy chain test structures. Figure 4 shows the yield for different bonding conditions with applied forces of 1, 2, or 4 kgf, and with or without applying an underfill material (UF). For each condition, different chain lengths were evaluated. The condition with no UF and 4 kgf had a perfect yield for the 36 measurements at this condition.

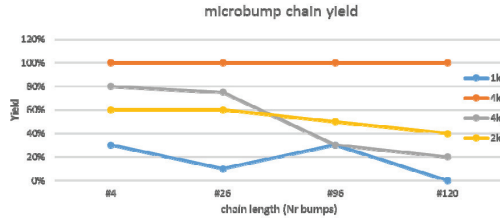


Figure 4: Micro-bump daisy chain yield for different bonding conditions and chain lengths of 4, 26, 96 and 120 links.

After populating all dies onto the wafer, a full 200mm cap wafer can be bonded over the populated wafer (Figure 5 left). With MMIC dies and cap mounted, the wafer needs to be thinned to reveal the TSVs (Figure 5 right). The Cu/Sn bonded cap wafer serves to support the interposer wafer during thinning.

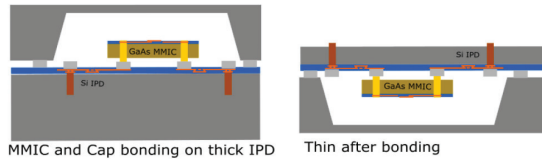


Figure 5: Die and cap bonded on a full thickness interposer substrate with TSV, TSV reveal of the structure by thinning on top of the cap wafer.

Thinning was done by grinding. However, due to the cavities in the cap wafer, the wafer will flex under the force of the grinding wheel, and cracks become visible (Figure 6). Grinding to 100 μm was not successful. Cracks started to occur during the last fine polishing steps. Therefore we concluded that grinding is limited to about 150 μm final Si thickness. In order to enable this approach, the TSV depth has to be increased from 100 to 150 μm or more.

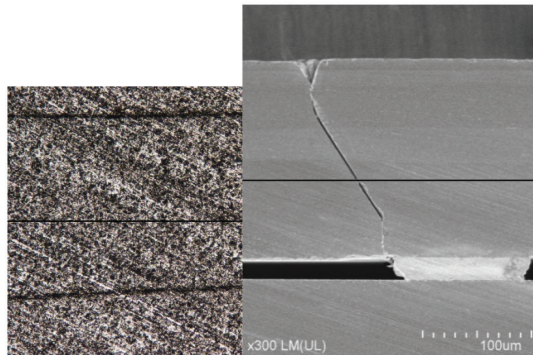


Figure 6: Microscope and cross section SEM image of a crack in wafer after grinding.

C. Interposer thinning at MIDDLE - MMIC on backside IPD

In order to avoid the need to grind the wafer on top of a cap wafer, the interposer wafer can be thinned first, prior to the mounting of the dies and cap. We start from the 725 μm thick wafer with finished front side as described in section III, and continue to wafer thinning and backside processing as would be done for the D2D approach (section IV A), but stopping before the debond and dicing.

At this stage the interposer wafer is face down bonded to a temporary carrier and the backside is on top. We can mount the MMIC and cap on the wafer backside (Figure 7). This requires a design where the MMIC is mounted on the opposite side of the passives, hence the TSVs are in the middle of the RF circuitry, which is not a preferred configuration because it adds parasitic impedances in the critical path of the layout and the passives are on the outside.

Alternatively the passive components can be fabricated on the wafer backside, but this would require a different process flow to make the process flow for the passive components compatible with backside processing and the limited thermal budget of the glue.

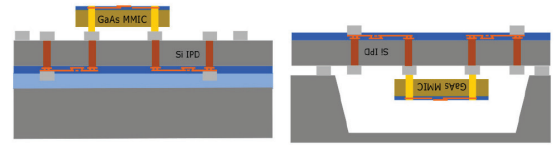


Figure 7: Schematics of thinning before die and cap bonding without wafer flip.

Both D2W of the MMIC and W2W bonding of the cap have to be done on the thinned interposer, glued on a carrier. Due to the softness of the glue material, the thin interposer will deform under the pressure of the bond. This is seen in Figure 8. Optical profilometer measurements show the wafer deformation in case of 2 and 4kgf of bonding force. Deformation of 3 μm and 8 μm , respectively, were observed.

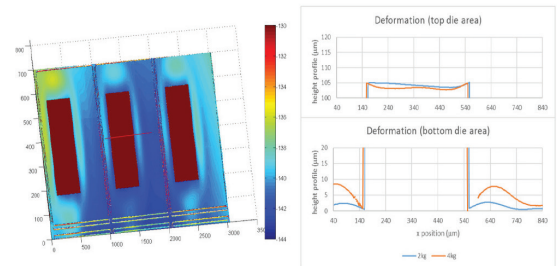


Figure 8: Optical profilometry scan showing the deformation of the surface after D2W bonding on the temporary bonded interposer.

D. Interposer thinning at MIDDLE - MMIC on IPD

The applied solution to get front side of interposer on same side as the MMIC, is to flip back the thinned wafer from one carrier to another, such that the passives are on top again (Figure 9 left). This is achieved by bonding to a second carrier. An experimental glue system was selected that requires a larger debond force than the BB305 glue used for the first carrier. Now the interposer is squeezed in between 2 carrier wafers. Debond peel is used to remove the first carrier which is the weakest bond of the two bonding layers.

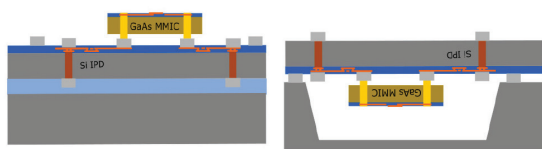


Figure 9: Interposer after wafer flip with passives and MMIC on interposer front side.

Now the side of the interposer with all the passive components is on top again, ready for D2W bonding of MMIC dies, followed by W2W mounting of the cap wafer (Figure 9 right).

Electrical evaluation of the performance of the D2W bond conditions was compared, all bond conditions except for the lowest force, yielded good performance for the daisy chain with 48 micro-bumps (Figure 10). However, the very short chain of 4 links had a low yield. These short chain structures are located at the corner of the die. Further optimization is required to improve yield in die corners.

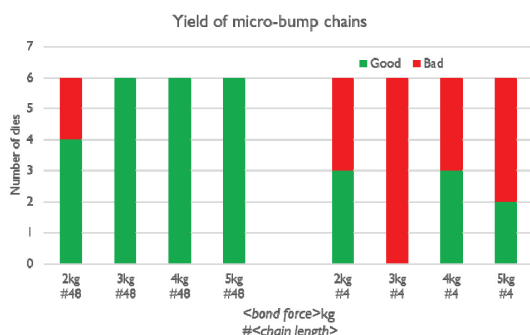


Figure 10: Daisy chain yield.

The verification of RF performance of the D2W process was done with dummy MMIC devices instead of the expensive active GaAs MMICs. The dummies consist of a CPW line on 100 μm thin high resistive Si, with micro-bumps for bonding to the interposer. These devices were measured in RF from the front side of the thinned interposer on carrier, and from the backside, after W2W bonding of the cap. The line loss of the CPW is shown in Figure 11.

To probe from the backside with cap present, the carrier was removed by peel debond. The debond was successfully but some localized damage at the wafer edges was observed.

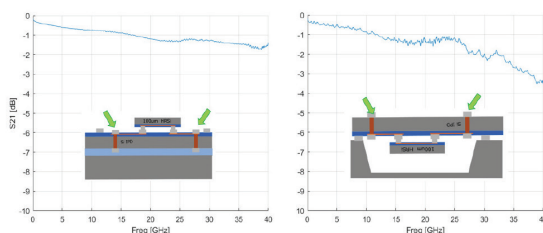


Figure 11: Line losses of CPW line bonded to interposer measured from front without cap (left) and backside, with cap (right), total line length is 3.2mm.

V. Comparison of Packaging Approaches

In this section we compare some approaches for the integration of MMIC components on interposer with a cap wafer (Table 1).

The “package level” approach is a well-established die level process. The “interposer thinning last” route saves the use of a temporary carrier. The MMIC and cap bonding is done on a solid 725 μm 200 mm wafer; the penalty is that the interposer thinning has to be done on a cap wafer with holes which limits the minimal thickness of the substrate.

In both “interposer thinning middle” approaches the thinning on top of a cap is avoided but requires a temporary carrier and bonding on a deformable substrate. In the case of “MMIC on backside,” only one carrier is required but the MMIC will be on the opposite side from the passives. The “MMIC on front” approach adds a wafer flip from the first carrier to a second carrier to the processing, in order to be able to put the MMIC and IPD on the same side. This wafer flip requires an extra carrier wafer and additional process steps.

Comparison packaging approaches	Pros	Contras
Package level	Known process	Sequential process increase cost
Interposer thinning LAST	No temporary carrier required Assembly on rigid wafer	Limitations due to designs/ depth of cavities Need thick substrate/ deep TSV
Interposer thinning MIDDLE, MMIC on backside	Established TSV reveal with temporary carrier	RF module design complicated Subject to parasitics Bond on top of temporary carrier
Interposer thinning MIDDLE, MMIC on front side	Established TSV reveal with temporary carrier	Bond on top of temporary carrier Wafer flip operation required

Table 1: Overview of pros and contras of packaging options

VI. Conclusion

We compared and developed a wafer level packaging flow to integrate GaAs MMIC on Si IPD interposer wafers. Package level process was established and two wafer level integration routes were studied experimentally. The first integration option is to mount the dies on a full thickness interposer wafer and then thin the interposer for TSV reveal. This route is limited by the thinning process due to the cavity wafer used as a cap for the module.

This problem could be avoided by thinning prior to bonding of the MMIC, however. This requires bonding on a thinned wafer that is glued on a carrier. The softness of the glue may result in some deformation that is detrimental to the yield, the layout rules need to be adapted accordingly or the temporary glue needs to withstand higher temperature. Despite such limitations we obtained several

continued from page 15

measurements of active and passive devices showing the potential of the MMIC integration onto HR Si interposer.

Acknowledgments

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E-Band 4-Bit Phase Shifter using SP4T Flip Chip Switches

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Abstract

A 4-bit millimeter-wave switched delay line phase shifter is presented. The phase shifter is designed using commercially available SP4T flip-chip MMICs attached to an alumina substrate. The module operates in the E-Band from 82 – 84 GHz and has an average insertion loss of 20 dB. The size of the module is 10 mm x 7.5 mm. This paper presents a cost effective 4-bit E-Band phase shifter.

Key words

phase shifter, flip chip, packaging, true time delay

I. Introduction

Millimeter-wave communications and radars require beam scanning agility and phased arrays are often preferred. Up-coming 5G cellular systems are anticipating the use of phased arrays [1]. Automotive collision radars already operate in the 77 GHz regime [2], and millimeter-wave wireless communication backhauls typically operate from 71 – 76 GHz and 81 – 86 GHz [3]. Phase shifters are a critical element in the realization of phased arrays, and have been implemented using III-V semiconductor, silicon semiconductor, and MEMS processes [4]-[7]. Passive phase shifters have the benefit of being highly linear, bi-directional, and can be operated single-ended compared to active vector modulator phase shifters. The main drawback is high insertion loss which requires gain compensation. In this paper, we present a low cost 4-bit E-Band phase shifter module using commercial off-the-shelf (COTS) SP4T MMICs on an alumina substrate.

II. Phase Shifter Design

The developed phase shifter is shown in Figure 1. It utilizes 4 SP4T MMIC switches (TGS4306-FC), which are cascaded in series. The switch has a typical insertion loss of 3 dB per state, 20 dB of isolation, and 8 dB typical thru state return loss. In the on state, the switch requires -5V and dissipates no current. In the off state, the switch requires 1.35V and dissipates 10mA. The phase shifter is comprised of 2 stages. In the first stage, 2 sets of switches control phase delays of 0°, 22.5°, 45°, and 67.5° at 85 GHz. The second set of switches control phase delays of 0°, 90°, 180°, and 270°. Figure 1 shows a schematic of the phase shifter. The SP4T switches are mounted onto a

127μm thick alumina substrate ($\epsilon_r = 9.8$, $\delta = 0.0004$). All transmission delay lines are modeled in HFSS and include CPWG launch effects. Ground-signal-ground (GSG) probe pads are used to launch the millimeter-wave signal. Thin 50μm traces provide the SP4T with DC biasing. Since the module has 2 metal layers, bondwires are used as crossovers. This can be seen in Figure 2. The total size of the phase shifter module is 10 mm x 7.5 mm.

Flip-chip MMICs use solder bumps to attach to a substrate. A common problem is for the solder bump to flow onto the landing pad, creating poor bonds and can even cause the chips to detach from the substrate. A solder trough is used to control the solder flow. Figure 3 shows the die picture of the TGS4306-FC, the side profile with the solder bumps, the alumina substrate, and the landing pattern used for the flip-chip.

III. Measurement Results

A custom TRL calibration kit was designed onto the alumina substrate in order to de-embed effects of the GSG probes and CPWG launch. The alumina module was attached to a test printed circuit board which had voltage controls to activate each of the 16 states. An Anritsu ME7808A millimeter-wave vector network analyzer was used for s-parameter measurements. The frequency extension modules have a waveguide output, and so a W281D WR10 to 1.0 mm coaxial adapter was used. A 24cm 1.0 mm coaxial cable was used to connect the frequency extenders to the GGB 100H picoprobes. Figure 4 shows our test setup. Figure 5 shows the measured insertion loss for all 16 states, and as can be seen from 83 – 84 GHz the maximum insertion loss is 22.41 dB and the

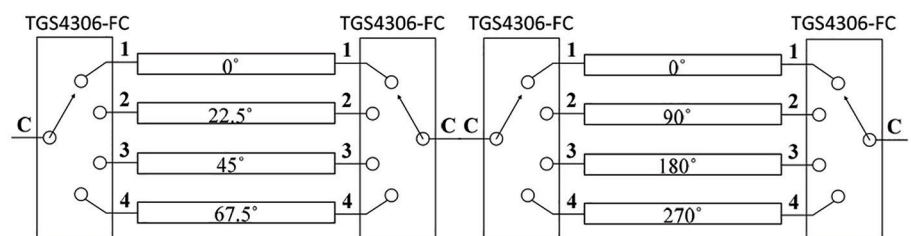


Figure 1. Schematic of 4-bit phase shifter using SP4T switches.

minimum insertion loss is 14.7 dB. Figure 6 shows the measured insertion phase across all 16 states. Since at E-Band the wavelength is small, physically routing the delay lines around the SP4T switch was challenging. In order to route the 45°, 67.5°, 180°, and 270° delay lines, an extra wavelength was added. This results in uneven phase slopes and limits the usable bandwidth of the switched delay line phase shifter and also negates true time delay capability. The SP4T switch is rated from 70 – 90 GHz, however the usable bandwidth of the phase shifter is from 82 – 84 GHz. Figure 7 shows the measured return loss of all 16 states, and as can be seen the return loss is better than 6.91 dB in the usable bandwidth. The main limitation of the input/output match is the intrinsic return loss

of the SP4T. The measured RMS phase error and average insertion loss is shown in Figure 8. The maximum RMS phase error occurs at 84 GHz is 13°, the minimum is 8.8° at 83 GHz. The average insertion loss is 20 dB. Table I shows a technology comparison between some state-of-the-art E/W-Band phase shifters. As can be seen, the performance is inferior to MEMS solutions, but comparable to CMOS solutions. In terms of cost-effectiveness, this design uses COTS parts on a ceramic substrate, and doesn't require integrated circuit level fabrication, reducing the cost dramatically. The main drawback to this design is the size, which limits the level of integration in a phased array, and its insertion loss, which must be compensated.

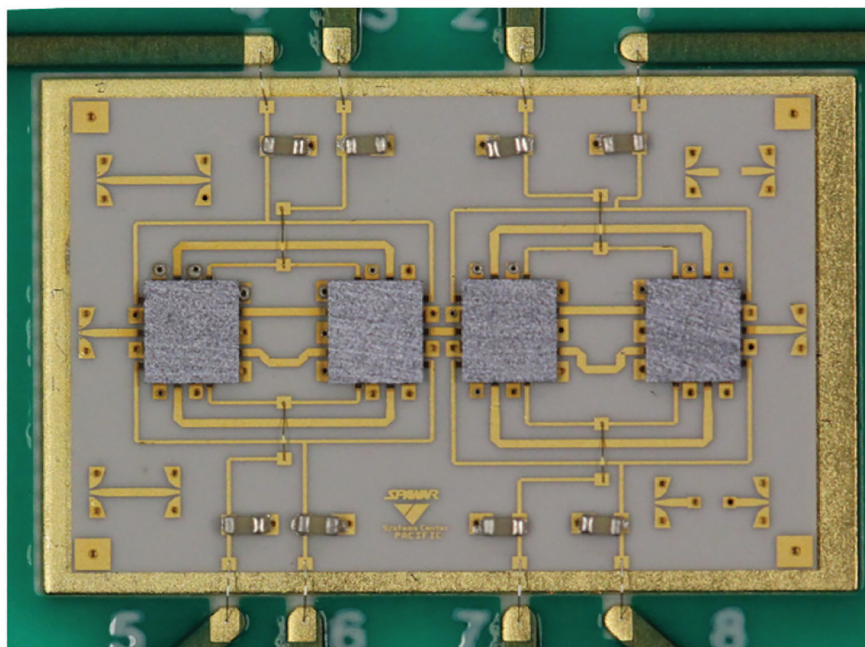


Figure 2. 4-bit E-band phase shifter module with 4 flip-chip SP4T.

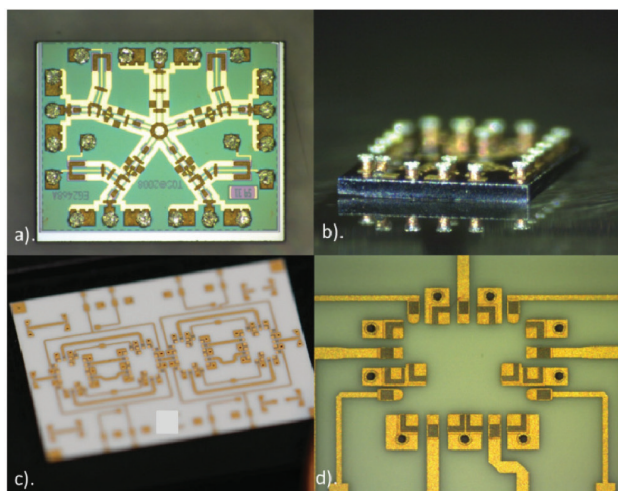


Figure 3. 4-bit E-band phase shifter: a) SP4T MMIC; b) side profile view of MMIC; c) phase shifter module; d) landing pattern for flip chip.

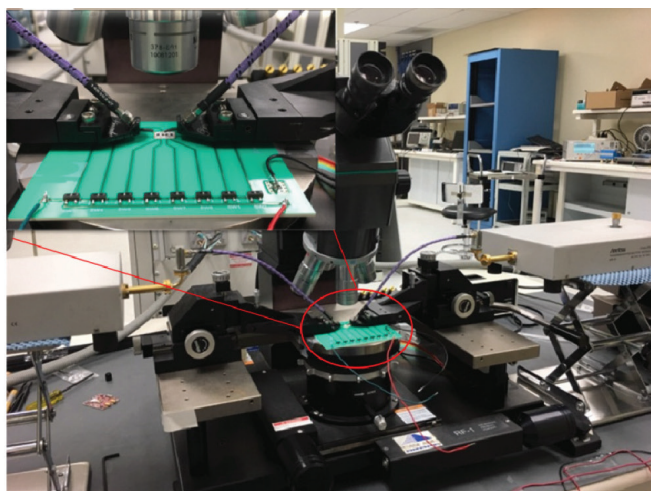


Figure 4. Anritsu ME7808A millimeter-wave test setup.

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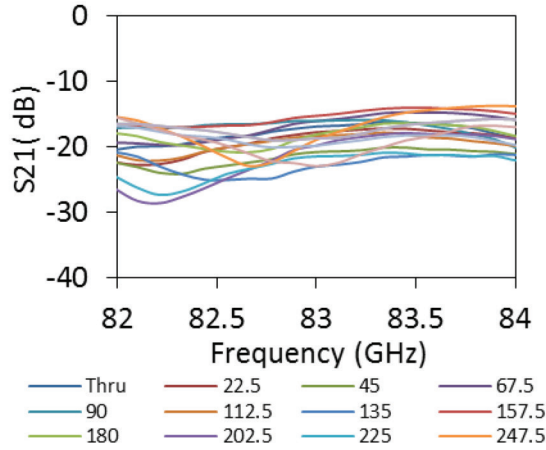


Figure 5. Measured insertion loss of 16 states.

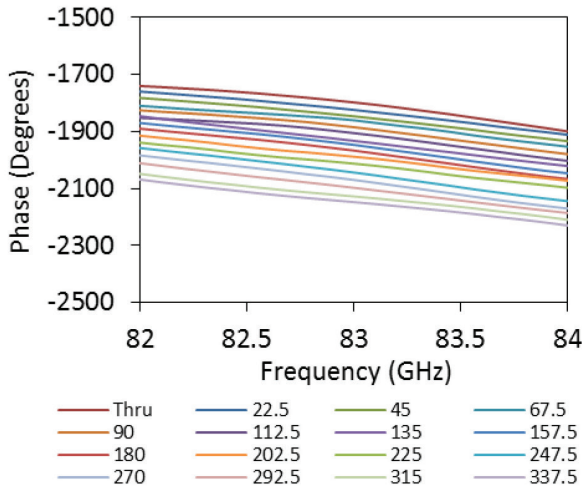


Figure 6. Measured insertion phase of 16 states.

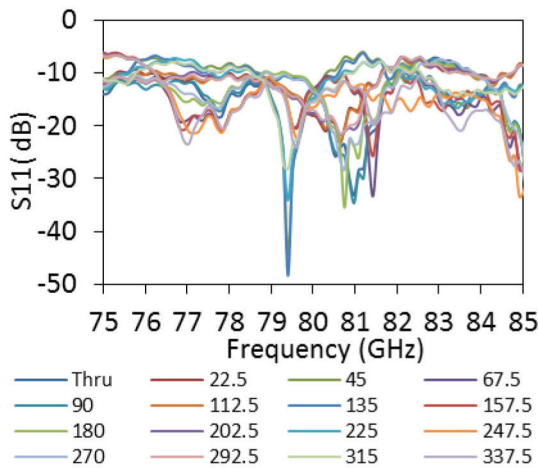


Figure 7. Measured input return loss.

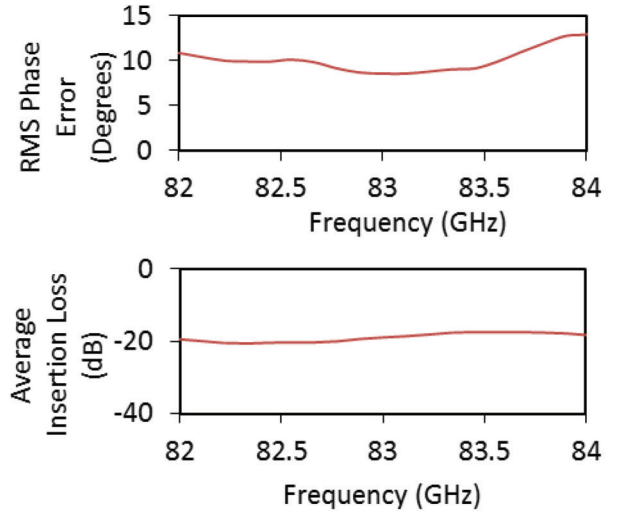


Figure 8. Measured RMS phase error and average insertion loss.

TABLE I
Demonstrated Performance of E/W-Band Phase Shifters

	[4]	[5]	[6]	[7]	This Work
Frequency (GHz)	81 - 85	75 - 85	75 - 110	50-75	82 - 84
Technology	InGaAs	CMOS	MEMS	MEMS	MIC Module
Average Loss (dB)	-12.7	-25	-2.2	-2.5	-20
Bits	4	4	3	2	4
RMS Phase Error (°)	8.2	11.25	3	1	13

IV. Conclusion

We have demonstrated a low cost E-Band 4-bit phase shifter using COTS SP4T switches on a alumina substrate. The phase shifter achieves an average insertion loss of 20 dB and has a RMS phase error of 13°. The total power dissipation of the phase shifter is 55mA.

Acknowledgment

This work is supported by the Office of Naval Research (ONR) under N0001417WX01023.

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Scenes from Device Packaging



IMAPS DPC 2018 CREW



Phil Garrou - Opening Keynote Speaker at IMAPS DPC 2018



Native American performers at DPC.



Francoise Von Trapp, et al., and 3D InCites donated \$3,000 to the Microelectronics Foundation. Many thanks 3D InCites.



Raja Swaminathan - Keynote Speaker at IMAPS DPC 2018

**Save the Date for
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March 4-7, 2019**



Peter Ramm of Fraunhofer EMFT, Munich, and General Chair of the Conference, welcomes attendees and introduces the Conference events.



Announcement and Call for Abstracts

International Conference and Exhibition on High Temperature Electronics (HiTEC)

www.imaps.org/hitec

May 8-10, 2018
Hotel Albuquerque
Albuquerque, New Mexico USA

Overview: HiTEC 2018 continues the tradition of providing the leading biennial conference dedicated to the advancement and dissemination of knowledge of the high temperature electronics industry. Under the organizational sponsorship of the International Microelectronics Assembly and Packaging Society, HiTEC 2018 will be the forum for presenting leading high temperature electronics research results and application requirements. It will also be an opportunity to network with colleagues from around the world working to advance high temperature electronics.

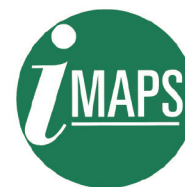
Abstracts being requested include the following topics:

- **Applications:**
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 - Oil well logging
 - Automotive
 - Military/aerospace
 - Space
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 - Solders/Brazes
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- **Energy Sources:**
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 - Capacitors
 - Oscillators
 - Connectors
- **Reliability:**
 - Failure mechanisms
 - Experimental and modeling results

Student Competition sponsored by the Microelectronics Foundation:



The Microelectronics Foundation sponsors **Student Paper Competitions** in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Students submitting their work and identifying that “Yes, I’m a full-time student” on the abstract submission form, will automatically be considered for these competitions. The review committee will evaluate all student papers/posters and award a total of \$1,000 in award checks at the ATW/Conference. The selected student(s) must attend the event to present his or her work and receive the award. For more information on the student competition, go to www.microelectronicsfoundation.org.



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EMPC-2019

European Microelectronics and Packaging Conference

16th – 19th September 2019

Pisa, Italy

www.empc2019.org

The Structures of Microelectronics

EARLY ANNOUNCEMENT – MARK YOUR DIARY

Pisa, the charming city in the famous Tuscany region, is a visitors' paradise with many places of interest to visit. The International Airport "Galileo Galilei" is only 2.7 km away from the Conference Centre. It has become one of the main Italian airports with flights to over 74 destinations all around Europe and globally. It is also a hub for low-cost airlines www.pisa-airport.com.

EMPC-2019 in Pisa offers the best of microelectronics and photonics, packaging and interconnection technologies, providing top quality coverage of technological innovation in this field. The four days will comprise Tutorials/Short Courses and the Conference and Exhibition during 16th to 19th September 2019 at the Palazzo Dei Congressi, an ideal venue which includes excellent lecture auditoria, exhibition space and a great social venue. The event will be complemented by social events for which IMAPS has a great tradition. Pisa, where tradition, art, culture and business meet harmoniously, is ideally also located to extend your visit.

Plan now to prepare your Technical Abstract for EMPC-2019. We will issue a fuller **Call for Abstracts** in June 2018. Included topics are: [Advanced Packaging](#), [Substrate Technologies](#), [Interconnection Technologies](#), [More Than Moore](#), [MEMS and Microsystems](#), [Optoelectronics](#), [Solar Energy and Photovoltaics](#), [Green Electronics](#), [Nano Technologies](#), [Medical Electronics](#), [Power Electronics](#), [Smart Textiles and Wearables](#), [Manufacturing Technologies and Materials](#), [Modelling](#), [Thermal Management](#), [Reliability and Quality](#), [Computing](#), [Applications](#), [Business Aspects](#).

Short Courses / Tutorials

Proposals are invited from professionals to give 3-hour or 6-hour tutorials on the topics of: High Density Circuits, MEMS and Microsystems, Wire Bonding, Soldering Solutions, and other topics relevant to the Conference.

Call for Exhibitors

The EMPC-2019 exhibition will be held from 17-19 September 2019 and will comprise a shell scheme within the exhibition hall at the Palazzo Dei Congressi. Details of bookings and Exhibition Hall layout are obtainable from info@empc2019.org. The Exhibition Hall is positioned adjacent to the technical session rooms to encourage flow into the exhibition. Coffee and meeting tables are also located in the Exhibition Hall.

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Kester Launches NP560 Solder Paste

Itasca, IL, March 12, 2018 — Kester is proud to announce the launch of NP560, a no-clean, lead-free, halogen-free solder paste. It consistently delivers paste transfer efficiencies of 0.50 to 0.55 AR and is fully capable of printing and reflowing 01005 components, even in air, with minimal graping behavior. In addition to its stable, consistent product performance, NP560 has redefined the voiding standard for PCB assembly and has the potential for low voiding performance.

For additional information on this product including technical and safety data sheets, please visit <https://www.kester.com/products/product/np560-solder-paste>.

For any questions or additional information, please contact: Fil Marcial-Hatfield, Global Product Manager at fmarcial@kester.com or Michelle O'Brien, Marketing and Communications Specialist.

Kester is a global supplier of assembly materials for the electronic assembly and semiconductor packaging industries. Kester is focused on delivering innovative, robust and high-quality solutions to help its customers address their technological challenges. Kester's current product portfolio includes soldering attachment materials such as solder paste, soldering chemicals, TSF (tacky solder flux) materials, and metal products such as bar, solid and flux-cored wire. Kester is an Illinois Tool Works (ITW) company. ITW is a Fortune 200 company that produces engineered fasteners and components, equipment and consumable systems, and specialty products. It employs approximately 49,000 people, and is based in Glenview, Illinois, with operations in 57 countries.



Six Master Bond Epoxy Adhesives Tested and Approved for MIL-STD-883J for Thermal Stability

Master Bond is pleased to announce that the following epoxy compounds, EP17HTDA-1, EP21TDCHT, EP33, EP46HT-1AO, Supreme 11AOHT and Supreme 12AOHT-LO, have passed MIL-STD-883J section 3.5.2., the subsection of the United States Military Standards set by the U.S. Department of Defense that refers to the thermal stability of a material. This test indicates a consistent product performance for temperatures up to 200°C.

MIL-STD-883 section 3.8.5 defines that thermal stability testing should be done by performing a thermo-

gravimetric analysis (TGA) according to ASTM D3850. TGA is the study of a material's weight change as a function of temperature and time under a controlled atmosphere. It can be used to determine the thermal stability of a material.

To evaluate the material, samples are placed in a nitrogen atmosphere (20-30mL/min flow). The measurement of the samples start at room temperature (25°C) and then continues as the samples get heated 10°C/min up to a final temperature of 200°C. During this assessment, the weight of the samples is continuously measured. A material passes this standard if the weight loss at 200°C is less than or equal to 1.0 percent of the cured material weight. Three samples are tested and the average value of the three must meet or exceed the minimum requirements.

To date, Master Bond has sent six epoxy adhesives for this test through an independent lab. All six have passed the MIL-STD-883J, Method 5011 (sect. 3.5.2 & 3.8.5), tested in accordance with ASTM D3850.

For a full product description for each of the six products tested, please visit the following pages:

- EP17HTDA-1:
<https://www.masterbond.com/tds/ep17htda-1>
- EP21TDCHT:
<https://www.masterbond.com/tds/ep21tdcht>
- EP33:
<https://www.masterbond.com/tds/ep33>
- EP46HT-1AO:
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For complete information on Master Bond products that passed the MIL-STD-883J test for thermal stability, please visit: <https://www.masterbond.com/certifications/mil-std-883j-thermal-stability>

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INDUSTRY NEWS



Remtec Introduces High Definition Etchable Thick Film (HDTF) Gold Process on Ceramic

Norwood, MA, March 20, 2018 — Remtec Inc. (www.remtec.com), the leading manufacturer of ceramic substrates, packages and submounts using PCTF® (Plated Copper on Thick Film) metallization, has commercialized etchable gold thick film process for High Definition Thick Film (HDTF) circuitry as a low-cost alternative to thin films. Remtec's new offering represents a significant advancement in miniaturization, circuit density and performance.



Remtec's new etchable gold substrates allow the use of ultra-fine lines with a standard line / spacing resolution of 50/50 μm (.002") and premium circuit of 25/25 μm (.001"). Circuit designers can also benefit from Remtec's capability for added value features available on the same

substrate. In addition to an etchable gold circuit, Remtec's HDTF can incorporate conductor multilayers. It also integrates built-in components such as Lang couplers, inductors, filters and high precision resistors in a wide range from 50 m Ω to 1 M Ω laser trimmed to $\pm 1\%$ on the same ceramic base.

Remtec supports the new line of advanced HDTF substrates with new, state-of-the art processing equipment in a class 1000 clean room. Design engineers can also take advantage of Remtec's well-known core competency technologies such as AgENIG® (Electroless Nickel Immersion Gold on Silver) and PCTF® (Plated Copper on Thick Films) metallization in their ceramic package designs.

Typical applications of Remtec's etchable gold HDTF ceramic metallization are for products requiring high circuit density and conductor proximity. HDTF substrates used for high performance products such as mm wave microwave circuits and high pin count analog and digital designs. They are ideal for radar, missile and satellite communications systems in both defense and industrial applications.

Remtec, a RoHS compliant, ISO 90001:2008 registered and ITAR compliant company, operates a manufacturing facility of 33,000 sq. ft. in Norwood, MA. Remtec produces custom and semi-custom packaging solutions for sensors and detectors, RF/MF products, DC power electronics, optoelectronics, laser industry and other high density and power circuitry in commercial, industrial and military industries.

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IN MEMORIAM

STEVEN BURLING

We are sorry to say good-bye to Steve Burling who recently passed away after a massive heart attack. Steve was R&D Manager for Metalor Technologies, a world renowned precious metal company, and also acted as Sales and Marketing Manager, Northern Europe for the Advanced Coatings Business Unit. His responsibilities included the introduction of new precious metal plating processes to European markets as well as liaising with colleagues in the US and the APAC regions. He was also responsible for Global Technology Product Management for products sold in the connector market segment.

Steve graduated from Southbank University in 1978 and in 2017 celebrated 48 years in the metal finishing industry. Steve spent 38 years in the precious metal industry with Engelhard/Metalor. Steve was heavily involved in the electroplating industry and was a member of IMF, NASF, ECS and SSEA. He was president of the International Branch of the NASF. Steve played an active role presenting papers at conferences in Europe, USA, Korea, China and India, including all the SEIA conferences and SURFIN APAC conferences in Singapore.

He will be missed by all his Metalor colleagues and by the electroplating industry.



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General Chair:

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Wire Bonding Workshop Focus:

The objective of the Wire Bonding Workshop is to have a unique forum that brings together scientists, engineers, manufacturing, academia, and business people from around the world who have been working in the area of Wire Bonding. This workshop has been specifically organized to allow for the presentation and debate of some of the latest and hottest technologies out there related to the use of Wire Bonding in semiconductor and microelectronic packaging.

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- Terminal pad structures and modifications
 - Cu/Low-K packaging materials
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- Novel packaging and design
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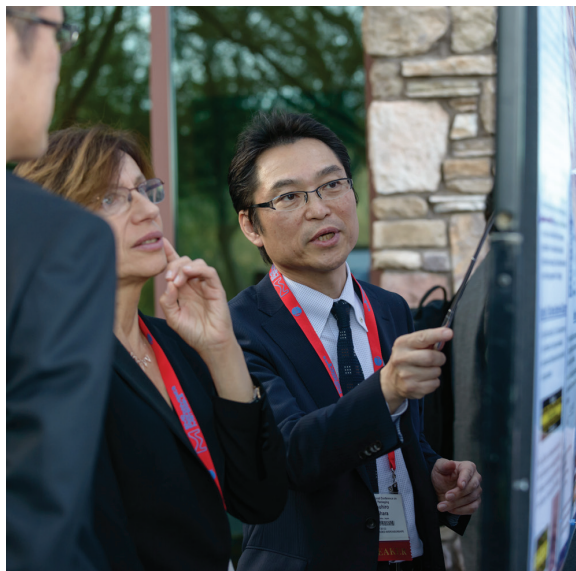
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MARCH 4-7, 2019

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- “Call For Abstracts” begins **NEXT MONTH** - *submit early - space is limited*
- Sponsor & Exhibit “Presale” in **MAY**
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January-February 2018

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Issue	Theme	Copy Deadline	Ad Commitment I/Os Deadline
Jul/Aug	IMAPS 2018 (Pasadena) Show Issue	May 8	May 14
Sep/Oct	Advanced Materials and Additive Manufacturing	Jul. 6	July 13
Nov/Dec	Chip Package Integration (CPI)	Sep. 7	Sep. 13

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Michael O'Donoghue, Executive Director, (919) 293-5300, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction

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CALENDAR OF EVENTS

2018

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start	end	
5-1-18	5-1-18	IMAPS New England - 45th Symposium & Expo Boxborough, MA www.imapsne.org
5-8-18	5-10-18	HiTEC 2018 - High Temperature Electronics Albuquerque, New Mexico www.imaps.org/hitec

OCTOBER

10-8-18	10-8-18	Topical Workshop & Tabletop Exhibition on Wire Bonding Pasadena, CA www.imaps.org/wirebonding
10-8-18	10-11-18	IMAPS 2018 - Pasadena Pasadena, CA www.imaps.org/imaps2018

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- ASP 2017 (Adv. Semi. Pkg) June 15, 2017
- System in Package 2017 June 27-29, 2017
- HITEN - High Temperature July 10-12, 2017
- IMAPS 50th - Raleigh 2017 October 9-12, 2017
- 3D ASP 2017 - 3D Architectures for Heterogeneous Integration & Packaging December 5-7, 2017
- IMAPS 2018 - Pasadena October 8-11, 2018

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