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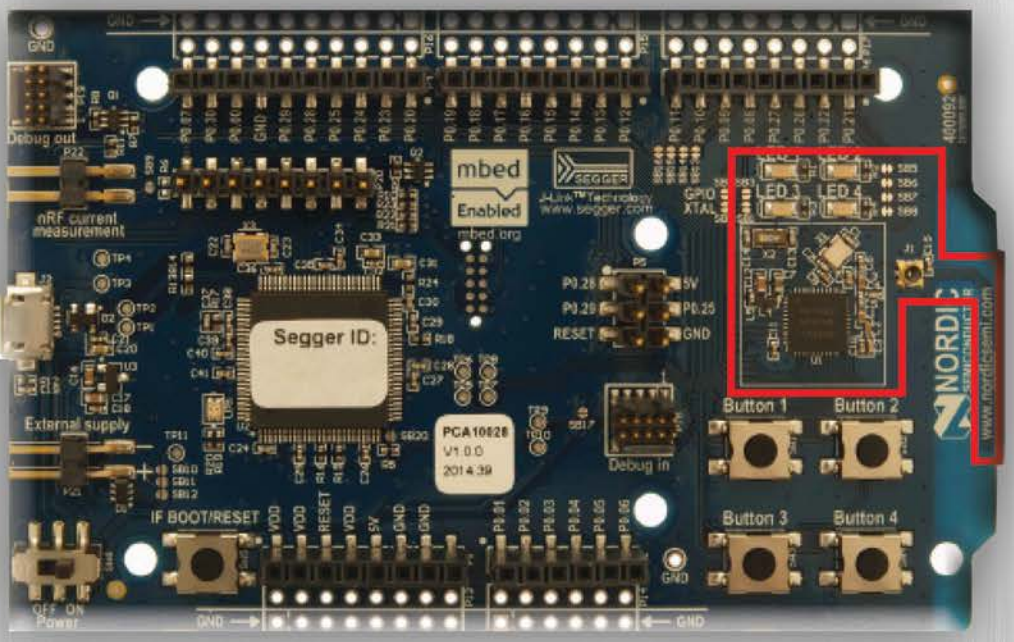
EVERYTHING IN ELECTRONICS BETWEEN THE CHIP AND THE SYSTEM!
MAY/JUNE 2017
Vol. 44 No. 3

Internet of Things



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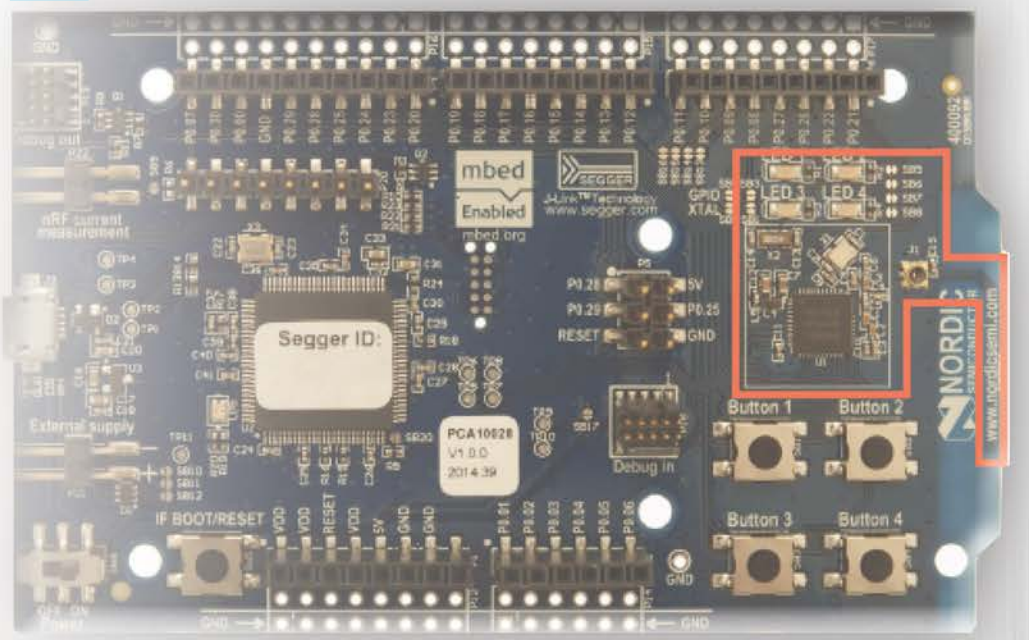

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The Nordic Semiconductor nRF51822 Multiprotocol Bluetooth low energy/2.4 GHz RF SoC is shown. The region in red is being relicated with AJP technology.

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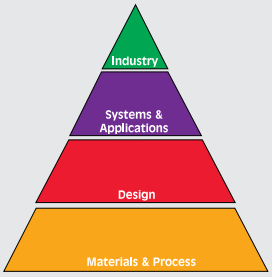

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Tim Jensen,
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Maria Durham,
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Internet of Things ...

In the current industry there have been many discussions related to the Internet of Things (IoT) and it seems like it is becoming more and more discussed. At the International Microelectronics Assembly and Packaging Society (IMAPS) 13th Device Packaging conference in March, many keynote speakers discussed this subject. Not only is it being discussed more but market growth is expected to reach at least 13% over the next 3 years. But is the market really there? It seems like production growth is growing but the market is small, but this can change very quickly.

Some of the electronics technology developments that are driving IoT are in the areas of RF, switches/routers, and servers. This makes complete sense considering the world will need all of these devices communicating data outward and routed, and loads of data will need to be stored.

A couple of hallmark technology developments that will help drive the future are 5G communication, GaN devices and silicon photonics packaging. Keynote Speaker Lionel Rudant from CEA-Leti discussed IoT as well as the up and coming 5G and what is needed for us to get there. Rudant discussed the following: "microelectronics is now led by system-driven roadmaps, and new drivers for 5G systems are diverging IoT services that require innovative flexibility and scalability from the technology." New innovations will continue to need this technology including artificial intelligence, robotics, and new digital user experiences.

All of this technology development will probably impact the transportation markets more than all others. Vehicles are able to effectively communicate outward as well as to one another. The technology will enable the vehicle to collect data on itself and its surroundings and make decisions thousands of times faster than a human driver could. Elon Musk has said, "We really designed the Model S to be a very sophisticated computer on wheels. Tesla is as much a software company as it is a hardware company." His view on the car is being adopted by automakers worldwide. Without rapid outward communication, data collection, and analysis of information, driver assisted and self-driving cars would not be possible.

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IMAPS 2017

October 9-12, 2017
Raleigh Convention Center, Raleigh, NC

The 50th International Symposium on Microelectronics will feature 5 technical tracks that span the three days of sessions on:

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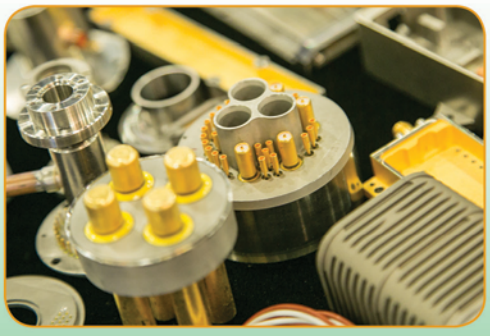

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WLFO Packaging Technology-based WLSiP – Enabler for Packaging of IoT/IoE Modules

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I. Introduction

Promising packaging technologies suitable for upcoming IoT/IoE applications, namely in the segment of wearable electronics, are the various substrate-less Fan-Out Wafer- and Panel-Level Packaging technologies developed during the last decade. Great potential with 50-80% CAGR in the coming years is forecasted in [1] and different other market research reports issued in the following years. This growth can also be explained by the wide design flexibility and system integration capability of the Fan-Out Wafer- and Panel-Level Packaging technologies, providing a small and thin package performing as active interposer. A deeper look into the various potential semiconductor applications for IoT/IoE devices and packaging requirements for those are discussed in [2] and [3].

For modules with needs to integrate mobile communication with other functional elements, and to achieve dense system integration while a high level of miniaturization is required, the FOWLP technology WLFO based on Infineon's/ Intel's proprietary eWLB (embedded Wafer-Level Ball Grid Array) technology shows the highest capability to fulfill those. WLFO is a proven packaging technology platform in high volume manufacturing. It is currently based on 300mm round panel/wafer format and comprises reconstitution, where known good dies from same or different grinded and diced incoming wafers are placed face-down on tape on a temporary mold carrier, wafer molding to create a new reconstituted round panel/ wafer, redistribution of the pads by vias and traces applying thin-film technology, and finally the solder ball attach, marking and package singulation. Component tests can be performed efficiently in round panel/wafer format using a wafer prober, as the package singulation process after the component test does not represent any risk for component functionality. The desired technology features and technology bricks for miniaturized system integration are either available in the WLFO tool box already today or in development.

Already developed WLFO-based 2D constructions like WLSiP (Wafer-Level System-in-Package) with embedded active multi-die, discrete passives, already packaged components, sensors and also optical elements, and WLFO-based 3D constructions like WLPoP (Wafer-Level Package-on-Package) can achieve the highest integration density. The first products are qualified and ready for volume production.

Thin reconstituted wafer handling, Thru Package Vias (TPV) and backside thin-film RDL processing solutions as enablers for thin WLFO-based WLSiP and for thin WLFO acting as a bottom package of WLFO-based WL3D/ WLPoP are essential building blocks for the required miniaturization of IoT/IoE modules. Its development is in the hot phase.

The WLFO has very short connections between die pads and package I/Os. This results in extremely low package parasitic values, especially in terms of inductance, and a good matching network, allowing for high frequency applications with superior electrical performance and low loss.

Thermal performance is getting more and more important as there will be more power consuming and heat dissipating functionality integrated on less and less space. Package designers and technologists have to invent effective methods to get the heat out of the system, avoid hot spots and dissipate heat in the system to places where it does not harm or can be dissipated into the environment. Chip-Package-Board co-design is essential to solve this system task.

II. System Integration in WLFO-based WLSiP

A. Toolbox and technology bricks

The WLFO technology is still a young technology with high potential for further developments widening its application fields. The tool box is continuously increasing. New technology bricks are developed and qualified. The majority of the work is currently done to enable system integration features allowing for high density integration:

- finer line/ space width;
- multi-layer RDL routing (Fig. 1);
- multi-die and discrete passives placement with smaller distances in between (Fig. 2 and Fig. 3).

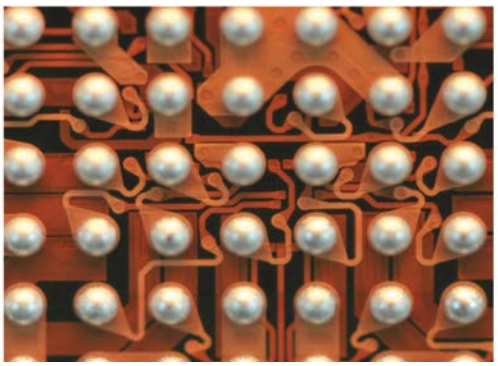

Figure 1 - Example of a multi-layer RDL of WLFO package.

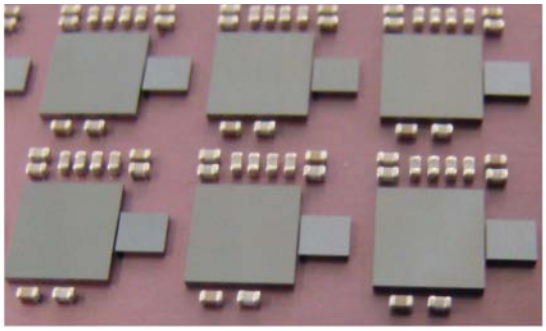

Figure 2 - WLSiP configuration with 2 active dies and 10 discrete passives placed active side face-down on recon wafer carrier before wafer molding.

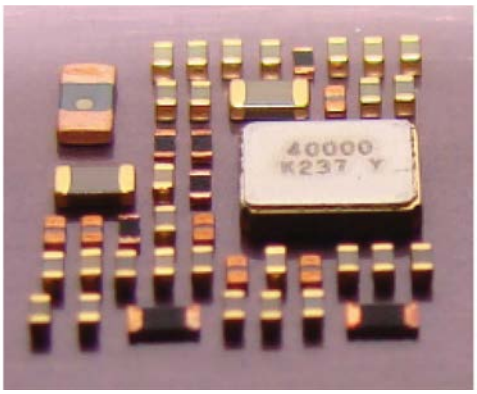

Figure 3 - WLSiP configuration with 40+ elements placed on recon wafer carrier before wafer molding (8.1x8.1mm² package replacing current 5x larger PCB-based solution).

Those design features and further development of the technology to reach smaller line/space width towards 2um/2um, multi-layer RDL with up to 4 metal layers, smaller distance between active dies towards 50um, between discrete passive towards 100um and others will allow for efficient system integration for SiP modules on a very small space. Fig. 4 shows an example of such SiP module representing a quite complete configuration for:

- securing sensing by integrated sensor
- raw data storage
- analyzing and making it meaningful data
- securing data to be transmitted
- sending data
- receiving data
- acting with actuator

Talking about sensor and MEMS integration in WLFO-based WLSiP with its overmold and thin-film process steps, it becomes obvious that sensitive areas need to be protected during processing and released safely and clean after processing. The development of the technology brick "Keep-Out Zones" (KOZ) becomes an essential element in the toolbox. This has been investigated by a wider consortium of industry partners, institutes and academia in a European Joint Undertaking (ENIAC) project named "Processes for MEMS by Inkjet Enhanced Technologies" (Prominent), which was recently successfully concluded. Fig. 5 shows an example of a pressure sensor with sensitive membrane integrated together with an ASIC die in WLFO-based WLSiP.

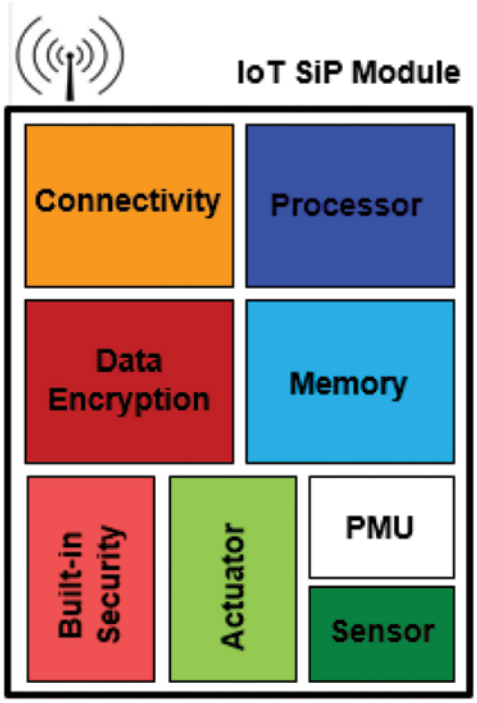

Figure 4 - Example of an IoT/IoE System-in-Package module with a wide range of functionality integrated.

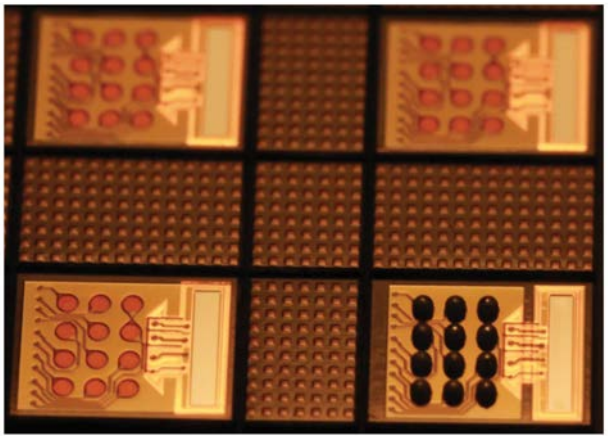

Figure 5 - Pressure sensor with sensitive membrane integrated together with an ASIC die in WLFO-based WLSiP.

B. System-in-Package reliability

The reliability of complex heterogeneously integrated WLFO-based WLSiP systems has been proven in stress tests and readouts done with Daisy Chain dies and with functional components focusing on board level behavior for mobile devices (e.g., Temperature Cycling on Board (TCoB) following IPC9701 specification condition TC2 temperature profile -25degC/ +100degC, 1 cy/h) showed first fail after 900 cycles.

Drop Test (DT) of this complex WLFO-based WLSiP following JESD22-B111 specification showed first fail at 30 drops. The Weibull distribution is shown in Fig. 6. The fails occurred mainly at outer BGA ball rows. Improvement has been achieved through the introduction of a DT optimized solder ball alloy.

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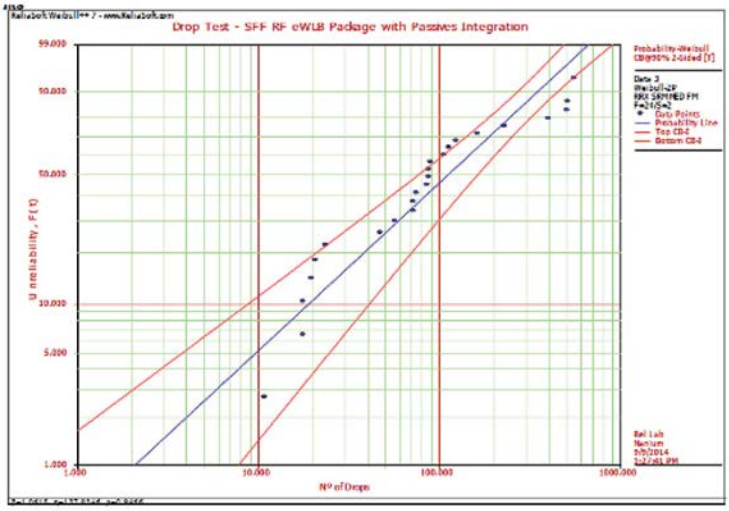

Figure 6 - First DT results of a WLSiP for wearables.

Package size and stand-off, solderballs alloy and internal stress causing dynamic warpage behavior of the package are impacting especially Board Level Reliability (BLR). Besides that, the complexity of the component (e.g., WL-PoP with 2 or 3 levels, interconnects between the levels, embedded element versus moldcompound ratio per level) has significant impact on the reliability achievable. Further investigations are ongoing to better classify this capability for different constructions.

III. Thin Package and WL3D / WLPoP

Challenges moving towards 3D includes the development of vertical interconnections (Thru Package Vias, TPV) from the re-distribution layer (RDL) on the package frontside (BGA side) to the package backside, and the development of solder land pads or even a full RDL on the package backside to allow component assembly on the backside of the bottom package, forming the WLPoP. Fig. 7 shows the relevant section of the NANIUM package offer.

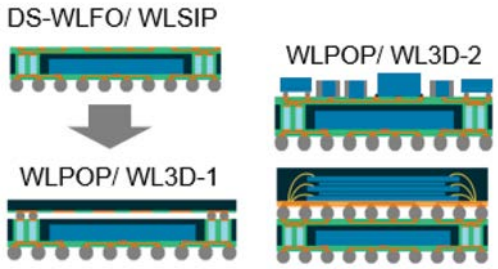

Figure 7 - NANIUM package offer for WLFO-based Fan-Out WLP solutions WLSiP and WLPoP with double sided (DS) redistribution layer or land pads connected by TPV.

Vertical interconnections developed or being developed for FOWLP are either "post-formed" Thru Mold Vias (TMVs) or different kinds of "pre-formed" vias. TMVs require capability for fast and accurate via drilling in the moldcompound by laser ablation. Implementation of connections in vias drilled in moldcompound is the major challenge and a significant cost factor. Although the via side walls can be done with inclination favoring the deposition of material layers, the filling of vias with rough sidewalls resulting from mold filler is still critical. Traditional adhesion/seed layer deposition techniques such as PVD or CVD and electroplating to fill the vias have difficulties achieving the required layer thickness and homogeneity, depending on diameter and depth of the vias. To overcome this, electro-less plating seems to be a good alternative. However, the number of process steps is high and impact on unit cost significant.

The alternative to post-formed vias are pre-formed vias. Its application requires the selection of the right material and suitable format for accurate placement on the mold carrier during the reconstitution process and sufficient position stability during the mold process. The modulus of the material is critical for the pick and place of via elements. Other material characteristics, namely the CTE and Tg of the pre-formed via element, have to be matched to the surrounding moldcompound. Finally, all materials and interfaces between materials in the package impact package reliability and, therefore, need to be understood and controlled.

NANIUM is focusing on the development of pre-formed vias in the format of PCB-bars (small pieces of organic laminated substrate/printed circuit board with a matrix of vias processed at substrate/printed circuit board supplier) placed in the reconstituted round panel/wafer before molding in order to make the vertical connection between front- and backside RDL layers or just backside the contact pads of the package. The developed pre-formed vias are visible in Fig. 8, and a WLPoP applying this TPV technology with three functional levels including a Flip-Chip placed underneath the package between the BGAs and connected to the frontside RDL of the package is shown in Fig. 9.

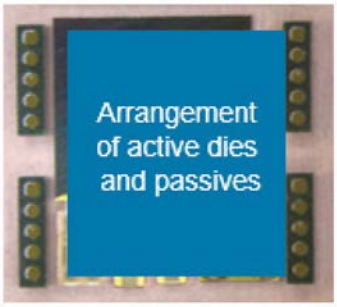

Figure 8 - WLSiP configuration with Thru Package Via bars for thin WLPoP bottom package placed on recon wafer carrier before wafer molding.

Figure 9 - Final WL3D / WLPoP-1 configuration with three levels of functionality (2x WLFO based WLSiP stacked, and 1x Flip-Chip assembled in ball grid array).

If the total package height of a WL3D/ WLPoP has to be very thin, such as below 1mm or even below 0.8mm for the mobile market, the thickness of the individual levels of the WLPoP have to be in the range of 200-300um only. Especially the WLFO bottom package with the Thru Package Vias (TPV) contacts has to be thin, and that is the one which needs to be processed at both sides. After processing the frontside of the recon wafer it has to be thinned to achieve the final thickness and reveal the TPV before processing the backside in the thin-film process line. As thin 300mm recon wafers are not stable enough to be handled as such, temporary bonding of recon wafers was developed successfully, supported by the project Enhanced Power Pilot Line (EPPL), partially funded by EU and national grants under the ENIAC program [4].

Temporary bonding of Si wafers, thinning and processing the Si wafer while sitting on the temporary carrier, and finally de-bonding the wafer as shown in Fig. 10 is an established process in the industry.

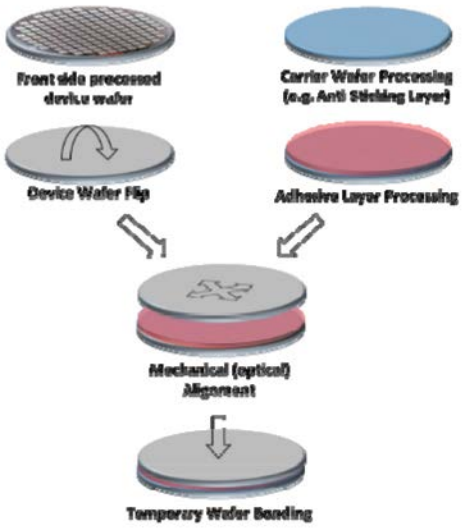

Figure 10 - Generic Temporary Bonding Process Flow for multilayer adhesives (Source: EV Group, 2012).

But WLFO recon wafers are plastic wafers with embedded elements in different configurations for each product. Consequently, the recon wafer behaves very differently than the Si wafer. In a set of experiments, different major parameters were tested, like carrier materials and thicknesses, adhesive materials and temporary bonding process conditions. The results showed the significant impact coming from both adhesives and carrier properties on the bond quality and on the ability to withstand the very aggressive thin-film processing for FOWLP. Based on the different results obtained during the multiple experiments, typical carrier materials were shown to be inadequate and new carrier materials, together with the most suitable temporary bonding adhesive and process conditions, demonstrated the existence of an optimal solution. After a careful selection, the best combination of such parameters enabled a robust temporary bonding solution for FOWLP. The data are proprietary and cannot be disclosed. However, no visual or internal abnormality was seen on the optimized configuration as well as only minimum wafer warpage was measured during FOWLP critical process steps [4].

IV. Electromagnetic and Thermal Performance

A driving force and significant advantage of FOWLP and WLFO in particular is the superior electromagnetic and thermal performance of the package compared to similar package types allowing similar levels of dense system integration.

A. Electromagnetic performance

Due to the very low package parasitics compared to laminate substrate or lead-frame-based packages, WLFO offers excellent RF performance. This is the result of the very short signal path length between chip, package, and board, as made visible in Fig. 11. Applicability of the WLFO package is proven in high volume for high frequency applications. It became a standard package for RF/ Baseband SoC in the mobile communication market [1] and is taking over market share for automotive and non-automotive radar applications such as the 77GHz module from Infineon Technologies AG [5]. Higher frequencies up to 80GHz for millimeter wave radar applications have been demonstrated, and feasibility of the packaging solution up to 120GHz are under investigation.

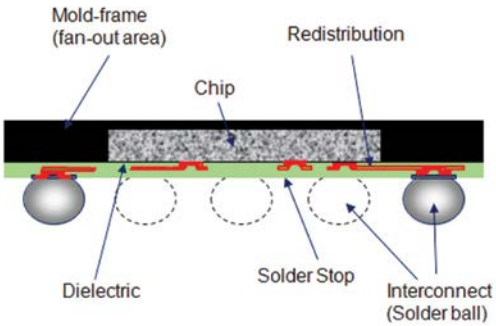

Figure 11 - Basic eWLB construction with single die (Source Infineon Technologies AG, 2009).

B. Thermal performance

System integration + Miniaturization = More functionality on less space. That means at the same time higher levels of power consumption and heat dissipation per area. The use of thermo-solderballs underneath the silicon die reinforcing the main heat path via the solderballs into the system board, as described in [5], allows for improved thermal behavior. On the package backside, exposed die backside and application of heat spreader on component or system level are effective measures for passive cooling. WLFO thermal behavior improvement by change to packaging materials with higher thermal conductivity and effective heat spreader application on the package backside, either direct over exposed die, or electrical isolated over an over-molded package backside of WLSiP with different embedded elements has been investigated in European FP7-Project "Nanotherm" [6]. The concept followed in the program comprises three major steps from characterization of the current status via test vehicles addressing single design features to the final demonstrator delivered and tested at the end of the project. Fig. 12 shows the investigated evolution of heat dissipation solution in systems with increasing complexity.

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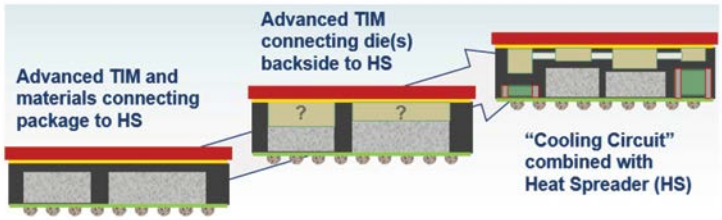

Figure 12 - Advanced thermal performance improvement solutions for WLFO-based WLSiP of increasing complexity.

New moldcompound with Al2O3 filler and 3.1 W/m*K compared to current standard moldcompound with SiO2 filler and 1.0 W/m*K has been successfully investigated. Package Rth was reduced from > 2K/W to < 1K/W. Ti-Cu sputter applied to over-molded package backside ensured good organic-metal adhesion. Together with the new more thermally conductive moldcompound a reduced rT across the surface of the FOWLP with Thermal Interface Material (TIM) and attached Heat Spreader (HS), which reflects the effectiveness of the heat transfer to a secondary system, was greatly reduced from that on standard FOWLP, from 19% temperature non-uniformity down to 3.6%.

V. Conclusion

Fan-Out Wafer-Level Packaging shows great potential to offer a wide range of package constructions best suitable as packaging solutions for IoT/IoE applications. The design flexibility allows for customization to the specific needs of the customer. High integration density ensures a high level of system integration, ensuring excellent electrical and thermal performance at a reasonable cost as manufactured on large format in batch processing.

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Exhibit at IMAPS 2017

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Lessons Learned in the Implementation of Aerosol Jet Printing for Fabricating Multilayer Circuit Boards

Peter Lewis, Robert White, and Brian Smith – Draper

Additive manufacturing applied to electronics is rapidly growing in volume and revenue worldwide with projections of significant technological impact and market influence in the coming decades[1-5]. Impact areas range from healthcare to energy management to electronic wireless systems[2]. Given that electronics are fundamentally multi-material systems, the challenge lies not just in material formulation but also material-material interaction including chemical compatibility, adhesion, temperature processing, and induced stresses. While initial deposition and functionality of the devices receive the most attention, long term aging and environmental performance are relatively unexplored topics in printed electronics, yet critical for adoption of the technology into field-able systems.

In particular, Internet of Things (IoT) applications require small, conformal modules integrating standard commercial off the shelf (COTS) components with a fast time-to-market and simple circuit customization/revision. This is congruent with additive manufacturing and, in particular, aerosol jet printing (AJP) technology, where the entire system can be deposited on a 3-D, potentially flexible, substrate, and not confined to two-dimensional planes. Other approaches often employ hybrid techniques such as stereolithography (SLA), fused deposition modeling (FDM) and inkjet in conjunction with conductor embedding and pick-and-place tools[5-7]. These methods generally employ multiple tools for different materials at different stages of the manufacturing process.

AJP can deposit both conductors and insulators while maintaining a millimeter-scale standoff distance above the printed surface. This enables conformal printing to 3-D substrates and expands circuit integration to geometries not suited for planar circuits. In addition, this approach shortens the circuit layout and fabrication cycle time to more quickly iterate a given design[1] and reduce material waste[8], particularly hazardous waste, compared to a conventional printed circuit board.

One IoT-relevant example is a Bluetooth transceiver system that integrates a low cost system on chip (SoC) with functional sensing, actuation of LEDs, and RF transmission. This builds on AJP work shown with COTS integration previously[9-11] and emphasizes the multilayer, RF challenges of these systems.

The Nordic Semiconductor nRF51822 Multiprotocol Bluetooth low energy/2.4 GHz RF SoC is an ideal candidate for the IoT demonstration. A transceiver circuit reference design is available, leveraging the COTS demonstration board nRF51 Development Kit (PCA10028), to compare "standard" PCB embodiment with the printed approach, particularly related to line resistivity, power

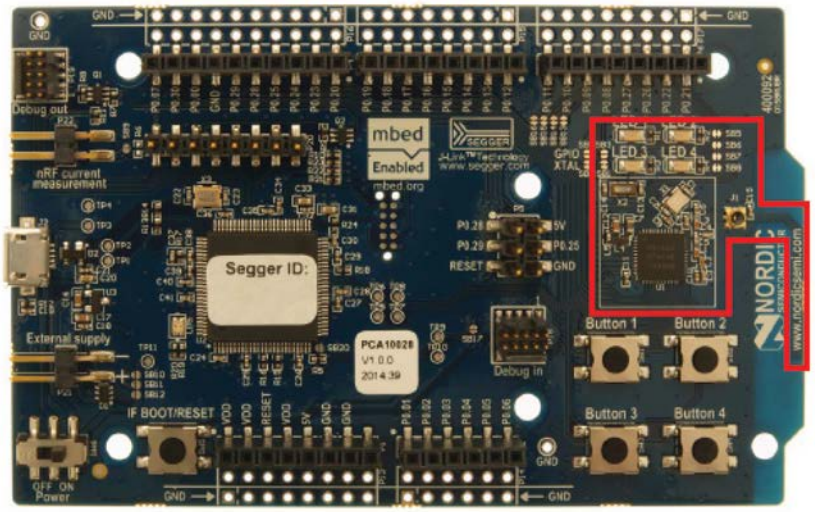

Figure 1: The Nordic Semiconductor nRF51822 Multiprotocol Bluetooth low energy/2.4 GHz RF SoC is shown. The region in red is being relicated with AJP technology.

consumption, and RF performance. The PCA10028 is reprogrammable, has both active and passive components, has an appropriately sized footprint for printing, and uses a variety of easily obtained commercial components so the application scope remains broad, particularly for IoT. Figure 1 shows the full commercial board along with the red region which is being replicated in the AJP circuit. Unnecessary peripherals are stripped out of the design so that the focus is only on interconnection to the chip, power and wireless communication.

Design changes to the original layout make the board more printable. These include reducing the ground plane area, placing the processor in QFN48 package upside down on the board, printing up the sidewall of the processor, and printing over the ground plane on the backside of the chip. This "chips first" approach builds up the electrical interconnect around the SoC. This relaxes the alignment restrictions on part placement and circumvents standard attach methods which can dissolve the AJP ink. Finally, the additive approach to dielectric deposition changes the layout rules versus standard subtractive PCB layouts that remove dielectric to create vias.

NovaCentrix HPS-030AE1 Silver Flake Ink and Corin XLS polyimide ink served as the AJP conductor and dielectric, respectively. The SoC was affixed to the substrate with Armstrong C-7/W epoxy (C-7) and other components conductively attached with Epotek H20E for prototyping and proof of concept. They could also be integrated first along with the SoC.

Fabrication starts with placing the microprocessor (QFN48 package) upside down and attaching to the substrate with C-7. Enough C-7 is used during this attach to make an epoxy fillet along the edge of the microprocessor package. This eliminates the airgap between the package and the substrate which can prove difficult to bridge with conductive inks.

Conductive traces integrating the package to the circuit are then printed with silver ink up the package sidewall. Five passes are used in order to thicken the trace and reduce the resistance. This approximately correlates to a thickness of 3-4 µm. Figure 2 highlights the flipped QFN package and the sidewall interconnect.

The ground plane is printed immediately after the sidewall integration traces on the QFN48 package. This is done without sintering of the sidewall traces to reduce heat exposure to the QFN48 package. Two passes are done in order to build up the thickness of the ground plane and reduce resistance. This correlates to a thickness of around 2 µm.

After the sintering of the ground and interconnect layers, which is done at 250°C for one hour, the dielectric layer is printed in patches. Dielectric is only dispensed in areas of need. For most areas, as long as the dielectric provides electrical insulation, the thickness doesn't matter. Generally the dielectric is built up with three passes of polyimide. However, the thickness is of critical importance for the RF circuitry, as discussed later. The polyimide is cured at 200°C for one hour.

The upper conducting layer is printed last. This layer includes pads for components down to a 0201 footprint (imperial units) in the RF portion of the circuit. Figure 3 shows two different locations on the board with a multilayer scheme. After this layer is sintered at 200°C for 1 hour, the board is populated with the rest of the parts and attached with conductive epoxy. Figure 4 shows the

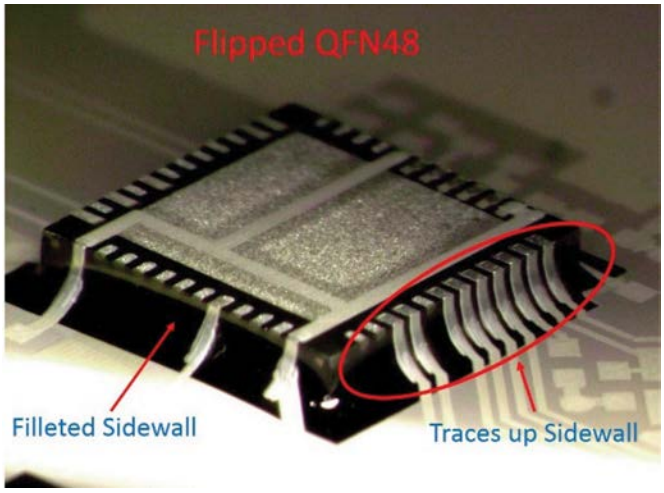

Figure 2: The flipped microprocessor (QFN48 package) with printed interconnect is shown. The glue fillet provides a ramp for the printed ink to traverse the sidewall of the package and make the pad to routing connections. On top of the package there are routing traces connecting pads together. They are shielded from the package ground plane by polyimide.

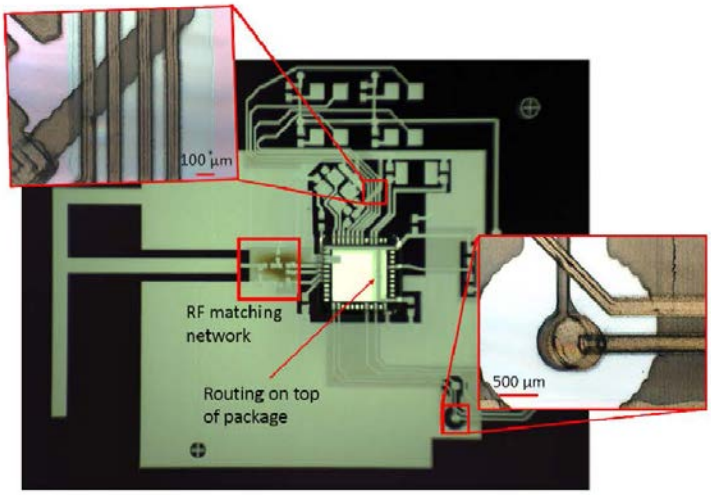

Figure 3: The transceiver circuit after printing of the routing layer is shown. Two locations are called out which show a multilayer stack up of conductor-dielectric-conductor. The targeted deposition of the dielectric is fundamentally different than traditionally PCB manufacture which removes dielectric from select areas.

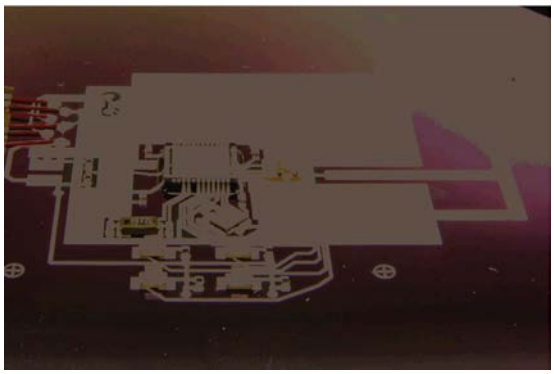

Figure 4: The final board after it was populated with COTS components is shown.

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completed transceiver circuit. Printed lines were designed to 25 micron width and 2-5 micron height. While material output variation, ink properties, and the aerosol jet stream can cause more geometric variation compared to PCB technology, misprints can be corrected with a simple isopropyl alcohol wash and reprint prior to ink cure.

This IoT platform provides a quantitative measure of fabrication time reduction and rapid design iteration. After the preliminary design, significant and sequential changes, particularly the dielectric patterning, each took no more than an hour, including machine code generation. The fabrication time was reduced to 10 hours and there is potential to reduce it by approximately 4 more hours by changing the sintering/annealing process and employing an automated tool for population of the circuit board components. Other approaches to sintering such as photonic annealing could reduce cure time from hours to seconds per layer.

The SoC is programmable via attached SPI port wires, resulting in successful boot of the system which executed a program that blinks three LEDs in a pattern. The traces have a resistivity 3-7x higher than that of PCB copper and result in nearly the same increase in total power consumed since trace loss dominates total power for this low-power design. The acceptability of this resistivity difference is largely application dependent. Silver traces reaching nearly 50% of the conductivity of bulk silver have been reported elsewhere, so further process improvement may be possible as well.

The RF portion of the circuit is most challenging due to the inconsistency of the microstrip antenna dielectric. Design and modeling calls for a 10 micron thick dielectric; a +/- 3 micron difference would lead to RF failure. Process variations and conditions in dielectric deposition did not yield this tolerance, therefore the Bluetooth communication portion of the system is nonfunctional. This highlights a critical future direction for development of AJP system electronics – new dielectric inks and processes to achieve uniform dielectric layers for multilayer RF antennas.

Overall yield of the limited number of circuits printed and assembled was less than 30%. The primary failure mechanisms are electrical shorting from layer-to-layer misalignment and conductive epoxy bridging electrical layers due to chemical incompatibility. The first can be solved with improved fiducial locations and alignment procedures. The second can be resolved by material change or component attach with AJP to preclude the need for epoxy.

Finally, environmental and aging testing employed typical test structures to assess the long term viability of the ink/dielectric system. First, a thermal shock test was conducted according to IPC-TM-650-2.6.7.2a Thermal Shock. The test units were exposed to temperatures of -55˚C to 125˚C in 15 minute cycles for 1000 cycles. Then, a moisture and insulation resistance test was conducted at 50°C/85% relative humidity regime according to IPC-TM-650-2.6.3F. This test was conducted for 5 days. Last, some structures were put into an oven at 60°C for months to determine the effect of lab humidity and elevated temperature on the structures. This was not done to an IPC standard. All test structures were subject to intermittent testing during their environmental exposure. This testing did not include electromigration analysis.

Each test article consisted of two silver barbell structures offset by 90° as shown in the corner of the top right plot in Figure 5. The two barbells are insulated from each other by a layer of polyimide at their intersection. This provided a portion of silver above and below the polyimide during the tests, simulating a multilayer circuit. The number of test articles per environment ranged from 112-192. Figure 5 shows the results of the three environmental tests. The resistance change over the duration of the test along with the number of failed modules is tracked. The error bars represent one standard deviation from the mean. As can be seen there is no noticeable change in resistance during the thermal shock testing, however there is over 42% module failure. This appears to be a result of adhesion degradation over the testing.

The moisture resistance test shows a significant change in standard deviation of the measurements but a less significant change in the mean resistance change. Module failure at the end of the test only reaches 7%. Similar to the thermal shock results, module failure appears to be primarily due to adhesion degradation between the conductor and the SiO2 substrate, a common failure mechanism for printed electronics.

Elevated temperature testing shows a significant mean resistance change but not an increase in measurement standard deviation nor any module failure. These test modules were sintered at 150°C for 1 hour, compared to 250°C for the IPC test articles. It can be inferred the mean resistance change is a direct consequence of sintering in the elevated temperature environment. Interestingly, when the structures are kept at a consistent temperature under lab humidity, the mean resistance variability is very low.

In conclusion, the AJP technology results in electronic systems fabrication with much greater versatility. Electrical resistance is 3-7X higher than bulk, which is acceptable for low frequency applications, but will result in an increase in parasitic power loss, which should be compensated for with trace design. For RF applications, the greatest challenge is improved control of dielectric thickness. Other challenges include electrical shorts resulting from layer-to-layer misalignment or conductive epoxy component attach. The work can be extended to a variety of substrates, inks and sintering methods.

The primary advantage of this method is concept-to-prototype fabrication time reduction from many weeks/months to days. Accelerated ageing shows generally good long term resistance performance, substrate adhesion as the primary failure mechanism, and that the inks could be useful in electronics applications for temperate environments. A SoC demonstration has been partially successful particularly for low frequency and digital domains, revealing challenges in adopting the technology for RF and IoT applications. Overall, AJP is a promising technology for rapid-prototyping of system interconnect.

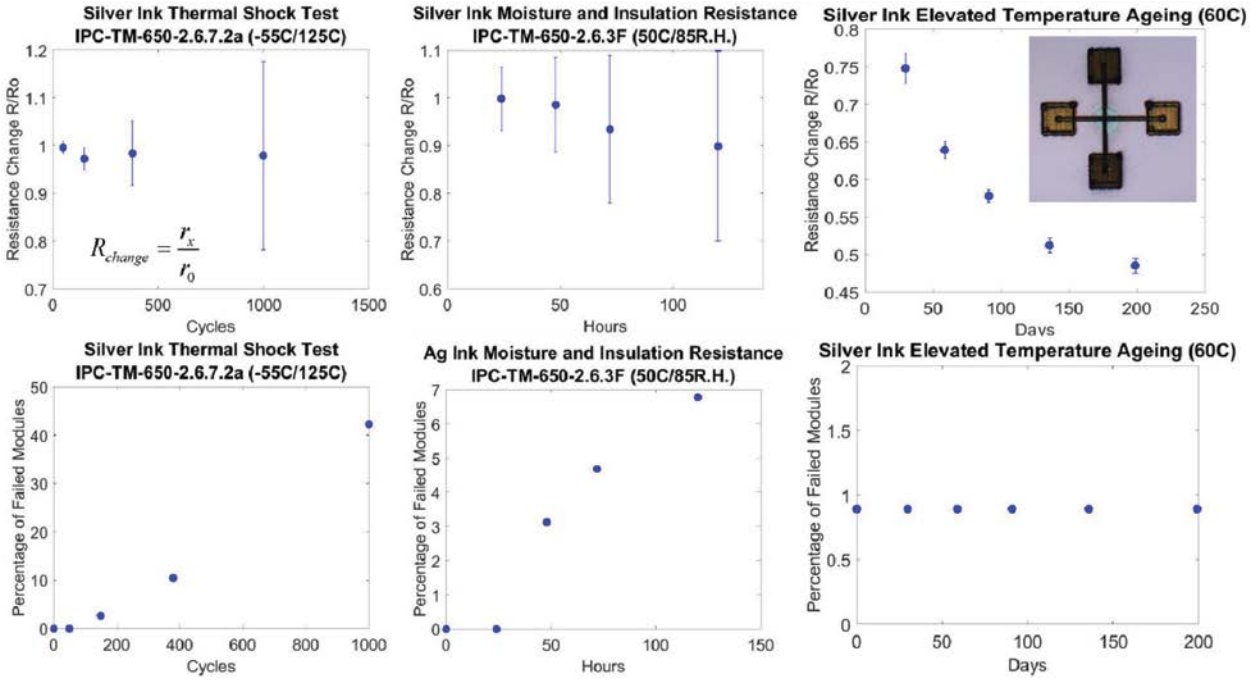

Figure 5: The accelerated ageing test results are shown above. Two tests were done to IPC standards while the third was done at elevated temperature in lab conditions. Each test included over a hundred structures with intermittent testing over the test. The testing occurred outside the environment. One structure is shown in the top right of the figure. The thermal shock results have a high module failure rate by the end of the testing, however the mean resistance change is fairly consistent. The moisture resistance test showed a much lower module failure rate and also a small change in mean resistance. The elevated temperature ageing shows virtually no module failure but a significant change in mean resistance. These modules were sintered at a lower temperature than the IPC test modules. A long term sintering of these modules is likely being observed.

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The Advancement of Device Packaging – A Resume on IMAPS DPC 2017

By Peter Ramm, Gilles Poupon, Pascal Courderc, Markus Lietgeb, and Maaike M. Visser Taklo

As part of the organizing committee, we believe this year's IMAPS Device Packaging Conference really fulfilled what the announcement promised – the largest conference dedicated to the full spectrum of 3DIC and packaging, fan-out technologies and MEMS/sensors. We enjoyed 12% attendee growth over 2016, welcoming nearly 600 attendees from 20 countries, in addition to a 12th consecutive sold-out exhibition hall! In this short resume we would like to highlight just a few of the outstanding talks at the DPC presented by Ron Huemoeller, Amkor Technology; Lionel Rudant, CEA-LETI; Pascal Couderc, 3D-PLUS; Sitaram Arkalgud, XPERI (formerly Invensas); Markus Leitgeb, AT&S; and Maaike M. Visser Taklo, SINTEF.

Ron Huemoeller, Amkor, delivers the opening keynote.

During the DPC opening session, the first speaker, Ron Huemoeller, corporate VP, worldwide R&D, Amkor Technology, Inc, presented "Heterogeneous Integration: Packaging the Future." Ron explained how in the past few years, advanced packaging technologies have increased in complexity, transitioning from single to multi-die packaging, enabled by 3D integration, system-in-package (SiP), wafer-level packaging (WLP) and creative approaches for embedding dies. State-of-the-art heterogeneous integrated semiconductor packaging provides reduced form-factor, increased data transfer rate, improved signal integrity and memory bandwidth, all with reduced power and improved thermal performance.

Lionel Rudant, CEA-Leti, delivered the second keynote.

Next, Lionel Rudant, CEA-LETI, introduced 5G networks and their impact on packaging roadmaps. 5G networks are expected to enable widespread internet of things (IoT) adoption by offering improvements like increased bandwidth and reduced latency. Microelectronics is now led by application-driven roadmaps, and new drivers for 5G systems are diverging IoT services that require flexibility and scalability from technology. Exploitation of innovative in-package integration of antennas was highlighted, together with the more widespread use of beamforming and multiple antennas. Rudant explained that there is a new complexity driving the technology roadmap since the transistor takes part of advanced system architectures where the software part is increasing.

The first keynote speaker on Thursday was Sitaram Arkalgud from XPERI, who presented "Trends in MEMS and Sensor Integration." Sitaram is XPERI's VP of 3D Applications. The combination of the keynote talk title and his job title shows clearly in which direction a great market track will be developing; a remarkable number of future MEMS and sensors products have a need for 3D integration technologies! He focused on IoT as the third wave of MEMS proliferation, after automotive and mobile phones. "Smart objects" are a subset of IoT that show local intelligence and awareness.

We are in the phase of rapidly growing markets and increasing competition and we must reach for cost reduction, standardization, and increasing functionality and performance. A corresponding key is the simplification of processes and Sitaram's talk focused correspondingly on wafer bonding processes. He discussed all relevant bonding schemes, including variants of glass-based and metal bonding – as thermocompression bonding (TCB) and solid-liquid interdiffusion (SLID), and compared production parameters with XPERI's technologies called ZiBond and direct bond interconnect (DBI). Sitaram's clear conclusion was that ZiBond and DBI, both low-temperature bonding technologies licensed to Fraunhofer Munich, offer sufficiently high bond strength for MEMS processing and 3D integration of MEMS/IC products. The technologies are highly competitive as they result in process simplification, a particularly high throughput for a low-cost of ownership, and the interconnects are highly scalable. The scalability is critical for answering to the future needs of increased functionalities and performance of the bonded systems.

Thursday's second keynote paper was presented by Markus Leitgeb from AT&S, who focused on embedding active and passive components into a large panel using PCB technologies. The PCB industry is well aware of the ongoing change in the electronic world and is developing innovative ways for supporting this trend of miniaturization and modularization of electronic devices, ending in an all-in-one-package.

Component embedding may not seem to be the latest break-through in PCB world; companies have worked on embedding in various shapes for more than 30 years (e.g. ECP® from AT&S). Besides the performance and form factor improvement (which are also offered by WLP technologies), embedding in laminate offers the economy of scale enabled by large panel format adopted in PCB production (18"x24" panel compared to 12" wafers).

Additionally, the PCB technology allows thick copper traces (up to 200µm) in the package, which is needed for current transport and advanced cooling of high power

devices. For the two main product lines, SiP and system-in-board (SiB), Markus explained that only embedding in PCB can be used for both types due to large form factors needed in the SiB.

At the end of his presentation, Markus pointed out that PCB companies will have to transform from an interconnection provider to a full turnkey solution provider. Therefore, AT&S has started several activities in recent years to offer a high-volume manufacturing capability and a product realization or even take over part of the supply chain.

In the fan-out session, Pascal Couderc, 3D PLUS, described the company's proprietary 3D technology named wire-free die-on-die (WDoD™), which is based on the stacking of known good rebuilt wafers using a fan-out wafer level package (FOWLP) process with only known good dies and PCBs with components. Interconnections are formed using a bus metal patterned with a laser. In this talk, two types of 3D modules developed in the frame of a study of implantable medical products (leadless pacemaker and neurostimulation) were described.

These electronic 3D modules had several layers, including PCB layers, comprising components that cannot be processed with fan-out technology. Only layers with bare dies were processed using eWLB-based FOWLP technology. For one module, their so-called Flow 3.5 technology was used as an alternative technology to FOWLP. External sides of these modules could be populated with additional components interconnected with other sub-modules. They can also be solder balled in order to be reflowed as BGA components.

WDoD™ allowed a smaller form factor than other competitive 3D technologies like chip-on-chip and flex-folded PCB.

One of the last presentations in the track for Engineered Micro Systems/Devices was given by Maaike M. Visser Taklo from SINTEF on the topic of reliability of conductive adhesives. The results are part of a larger European project called Lab4MEMS II led by STMicroelectronics. The focus of the project is to reduce cost and improve manufacturability of assembly of optical MEMS, like mirrors and scanners. In that respect, SINTEF has studied the possibility of performing reliable flip-chip assembly of mirrors directly onto rigid-flex boards using conductive adhesives. A novel adhesive based on metal-coated polymers spheres, developed by Conpart, was found to have remarkable performance compared to a commercial reference material when exposed to hygrothermal aging. Exposure to humidity will be one of the key challenges of several future IoT devices as they will be placed all around us, also outdoors.

All the presentations and extended abstracts from the conference were published on April 4 and can be downloaded via www.imaps.org/devicepackaging/down/2017DPC_SECURED.zip

We invite you to enjoy reading the great papers of the three tracks of the conference:

- Interposers, 3DIC and Packaging
- Fan-Out, Wafer Level Packaging and Flip Chip
- Engineered Micro Systems/Devices

Upcoming IMAPS events

Mark your calendars for the 14th International Conference and Exhibition on Device Packaging from March 5-8, 2018. Be sure to view details about all upcoming events at www.IMAPS.org, including the 50th International Symposium on Microelectronics in Raleigh, NC from October 9-12.

Editor's Note: This article first appeared on April 17, on 3D InCites. Please visit 3D InCites for more coverage of IMAPS DPC. (www.3DInCites.com)

It's a Jungle Out There: Supply Chain in Transition!

Analysis and More at Device Packaging in Sunny Arizona

By Thomas Goodman, Izinus Technologies, tgoodman@izinus.com

Where is our industry headed? With increasing consolidation, burgeoning activity in Asia, and shifting market drivers, it's a veritable jungle out there. Attendees at the IMAPS Global Business Council's Third Annual half-day plenary session got a fresh look at the status and outlook for our industry. The session was held as an integral part of the Device Packaging Conference in Fountain Hills, Arizona on March 8, 2017. The timely and important topic this year: Microelectronics Supply Chain in Transition.

Jim Walker from WLP Concepts started the morning session out with his presentation on "Have the Semiconductor Industry Grow Again," noting that long-term semiconductor industry revenue growth rates have fallen from 15 percent to 5 percent in the last thirty years. Semiconductor revenues for 2016 were tepid at about 1.5 percent growth; however, Mr. Walker said that DRAM and NAND, along with application-specific standard products (ASSP), drove a surge late in 2016 that propelled the industry into a strong 2017. With this momentum, he said, the industry is poised for strong growth "on all cylinders," with a 7.2 percent growth forecast in 2017. In addition, Mr. Walker noted that the inventory correction of the past two and a half years is over, and that restocking of both semiconductors and finished goods will continue into 2017, adding to growth.

But he also said profit margins are decreasing and a slower growth market is ahead. Mr. Walker stressed that companies had to pursue alternatives to gain competitive advantage, saying that business as usual is no longer an option. In particular, he noted three directions in which the semiconductor industry needs to move in order to stay competitive: mergers and acquisitions (M&A), diversification into new markets, and adoption of new strategies or business models.

Some of the major M&A activity over the last three years noted by Mr. Walker include Tianshui Huatian's purchase of FlipChip International in 2014; JCET's acquisition of STATSChipPAC in 2015; China WLCSP's acquisition of an Omnivision facility in 2016; and most recently, Amkor's offer to acquire Nanium in 2017.

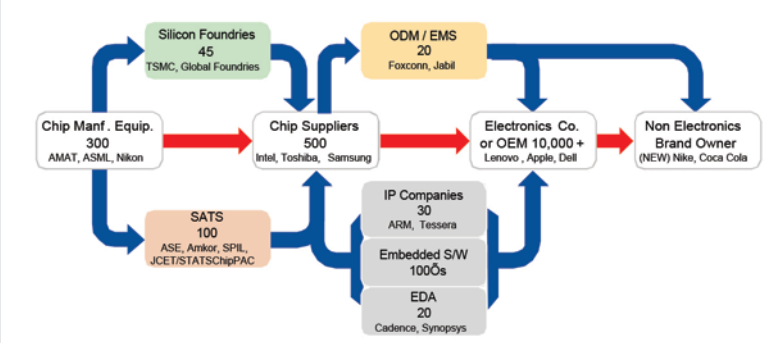

Figure 1: The semiconductor ecosystem.

As Mr. Walker showed in the semiconductor ecosystem in Figure 1, our industry has followed a traditional business model (red arrow) in which chip suppliers sell chips to electronics companies or OEMs. Other models involving silicon foundries and Semiconductor Assembly and Test Services (SATS) have been in play for a number of years.

A recently emerging model is what Mr. Walker calls the OEM Direct Supply Model. In this case, the traditional chip suppliers are bypassed by the OEM which goes directly to a foundry to have its chips made. One example of this is Apple which has its own APU designs fabricated and packaged at TSMC, then sent to Foxconn for assembly into phones and tablets.

He then further elaborated on HonHai/Foxconn, which has become vertically integrated through a series of M&As over the last few years; for example, Foxconn acquired Sharp Corporation (largest display manufacturer) and SMART Technologies (supplier of interactive touch technologies and software) in 2016. Mr. Walker said that Foxconn is attempting to complete its full vertical integration by acquisition of Toshiba: Foxconn issued a statement in March 2017 expressing its intention to bid for the world's largest flash memory maker.

E. Jan Vardaman, President of TechSearch International, followed with a presentation on "Market Drivers and Packaging Trends for Automotive Electronics." Ms. Vardaman began with a discussion on Advanced Driver Assistance Systems (ADAS); development of these systems is being driven by an increasing number of features for safety and autonomous driving, such as blind-spot detection, parking assistance and collision avoidance (Figure 2). She noted that there is a long path to autonomous driving along which we'll see an increasing number of features over time such as self-parking (when you exit the car it parks itself, then returns when you call it). Ms. Vardaman quoted Infineon's assessment that adding partial automation to today's cars would add an additional $100 to $150 to the current $330 of semiconductor content per car; a car with full automation could have up to $550 in added content per vehicle.

Some safety features require complex modules; an air bag module in a Toyota Prius contains accelerometers, CPU with memory, power controllers, impact trigger and serial EEPROM. This small module saved Ms. Vardaman's daughter Natalie in a frontal confrontation with a tree on a rain-slick highway: as seen in Figure 3, the tree won, but Natalie walked away from the crash with only a slight seatbelt burn on her shoulder. Ms. Vardaman said there

are still advances being made in this technology: Freescale reports a 70 percent size reduction in impact detection sensors over the last 13 years.

One key point Ms. Vardaman stressed was that, due to the exceedingly stringent reliability requirements for automotive components, advanced packaging used in mobile communications and computing generally cannot be moved directly into automotive applications; most mobile packaging would not be able to pass automotive-level reliability testing. For example, she said, devices used in an Engine Control Unit (ECU) require Zero Defect quality and greater than 15+ year reliability. Ms. Vardaman noted that though there are many revenue opportunities in automotive electronics, the road to them is not an easy one.

Still, companies are striving to adapt their technologies and packaging to the automotive space. Ms. Vardaman explained that Sony, a leader in CMOS image sensors (CIS) with extensive product experience in the mobile phone space, is one of many CIS companies working hard to capture business for automotive applications such as front collision warning, backup cameras, and driver/passenger monitoring.

Finally, Ms. Vardaman spoke of sensor fusion, the integration of sensing, and big-data processing hardware and software in the automotive environment for airbag deployment, collision avoidance, etc. She noted that these systems need to react fast! Renesas' sensor fusion ECU, for example, combines results from radar and camera sensors with vehicle acceleration, braking, and handling systems to avoid and reduce the possibility of accidents in advance.

Santosh Kumar, Senior Technology and Market Analyst at YOLE Developpement, followed with his presentation of "What's Happening in China's Advanced Semiconductor Packaging Landscape?" Mr. Kumar opened his talk with a snapshot of China's place in the electronics world, saying the market for ICs in China is expected to grow at a 7 percent CAGR, compared with the rest of world's growth at 2.5 percent. China produces over 70 percent of the world's laptop tablets and mobile phones, he said, although it only produced 18 percent of the $149B worth of ICs it consumed in 2016. This gap between the market and production in China makes its IC industry an attractive target for Chinese industry and the government, and the rest of the world.

China is investing across the entire supply chain, Mr. Kumar said, to build a complete IC ecosystem of OEMs, foundries, design/fabless houses, OSATs, EMS and Equipment/Materials makers. This growth effort is being driven by investment by global companies such as SPIL and Amkor, long-term growth in the China IC industry, aggressive M&A, and by Chinese government initiative.

Mr. Kumar described several of the many aggressive plans developed by the Chinese government to grow its IC industry and ecosystem: it adopted a National IC guideline in 2014 that mandates China to develop a world-class IC value chain and rolled out its "Made in China 2025" plan in 2015. China is also preparing an upcoming 13th Five-Year Plan to promote innovation. As he showed in Figure 4, local IC design houses and OSATs are expected to become competitive with global players by 2020.

Mr. Kumar notes that China has been employing M&A as a strategy to acquire technology and grow quickly. Major acquisitions over the last couple of years have pushed several Chinese companies up the recent revenue rankings of major OSATs worldwide: JCET is number four

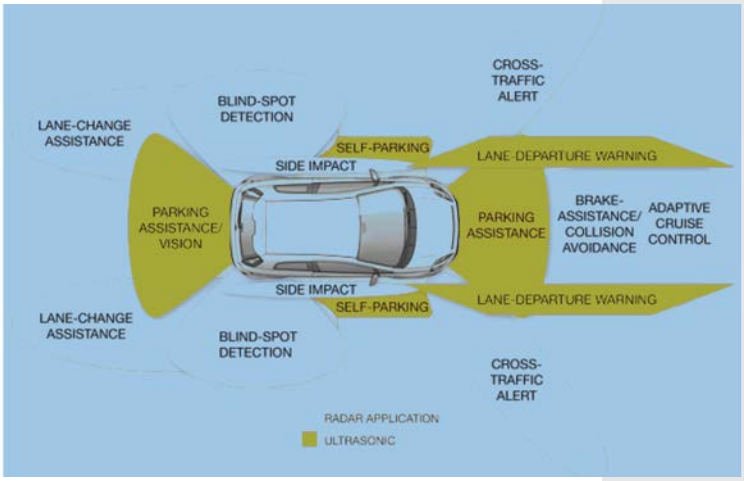

Figure 2: Features of Advanced Driver Assistance Systems (ADAS).

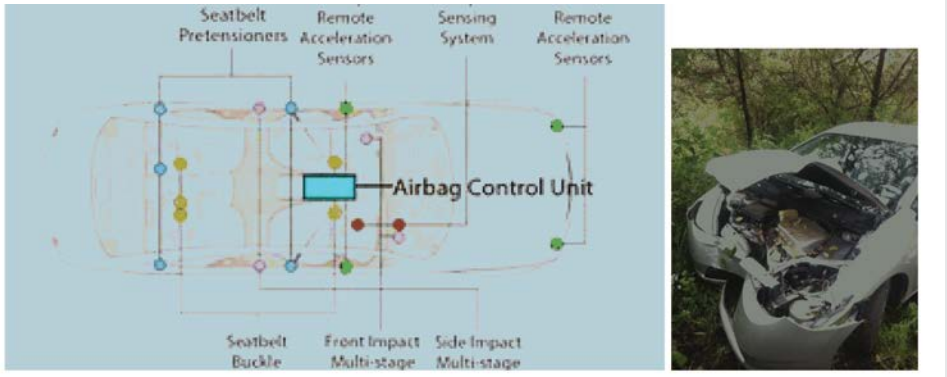

Figure 3: Diagram of (and need for) Safety Sensors including Airbag Control Unit.

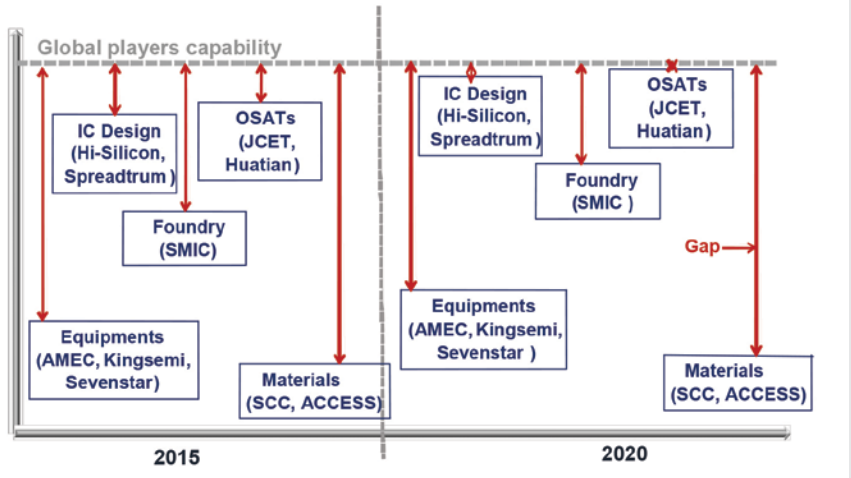

Figure 4: Gap analysis of suppliers in the advanced packaging supply chain.

continued on page 20

continued from page 19

worldwide after its purchase of STATSChipPAC, and Tianshui Huatian rose to number six after its acquisition of FlipChip International. Other important acquisitions in China include Nantong Fujitsu's taking over some AMD assembly and test facilities. However, he said, not all attempts at M&As are successful: Tsinghua Unigroup's bids for PowerTech, ChipMOS, SPIL and Micron all ended in failure.

Mr. Kumar wrapped up his talk by warning that, in considering the aggressive growth and rapid technology expansion in China, the country should take care not to over-produce capacity and break the market as had happened previously in the solar cell industry.

Next up in the GBC lineup was Eric Huenger at Dow Electronics Materials who spoke on "Integrated Packaging and Substrate Technologies for Next-Generation Smart Devices." To start off, Mr. Huenger showed that the projected number of connected devices in the "Internet of Things" in 2020 ranges from 25 billion to 50 billion. These will, according to estimates, connect some four billion out the approximately seven and a half billion people on the planet. Over half of the devices estimated to be produced in 2020 will be in consumer products, he said.

The growing ubiquity and required performance of these connected devices drive a wide range of market requirements as shown in Figure 5. Mr. Huenger said these future applications will require a variety of Advanced Packaging technologies – even more so than required in smartphones – at both the wafer and substrate level.

Some examples of applications and associated Advanced Packaging technologies currently in use in smart phones include fingerprint sensors (3DIC integration), ambient light sensors (3DIC integration), applications processors with DRAM (FOWLP or flip chip-based POP) CMOS image sensors (3DIC integration, WLP, FC), and Power amplifier/RF modules (SiP, Cu pillars and 3DIC Integration). As smartphones and future generations of smart devices evolve, he said, development of new packaging will be driven by requirements for increased functionality, higher performance, low power consumption, miniaturization, lower cost and environmental consciousness.

The growing diversity in advanced packaging, Mr. Huenger said, will require new innovation and challenges across the supply chain; this will drive the need for more robust process solutions spanning wafer-level packaging to the substrate space. Wafer level technologies such as fan-in/fan-out wafer level packaging will continue to grow in performance and applicability. He described PCB and IC substrate technologies such as micro vias, through-hole vias, fine patterning, low-roughness metal traces and insulators, thin substrates, and embedded dies and systems that will be key to bring the next generation of consumer devices to fruition. Mr. Huenger noted that high-density interconnect at both the wafer and substrate level has been generating considerable interest for some time; he also noted that electrodeposition was still the preferred method for forming interconnects such as flip-chip bumps, Cu pillar and micro-pillar with solder cap, TSVs, RDL and through-hole vias.

In summary, Mr. Huenger said that packaging solutions that can integrate various functionality within smaller and lower-cost packaging with increased performance will be required to enable next-generation connected products. He also stressed that flexibility in process capability and material selection to address a wide variety of packaging needs will be important.

The GBC session was concluded by Brandon Prior from Prismark with his talk on "The Changing Landscape in the Back End." He began his talk by echoing previous speakers on the approximately five percent growth outlook of the semiconductor market with slowing smartphone and tablet growth, and declining PC sales. He said that new market segments such as automotive, industrial and IoT will provide opportunities, but will require continuing development of advanced packaging technology and manufacturing. Mr. Prior noted the investment required for companies to stay competitive in advanced packaging has increased substantially with the growth of FOWLP, advanced substrates and 2.5D/3D packaging.

Mr. Prior described the growth in value of different package types through 2020 in Figure 6, which clearly shows the big focus in packaging to be System in Package (SiP) and wafer level packaging, including fan-out and

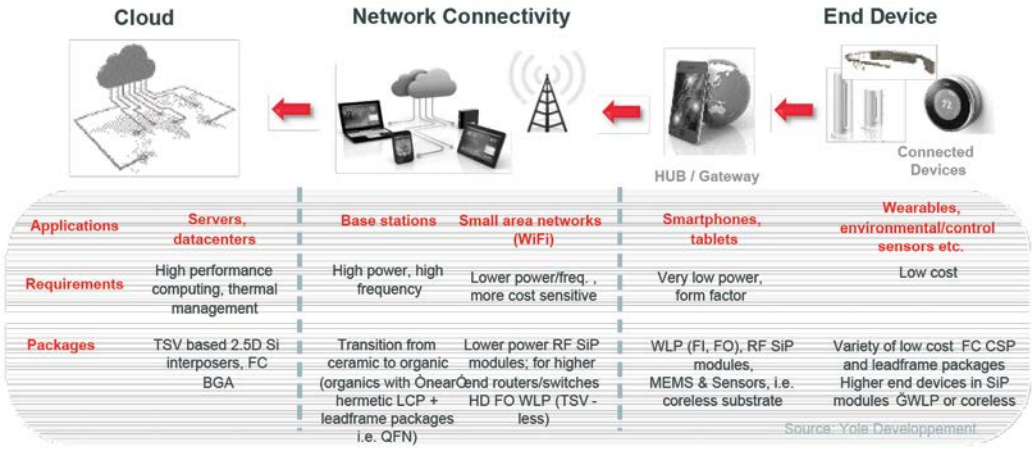

Figure 5: Wide range of requirements for future connected devices.

	2015 ($Bn)	2020 ($Bn)	CAAGR
SO/QFP	$6.1	$5.3	-2.8%
QFN/FC -QFN	$2.8	$4.0	7.1%
Wire Bond BGA/CSP	$5.0	$5.0	0.0%
Stacked CSP	$4.9	$5.3	1.7%
Wire Bond Module / SiP	$1.2	$1.0	-3.8%
WLCSP / FO -WLP / PLP	$1.2	$4.4	29%
Display Driver (Bump, Substrate, Assembly)	$1.5	$1.7	1.9%
FC Module / SiP	$0.5	$1.0	17%
FCCSP*	$3.9	$4.4	2.2%
FCCSP for DRAM*	$0.5	$0.6	2.5%
FC BGA/PGA/LGA*	$3.8	$3.4	-2.5%
Wafer Bump for FCBGA and FCCSP	$2.5	$4.0	10%
Total	$34.0	$40.0	3.3%

**Includes substrate, excludes bump*

Figure 6: Growth in IC Package Value, 2015~2020.

panel-level. One example of an application driving strong growth in SiP and WLP is the Samsung Gear S3 Frontier Smartwatch; this wearable is interesting in that it features stand-alone capability for 4G/LTE connectivity. Of the 14 total packages in this smartwatch, five are SiPs and five are WLPs.

SiPs, Mr. Prior noted, are not just for RF modules anymore. SiP technology is being increasingly deployed in other applications such as display touch modules, MEMS, and fingerprint sensors. One touch controller SiP in the iPhone 6S features three WLP, one QFN, 30 passives and a seven-layer substrate. Although EMS companies and some specialty manufacturers are offering capability to enable SiP, he said, the market is currently being well-served by traditional OSATs. Some substrate companies are looking to capture part of this market, particularly with applications that require embedded die and components.

FOWLP has been in development for ten years now, and has expanded from its initial offering as a single-chip package to include package-on-package designs (for example, InFO PoP from TSMC for the Apple A10 processor) and multi-die configurations with passives. Mr. Prior noted that many advanced packaging companies have been developing panel-level packaging (PLP) to increase throughput and reduce the cost of FOWLP, in many cases by adapting technologies and equipment from the substrate, display and solar industries. But, he observed, the industry has seen little of the major investment that would signify near-term establishment of high-volume PLP manufacturing.

He noted that substrate manufacturers have lost $400 million worth of PCB business to applications that have been moved from a substrate-based flip chip design to a FOWLP, but also said that the growth of PLP applications may provide substrate manufacturers an opportunity to leverage manufacturing expertise to win back some of that business.

Thomas Goodman is president of Izinus Technologies, a firm specializing in technology commercialization and business development. Goodman has over 30 years of experience in the development of new technologies and markets in microelectronics and advanced packaging, with special expertise in Japan and Asia. He holds several US patents in the area of advanced packaging and an MS degree in Macromolecular Science and Engineering from Case Western Reserve University. Goodman is a member of the IMAPS Global Business Council Steering Committee. He can be contacted at tgoodman@izinus.com.

IMAPS 2017

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ABSTRACTS DUE: AUGUST 9, 2017

Early Registration & Hotel Deadline: October 1, 2017

ABSTRACTS ARE SOLICITED IN THE FOLLOWING AREAS:

- **Market Drivers:** Understanding thermal challenges and business / economic drivers that influence change in electronic systems design and manufacturing – and how these impact thermal design requirements. Developing market trends, market segmentation, cost drivers and reliability factors are examples of topics that set the framework for where and what types of new technical solutions are viable.
- **Multi-Die Packaging:** Advanced packaging technologies, such as System-In-Package, Multi-Chip Module and Multi-Package Module, stacked-die, etc. provide significant opportunities for miniaturization and performance enhancements. These technologies also can introduce significant thermal and interconnect challenges that must be balanced against those benefits.
- **Mobile and Handheld Devices and the Internet-of-Things (IoT):** Wearables, mobile and medical devices, small displays, tablets and notebooks are increasingly critical for our interconnected world. These devices often introduce unique component- and system-level thermal management challenges that require novel design approaches and materials.
- **Wireless and Telecom Infrastructure:** High performance telecom hardware have challenging component and system level requirements that require technical advances to meet the evolving needs for routers, networked systems, base stations, etc.
- **Power Semiconductor Thermal Components, Systems, and Solutions:** Developments in IGBT thermal management and packaging strongly influence advances in electronic and electrical drive systems. These advances are increasingly important in the Electric Vehicle/Hybrid Electric Vehicle and renewable energy markets.
- **Mil/Aerospace:** Emerging military and aerospace systems, including avionics, RF, and microwave components and modules for phased array radar, countermeasures, and other systems, require advanced thermal management as well as high-temperature materials and packaging.
- **System-Level Cooling:** The thermal design of complex systems, such as high-performance computing systems, relies on extensive component- and system-level thermal management analysis to address the broad spectrum of issues that entail a comprehensive system design.
- **Data Center Cooling:** Data center cooling includes a variety of design optimization activities including cooling provisioning, airflow control, temperature distribution and migration paths that range from forced air convection to system liquid cooling.
- **Liquid cooling, Phase-change, and Refrigeration:** Advanced cooling methods that use liquid, latent heat and/or active cooling provide opportunities for enhanced performance and design flexibility. Effective designs must balance these advantages against factors including life-cycle cost, reliability and serviceability impact.
- **Thermal Interface Materials (TIMs) and Testing:** Advanced thermal interface materials that may include organic, metallic and graphitic materials in bulk form as well as nanoscale are enabling significant advances in the thermal management of high-performance processors, memory, telecom, IGBT, RF, and microwave components and systems. Effective testing and reliability methods and standards are critical in determining the suitability of a TIM for a given application.
- **CTE-Matching and High Thermal Conductivity Materials:** Metallic, ceramic and composite materials have been engineered to exhibit excellent thermal conductivity with controlled coefficient of thermal expansion (CTE) properties to allow for better matching with GaN, SiC, silicon or ceramic materials to reduce thermal stresses in component packaging.

PREPARATION OF ABSTRACT:

Speakers should submit one copy of a two-paragraph abstract describing their proposed 25-minute presentation no later than **AUGUST 9, 2017**. No formal technical paper is required.

Abstracts must be submitted on-line at **http://www.imaps.org/abstracts.htm**.

A post-conference DOWNLOAD containing the full presentation materials as supplied by authors will be emailed approximately 15 business days after the event to all attendees. Presentation material must be submitted onsite no later than NOVEMBER 9, 2017, and will be included on the post-conference DOWNLOAD.

Questions:
Brian Schieman, bschieman@imaps.org
You may also contact the workshop chairs.

www.imaps.org/thermal

Welcome New IMAPS Members!

January-February 2017

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Ahmad Shah Idil
Matthew Shryock
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Akhil Singh
Clayton Sippola
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Christopher Smith
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Find out more information at http://jobs.imaps.org/home

Your IMAPS Member Benefits at Your Chapter Level

Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar

Cleveland-Pittsburgh

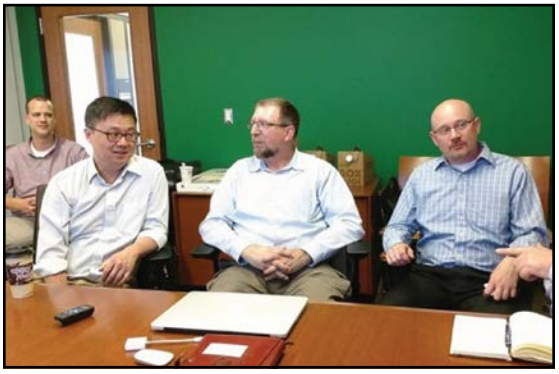
The spring meeting of our IMAPS Cleveland-Pittsburgh Chapter was held at University of Pittsburgh Benedum Hall, hosted by Professor Kevin Chen. We had three presentations and a tour of engineering facilities.

Professor Kevin Chen presented his students' work in making optical waveguides inside of glass slabs. This is basic work in optical connectivity between fibers and integrated photonic devices. We also toured Professor Chen's laboratories and the 3D printing lab.

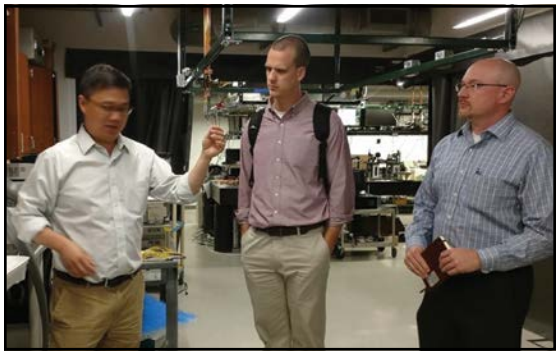
John Mazurowski of Penn State Electro-Optics Center presented a tutorial on difficulties and decisions in photonics packaging. It is most difficult to establish optical connectivity between different types of optical devices — fiber, micro-optics, or integrated platforms. John gave examples of how multiple functions could be placed in similar media. He declared that we are able to connect optical signals between continents and tiny photonic chips.

Jim Petroski of Design-By-Analysis gave a presentation on his thermal simulations of a power-over-Ethernet connector. Within the era of Finite Element Analysis (FEA) simulation (Pittsburgh is headquarters for some of this activity), Jim developed a very simple analytical model based on physical, electrical, and thermal behavior. His model achieves results in minutes — compared to several hours for some of the FEA approaches.

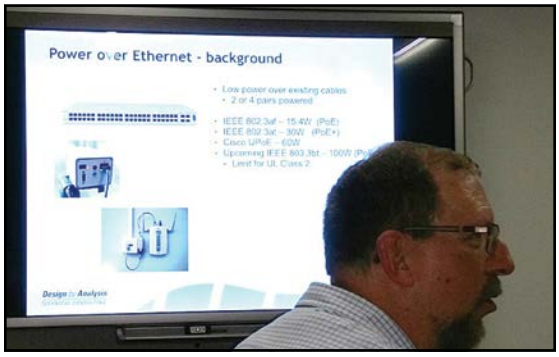
John Mazurowski



Luminaries of the Pittsburgh IMAPS chapter in a heated discussion about whether power over Ethernet should be DC or AC. These discussions occur roughly once per century.



Professor Kevin Chen of University of Pittsburgh reviews techniques for constructing optical waveguides inside of glass.



Jim Petroski of Design-By-Analysis begins his presentation on thermal simulations of power over Ethernet connectors.

INDUSTRY NEWS

Atotech's New Neoganth® E Reducer

Berlin, April 27, 2017: Atotech is one of the global leaders of specialty chemicals and equipment manufacturing. With its innovative solutions it is at the forefront of customer needs and market developments. Sustainable solutions, cost-effective products and processes and technological leadership help tackle the industry's challenges, such as the increasing cost pressures within the PCB HDI industry.

To tackle these cost pressures, Atotech has developed a new reducer process for its market leading ionic activation system Neoganth®: The Neoganth® E Reducer. This reducer process enlarges Atotech's unique desmear and metallization product portfolio and contributes to the cost-effectiveness of its market leading process solutions for the PCB industry.

Neoganth® E Reducer for horizontal applications (here: Uniplate® LB).

"The key benefits of our Neoganth® E Reducer are clearly its enhanced process stability and safety, the reduction of running costs due to the reduction in chemistry consumption by up to 25%, and the reduction of boron in the waste water, thanks to the minimized total amount of the active component in the waste water," states Lars-Eric Pribyl, Global Product Manager of Atotech's plating through hole (PTH) business technology team.

The reducer contains a special additive that deactivates the catalytically active palladium seeds accumulating in the reducer module over the bath lifetime. The active palladium particles for the decomposition reaction are thereby significantly decreased. This leads to a reduction of the reducer chemistry consumption by around 25%.

Neoganth® E Reducer is optimized for horizontal application, especially in Atotech's market leading Uniplate® LB equipment. Due to the low and stable consumption over the lifetime, process stability is improved. At the same time, an excellent backlight performance is guaranteed.

The process also fulfills highest reliability standards proven in solder shock, quick via pull, thermal cycle and interconnect stress testing. Furthermore, the new reducer is compatible to all established pH buffer systems that are applied in the reducer process step.

Contact:
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10553 Berlin, Germany
+49 30-349 85-220
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About Atotech

Atotech is one of the world's leading manufacturers of specialty chemicals and equipment for the printed circuit board, IC-substrate and semiconductor industries, as well as for the decorative and functional surface finishing industries. Atotech has annual sales of US$1.1 billion. The company is fully committed to sustainability - we develop technologies to minimize waste and to reduce environmental impact. Atotech has its headquarters in Berlin, Germany, and employs more than 4,000 people in over 40 countries.

DuPont Performance Materials Announces High-Performance Materials for 3D Printing

Products Showcase at Additive Manufacturing Users Group Conference

Wilmington, Delaware, March 20, 2017: DuPont Performance Materials announces participation in the 3D printing industry at the Additive Manufacturing Users Group Conference by showcasing high-performance materials in filament forms of DuPont™ Hytrel® thermoplastic elastomers, DuPont™ Zytel® nylons, and DuPont™ Surlyn® ionomers.

Proven over decades of use, Hytrel®, Zytel® and Surlyn® offer high quality, reliability and performance in various applications in a wide range of industries. The expansion of these high-performance materials into the realm of 3D printing will enable users to achieve the true benefits of 3D printing (greater design freedom, light weighting, reduced product development cycles and much more), allowing for rapid prototyping, part production and mass customization.

Rahul Kasat, business development leader, DuPont Performance Materials, spoke about DuPont's high-performance materials for 3D Printing on March 22. "We are very excited about the addition of these new filament-based products to our existing portfolio and the progress made in the launch of these products for the 3D printing industry. We believe these products will help our customers meet their needs for prototyping and manufacturing using 3D printing as this technology continues to get adopted across multiple industries." For additional information on DuPont's offerings in the 3D printing market, visit www.3DPrintingSolutions.DuPont.com.

About DuPont™

DuPont Performance Materials (DPM) is a leading innovator of thermoplastics, elastomers, renewably-sourced polymers, high-performance parts and shapes, as well as resins that act as adhesives, sealants, and modifiers. DPM supports a globally linked network of regional application development experts who work with customers throughout the value chain to develop innovative solutions in automotive, packaging, construction, consumer goods, electrical/electronics and other industries. For additional information about DuPont Performance Materials, visit plastics.dupont.com.

DuPont has been bringing world-class science and engineering to the global marketplace in the form of innovative products, materials, and services since 1802. The company believes that by collaborating with customers, governments, NGOs, and thought leaders we can help find solutions to such global challenges as providing enough healthy food for people everywhere, decreasing dependence on fossil fuels, and protecting life and the environment. For additional information about DuPont and its commitment to inclusive innovation, please visit www.dupont.com.

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Contact:
Melissa Bruhl
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Remtec Expands Power Transfer Via (PTV®) Technology to DBC Substrates

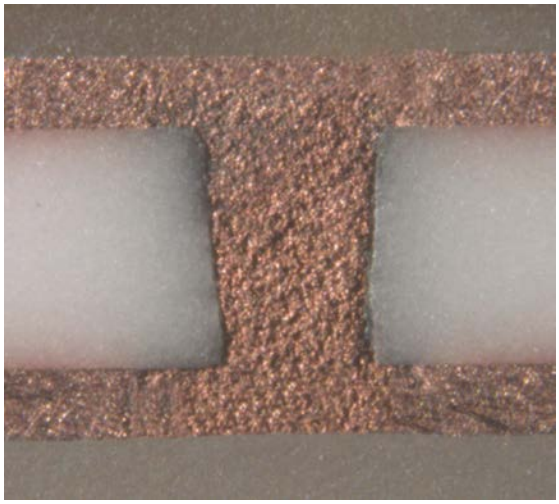
Norwood, MA, April 10, 2017: Remtec Inc. (www.remtec.com) the leading manufacturer of ceramic substrates, packages and submounts using PCTF® (Plated Copper on Thick Film) metallization, has expanded its enhanced Power Transfer Via (PTV®) technology to Direct Bond Copper (DBC) substrates. Now circuit designers are able to interconnect both sides of DBC substrates with either PTV® copper plugged vias or copper coated through-holes.

Remtec's new PTV® vias adapted for direct bond substrates benefit from the well-known quality of curamik® DBC ceramics coupled with Remtec's innovative copper via plugging and plating process. The added values of Remtec's new DBC alumina and Aluminum Nitride ceramics with PTV® vias are higher connectivity and circuit density as well as a high current carrying capacity.

Remtec's new Power Transfer Vias for DBC substrates are hermetic to 10-8 and have a low dc resistance of 2-5 milliohm per via depending on a via size and ceramic thickness. Combining a number of vias into an array allows running currents in excess of 50 AMP. These newly developed DBC substrates with vias can withstand a wide temperature range required for all common assembly methods such as SMT reflow solder, gold tin, gold germanium and Cu-Sil brazing.

Adapting PTV® vias for DBC technology allowed Remtec to significantly expand its product offering for applications requiring higher power and integration levels with space limitations and a need for wire feed-through, installation of pins or terminal headers, high current low resistance and top-to-bottom interconnects.

Remtec's Power Transfer Vias with DBC substrates are used in high power and current electronic assemblies with efficient heat removal in commercial, industrial and military/space markets. Typical examples include power packages, Light Emitting Diode (LED) devices, laser diode assemblies, hybrid circuits and other high reliability applications requiring high power and high current carrying capacity substrates.



Remtec Power Transfer Via (PTV®)

For more information, contact:
Mr. Nahum Rapoport
Remtec, Inc.
100 Morse Street
Norwood, MA 02062
Phone: 781-762-9191
Fax: 781-762-9777
sales@remtec.com
www.remtec.com

SYSTEM-iN-PACKAGE (SiP) TECHNOLOGY

Inaugural Conference and Exhibition

June 27-29, 2017 | Doubletree Sonoma Wine Country
Sonoma, California USA
www.IMAPS.org/SiP

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Principal Engineer, Qualcomm

Dr. Dongkai Shangguan
CMO, Stats ChipPac

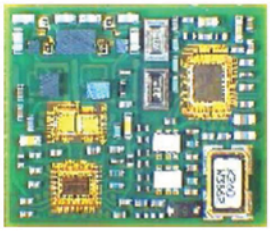
SiP 2017 is the first System-in-Package (SiP) conference fully dedicated to covering all aspects related to SiPs - market trends, system integration/miniaturization, and new technology innovation enablers to meet current and future SiP challenges. This conference will bring the entire SiP supply and design chain from OEM, Fabless, IDM, OSAT, EMS, EDA, silicon foundries, and equipment and material suppliers together under one roof.

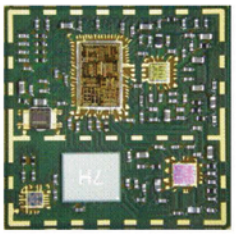
Speakers, sponsors, exhibitors and attendees will focus on the insights of SiP technology in the relaxing Sonoma wine country of California, away from big city distractions.

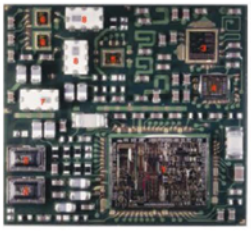
Featuring three full days of technical sessions, panel discussions, exhibitors and local activities, SiP 2017 will provide dynamic learning and technology updates for SiP-related trends and new engineering innovations from the industry's world SiP leaders.

Speaking and presenting opportunities are by invitation from the technical committee.

Visit
www.IMAPS.org/SiP
for more information







Inaugural System in Package (SiP) Technology Conference and Exhibition

June 27-29, 2017 | Doubletree Sonoma Wine Country
Learn more at ***www.IMAPS.org/SiP***

Technical Program Preview

June 27

SiP market overview, SiP in cellphone teardown of latest cellphones, SiP innovation challenges in mobile applications, active and passive components trends, MEMS and sensors technology trends, SiP package level conformal and compartmental shielding methods, human factor impacts on SiP, and SiP opportunity in China.

June 28

RF frontend SiP, connectivity SiP (WiFi, BT, GPS…), medical and wearable SiP, power module, analog SiP, MEMS, sensors and automotive SiP, SiP miniaturization techniques.

June 29

Embedded active and passives technology, Integrated Passive Devices (IPD), thin substrate technology, Fan-out solution OSAT and foundry perspectives, water proved Products/NanoCoating technology, assembly process improvement EMS perspective, enhanced new materials for SiP design and EDA tools, EMI shielding equipment.

Sponsorship and Exhibition Opportunities

Limited event sponsorship opportunities are available and won't last long. Contact Brian Schieman at bschieman@imaps.org to secure your organization's sponsorship for SiP 2017 before they are filled.

A tabletop exhibition will be held in conjunction with the technical program on June 27th and 28th.

Visit www.IMAPS.org/SiP for conference updates, including the technical program, attendee and exhibitor registration, deadlines, and more. Contact IMAPS HQ to sponsor SiP 2017 or if you have any questions.

International Conference and Exhibition on

High Temperature Electronics Network (HiTEN 2017)

July 10-12, 2017
Queen's College | Cambridge, United Kingdom

Conference Chairs:	
Colin Johnston Oxford University colin.johnston@materials.ox.ac.uk	**R. Wayne Johnson** Tennessee Tech University wjohnson@tntech.edu

HiTEN Conference Focus:
The objective of the HiTEN Conference is to have a unique forum that brings together researchers and practitioners in academia and industry from all over the world. All styles of practical high temperature electronics design and implementation approaches are encouraged, along with a variety of high temperature application areas. Today the main semiconductor focus of HiTEN is silicon and silicon on insulator (SOI). Although, HiTEN is not simply a semiconductor-focused network. HiTEN provides a conduit for the exchange and dissemination of information on all aspects of high temperature electronics. It is a global network with users, suppliers, developers and fundamental researchers dealing in all aspects of High Temperature Electronics.

- Applications in the Aerospace, Automotive, Oil and Gas, and Geothermal industries
- Devices and applications
- Novel devices
- ASICs for high temperature applications
- Memories
- Passive components
- Power devices
- Semiconductor materials
- Contacts and metallizations
- Materials
- Packaging and interconnects
- Sealants, adhesives, solders
- Reliability and failure mechanisms
- Lifetime predictions
- Accelerated life testing
- Testing at high temperatures

The HiTEN Proceedings papers will be ARCHIVED into IMAPS' new online research portal/library, ***IMAPSource®*** - www.imapsource.org. ***IMAPSource®*** currently features all IMAPS proceedings, journal papers, magazines, and other conference publications back to 2010. This portal is a fully searchable, user and Google Scholar-friendly database. The software allows for fully exportable citations, improved keyword and Boolean search functionality and customizable alerts, among many other features. The library is indexed by Google Scholar and many key scientific engines/indexes, and growing each day. *The 2017 HiTEC papers will be added in May*. For now, please visit www.imapsource.org and search. ***HiTEN 2016 proceedings can be found at http://www.imapsource.org/toc/apap/2016/HiTEN*** and older HiTEC/HiTEN Proceedings can be found in our conference section: http://www.imapsource.org/loi/apap.

Accepted papers may also be considered for publication in the IMAPS *Journal of Microelectronics and Electronic Packaging*.
For more information, please email Brian Schieman (bschieman@imaps.org).

www.imaps.org/hiten

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www.imaps.org/hiten/HiTEN2017_Sponsorships.pdf

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Advancing Microelectronics
2017 Editorial Schedule

Issue	Theme	Copy Deadline	Ad Commitment I/Os Deadline
Jul/Aug	2017 Show Issue	May 8	May 13
Sept/Oct	MEMS and Thermal Management	Jul. 8	July 13
Nov/Dec	Ceramic: Thick and Thin Film	Sep. 8	Sep. 13

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CALENDAR OF EVENTS

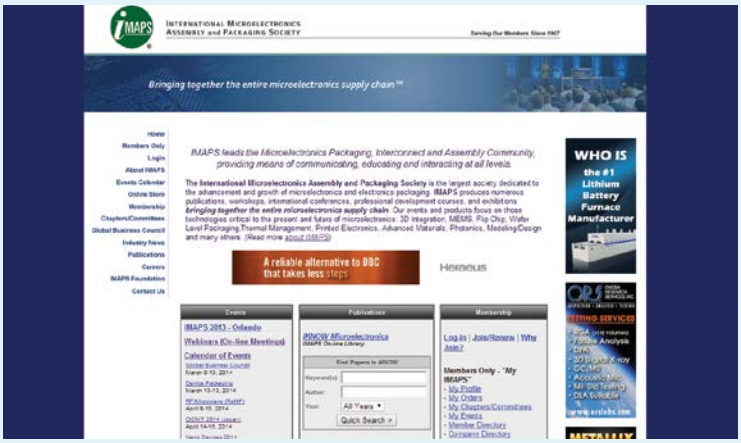
2017

	start	end	
JUNE	6-15-17	6-15-17	Advanced Technology Workshop and Tabletop Exhibition on Advances in Semiconductor Packaging Binghamton University, Vestal, NY www.imaps.org/asp
	6-27-17	6-29-17	System-in-Package Technology Conference and Exhibition 2017 Sonoma, CA
JULY	7-10-17	7-12-17	HiTEN - High Temperature Electronics Network Cambridge, United Kingdom www.imaps.org/hiten
OCTOBER	10-9-17	10-12-17	IMAPS 2017 Raleigh, NC www.imaps.org/imaps2017
NOVEMBER	11-7-17	11-9-17	Topical Workshop and Tabletop Exhibit on Thermal Management Los Gatos, California www.imaps.org/thermal

Visit www.imaps.org

for links to all upcoming events including:

- **full event descriptions**
- **abstract submissions**
- **exhibition information**
- **event updates**



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