Internet of Things

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2015 International Symposium on Microelectronics
On the Cover:
From Uniqarta, Inc., Unified IoT architecture integrating both RFID-enabled and smart objects, collectively constituting the "things" in the Internet of Things. And, from Austria Technologie & Systemtechnik Aktiengesellschaft, main requirements of IoT electronic modules. The blue boxes represent possible enablers reducing costs, form factor and increasing the power efficiency.
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Advanced Technology Workshop & Tabletop Exhibits on Additive Manufacturing & Printed Electronics
June 20-21, 2016   Lowell, MA

Advances in Semiconductor Packaging (ASP)
September 22, 2016   Marcy, New York

Advanced Technology Workshop and Tabletop Exhibit on Thermal Management
October 25-27, 2016   Los Gatos, California

IMAPS 2016
October 10-13, 2016   Pasadena, CA

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The drive toward the total connectivity of the Internet of Things (IoT) creates immense challenges in the design and assembly of the electronics. Price, size, and bandwidth are three major drivers requiring innovation. Each driver impacts the other so all three must be considered together as products and technologies are being designed.

The need for bandwidth is an interesting one. It is easy to underestimate the amount of data that would need to be transmitted. In a recent statement, the IT Director for Virgin Atlantic Airlines, David Bulman, stated that he expected their Boeing 787 aircraft to be generating about half a terabyte of data per flight. Virtually every mechanical and electrical component to these aircraft are generating and transmitting data during the flight. From the position of the flaps to the seal on the cargo door, data is being transmitted and processed. According to a 2014 ATAG report titled, “Aviation Benefits Beyond Borders,” there are over 100,000 commercial passenger flights per day. Combining these two data points suggests these aircraft alone will be contributing to 50,000 terabytes of data generated every day. Commercial passenger flights are not the only aircraft either. I have not seen data of the total amount of flights per day but I would guess that commercial passenger flights are only about one third of all flights.

If you try to extrapolate that out to all the other objects that are destined to be collecting and transmitting data the numbers are immense.

Cost and size of the electronics and sensors are critical to making IoT viable. It is easy to talk about and justify sensors in vehicles and aircraft. However, if you want to add these sensors to street lamps, parking meters, door locks, refrigerators, and every other object that you never knew needed connectivity (but soon won’t be able to live without), they need to fit into widely varying form factors and be low in cost.

One challenge that is being discussed in more detail in this issue is the optimum way to efficiently build components, along with integrating all the functions at a reasonable cost. Another challenge is the limitations of Radio Frequency Identification (RFID) technology and how RFID technology will play a role. Broad implementation of IoT is fraught with challenges. In this issue of Advancing Microelectronics magazine, you will find a number of articles discussing these methodologies and technology developments that will help to address these challenges.

Tim Jensen and Maria Durham
Indium Corporation
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Abstract
Also sometimes referred to as 2.5D integration, interposers are now a true and important component of the “3D world” based on die stacking technologies. Considered as an intermediate step in the field of high density die stacking (memory on logic, logic on logic, etc.) this technology is on the other hand fully generic to manufacture heterogeneous systems which will constitute the basic of IoT (sensor with simple logic, RF capabilities and even energy harvesting).

This paper presents first a short overview of the core technologies needed in this field. The versatility of these technical blocks, allowing efficient manufacture of a large variety of interposer-based devices, is then demonstrated through different subsystems related to IoT: sensors, passives, energy harvesters, RF communication.

Some recent achievements in smart systems based on interposers mixing together passive components, microsystems and RF functions are then presented, and more particularly a system dedicated to short range high bandwidth communication for wireless HDMI and a system for implanted medical applications. In both cases, the gain in surface area is particularly important, making such solutions highly attractive.

Key words heterogeneous integration, Internet of Things, silicon interposer

1. Introduction
Internet of things (IoT) is today the next wave in the era of computing and communication, outside the realm of the traditional desktop. In this new paradigm, many of the objects surrounding us will be on the network in one form or another, with Radio Frequency IDentification (RFID) and sensor network technologies playing a major role in this new challenge [1]. Several major industrial actors strongly push the developments of these technologies (see for example [2] or [3]), and markets analysts forecast [4] high revenue generation, with 26 billion units installed by 2020. Even if most revenues will probably be generated on services [5], it is expected that many technologies will directly profit from this strongly increased hardware demand, notably in the manufacturing of innovative, miniaturized and autonomous sensors nodes. These key elemental components will be asked to measure environment parameters, process at a first level the associate information, and communicate the resulting values to the ambient network, while working almost autonomously. Integrating at reasonable cost the energizing, sensing, processing and communicating functions in a compact standardized device requires manufacturers to perfectly control different packaging, stacking and heterogeneous integration technologies. The optimum way to efficiently build such components, which often include different chips from diverse technologies (RF chip, MEMS chip, digital chip …) consists in using interposers on which they will be placed or stacked, depending on the final component specifications. Today, interposers are used routinely to implement many functions in efficient system-on-chip [6], offering design versatility and compatibility with die based on different technologies. Indeed, different integration schemes and stacking strategies (easier to design face to back flow, easier to process face to face flow) are today available to manufacture such systems, based on the same generic core technologies, briefly described in the next paragraph.

II. Interposers for IoT devices
IoT ICs are going to be used in a very wide range of consumer products (smart watch and goggles, health patches, bottle tags, etc.) used in various environments which involve among others wearable devices, flexible circuits, micro-actuators, bio-sensors. This means that in addition to traditional IC packaging specifications new constraints have to be met like flexibility, hermeticity, and/or bio-compatibility.

On the other side, a large choice of packaging substrates is today available for SiP (System in Package) IoT type devices, from renowned ceramic to laminate and new flex materials and includes silicon interposer wafers. For each of these solutions important progress has been made recently in the aspects of integration density, manufacturability and cost competitiveness, so the choice of the best solution requires a very good understanding of the packaging requirements for a given product. More specifically technical criteria as diverse as RF signal integrity, thermal management, thermo-mechanical behavior, conformability or ergonomic properties need to be considered carefully.

However a silicon interposer which uses a large panel of wafer level technologies (WLP) provides a strong packaging platform to address the highest integration needs, the highest bandwidth RF communication, incomparable embedded capabilities and improved thermal dissipation in a small, thin package format. Figure 1 illustrates a silicon interposer incorporating ICs chips reported by flip-chip, µbumps and multi-level interconnection lines...
on front side, TSV-last, redistribution layer and solder balls for fan-out connections to BGA substrate on back side. Some features are also implemented to manage the thermo-mechanical stress at the module level and achieve a high level of reliability.

Advanced packaging technologies such as wafer level packaging are being addressed today as promising alternatives to widespread BGA flip-chip and large QFN packages and are quickly becoming a package of choice in the rapidly evolving mobile and IoT market. Moreover it is unique to achieve ultra-small form factor devices which is probably what most matters for IoT devices.

III. Core technologies for interposers

Many dedicated technological blocks have been developed in the field of 2.5D or 3D systems and are available in the main foundries worldwide. For IoT devices, the choice of the interconnection technologies is predominantly driven by the cost and the ability to high volume manufacturing.

- TSV: Technological steps for making copper filled Through Silicon Via with aspect ratios in the range 3 to 10 are today routinely controlled, with via diameters spanning between a few microns to several tens of microns. Important efforts are still made to increase aspect ratios (i.e., dealing with thicker interposers) both for economical (simplifying wafer handling) and technical (low warpage allowing larger interposer) reasons.

- Micro-bumps and micro-pillars today are the standard methods to interconnect the different die to the interposer wafer. They are generally based on Cu/Ni/SnAg solder architecture. Connections to the laminate or board are based on the same technologies but with higher dimensions. Figure 2 illustrates the different elements of connection and the pitches for die-to-die (top) and die-to-substrate (bottom) connections.

- Stud bumping with gold or silver even though not a wafer level processing technology.

- Chip attach based on conductive paste, solder joint or preform, anisotropic conductive film (ACF) usually dispensed by stencil or jet printing offers attractive capabilities for larger pitch interconnections particularly with organic interposers like laminates and flex. These interconnection technologies can be used either in back-to-face or face-to-face approaches possibly coupled with RDL routing layers.

- Routing is generally achieved with two to four layers of thick copper, either using damascene process for inorganic passivation layer, or ECD (ElectroChemical Deposition) processes for routing on organic passivation layer, as illustrated in both cases in Figure 3.

- Internal stress monitoring: 3D integration and the TSV process require chip thinning. For the TSV mid technology or the TSV last technology, chips with silicon thicknesses below 200 µm or even below 100 µm are becoming more and more usual. In relation to this silicon thickness decrease, those chips are very sensitive to the deposited layer’s stress. An accurate chip bow management with temperature is then mandatory for the chip’s mounting compatibility and further, for the reliability during operating conditions.

- Chip mounting based on flip-chip copper pillar technology requires a very good flatness. The thickness of the alloy used for the nodule nears 15 µm (copper pillar of 25µm diameter and 40 µm height).

- Temporary bonding and debonding: This is an important core technology to efficiently manufacture accurate interposers in the range 80 to 200 µm. Bonding has to handle manufacturing temperature and stress as well as comply with potential topologies. Debonding remains a critical step of the process. Depending on the internal stress level in the interposer and topology due to micro-bumps or already assembled die(s), debonding could also be impacted by the move from the 200mm to 300mm diameter. Zone bond process is now supplanted the slide-off solution to deal with 300mm wafer diameter and room temperature debonding.

- Wafer level encapsulation: Different polymer materials and techniques (pre-applied underfill, lamination, molding) are progressively introduced in the fabrication of the SiP to replace the standard packaging solutions (capillary underfill, glob top and injection molding) done at component levels.

Figure 1: Illustration of passive silicon interposer for SiP module using 3D wafer level technologies.

Figure 2: Illustration of vertical interconnection building blocks for 3D and 2.5 SIP.

Figure 3: (Left) Redistribution layer on a 12 µm planarized chip. (Right) Conformal routing on a 30µm thick die stacking.

continued on page 8
These different items constitute the central value of the integration tool box related to interposers and 3D technologies. They allow integration on interposers of the different functional blocks needed for IoT components.

IV. Integration of sensing element

Si interposers are enabling electrical connectivity on extremely small footprints and are of greatest interest for integrating microsensors (MEMS) in high value SiP. They may contain complex electrical paths and circuits that re-route signals from the microsystem and ease interfacing with additional components such as driver IC chips and RF communication chips. Moreover, lines and spaces are then reduced by an order of magnitude from traditional PCB. Furthermore, mounting Si MEMS (often sensitive to the stress field) onto Si interposers avoids the thermo-mechanical stress induced by a poor matching of the respective coefficients of thermal expansion of the device and the substrate.

These advantages lead many players today to develop product prototypes based on this approach, and notably in the field of RF, microwave and millimeter-wave systems with wavelengths of the signals approaching typical microsystem dimensions.

In this context, it can be mentioned as an illustrative example the integration of an RF switch piezoelectrically actuated (Figure 4) whose manufacturing and characteristics have been extensively described in [7]. The moving part of the switch is realized on a first wafer, while input pads and CPW (CoPlanar Waveguide) lines are realized on a second wafer (interposer) that includes all the DC command lines and RF routing, as well as TSVs to allow the moveable part to work in a controlled hermetic cavity. The fully packaged component exhibits both good isolation and low actuation voltage.

Other developments to integrate inertial sensors onto Si interposers can also be found in ref [8].

As stated by Yole [9], silicon interposers are already a commercial reality in MEMS, Analog, RF and LED applications on 150mm / 200mm, supported by infrastructures of MEMS players such as DALSA / Teledyne, DNP, IMT-MEMS, and Silex Microsystems.

V. Integration of energizing elements

Industry and infrastructures are strongly interested in abandoned sensors, which can increase process control and safety at very low cost. In this new context, self-powered systems are of great value. Such systems requires energy harvesting technologies coupled with storage capabilities. Due to the actual very low power consumption of MEMS sensing devices, manufacturing of such components becomes possible. Many solutions for harvesters supplying power in the range of microwatt to milli-watt, are today investigated, based on diverse techniques (piezoelectric, electromagnetic, or thermoelectric…). In this range of energy, harvesting systems, often manufactured by micro-technologies, are small enough to be integrated on cm-sized interposers.

The same approach can be considered for the associated storage unit needed to save and manage the harvested energy. Thin film all-solid-state rechargeable Li-ion microbatteries may be directly manufactured on interposers. Figure 5 shows examples of deposited full solid-state microbatteries integrated in diverse configurations.

With overall thicknesses in the range 5-20µ, and customizable footprint, such components perfectly fit on Si interposers for hybridization with sensors and energy-harvesting solutions. Initially developed at Léti, this technology has been transferred to ST [10] and is today available at the mass production level. A typical example of demonstrator integrating thin film energy scavenging and storage components with their associated power management can be found in [11].

VI. Integration of passive elements

One of the major advantages of using an interposer approach for SiP module is the possibility to integrate high capacity and high quality passive devices (resistors, capacitors, inductance, filters, antenna…) very close to the active ICs. This can be done either by heterogeneous integration of passives silicon chip on top of the interposer using the same interconnection scheme (flip chip or others) or by embedding the passives inside the interposer itself.

In the first approach one needs to consider the passive devices post-processing for 2.5D interconnections at wafer scale to benefit from wafer level processing capability which implies having access to the wafers. The main advantage is to use the best dedicated technology to fabricate the required passive devices giving potentially the best compromise between cost, compactness and performances.

In the second approach the integration is pushed a step further which leads to even more density. When mi-
nor added complexity in the interposer process flow is necessary for achieving the passive functions this solution can be really cost effective. For example resistors or inductances require relatively few added steps when coupled to RDL levels. Yet, it is often difficult to obtain the same performance with a co-processing approach than with a heterogeneous one.

Finally, the two approaches can be advantageously combined with various passive elements on the same interposer to offer the best compromise for a given application (Figure 6) which provide a great flexibility in the architecture design.

VII. Integration of RF elements

For IOT devices, wireless communication is one of the key features. New applications such as sub-THz imaging and automotive radar are already shaping the future of the next generation of smart devices while 5G gives a long term evolution (LTE) roadmap for communication of tomorrow. High data rates in the range of a few Gbps at short-range are nowadays achievable thanks to a larger RF bandwidth (up to 9 GHz for the 60 GHz ISM band). This progress has benefited from the advances in silicon-based RFIC front-end design, mostly inherited from CMOS technology which was initially dedicated to digital and low frequency analog applications. The complete TX/RX module including the digital to analog conversion, the PA (Power Amplifier) and the antenna has likely to be integrated at the chip level for optimizing the size and the performances.

However, the antenna stage footprint is still an issue due to the fundamental relation between the radiator’s effective area and the achievable gain. Frequencies corresponding to sub mm wavelengths require antenna size (λ/4) compatible in size with SiP technology, but it is known that CMOS integrated antennas-on-chip (AoC) suffer from low radiation efficiency (below 20%).

Antenna-in-Package (AiP) approach using a silicon interposer seems to be a good candidate to solve this issue: vertical stacking offers compact 3D integration capabilities as well as very good thermal dissipation properties. Moreover, using high resistivity silicon substrates (ρ > 1 kΩ·cm), radiation efficiencies in the range of 50% could be targeted. Léti has worked on two dedicated demonstrators to assess the interest of this technology.

A first 2.5D silicon mmW demonstrator module [12] is presented in Figure 7, where a passive interposer is mounted on a PCB with Ball Grid Array (BGA) solder balls.

Micro-bumps are used to bond the RFIC chip to the interposer with a flip-chip process. In this design, RF signals are carried through front-side transmission lines to the Tx/Rx antennas while base-band signals are driven through TSV interconnects to the back side of the interposer. The radiating element is on the top side of the interposer, backed by a cavity formed by a ring of TSV, a ring of BGA solder balls and a reflector on the PCB. The antenna cavity depth is properly calculated to achieve the desired impedance and radiation properties and is defined by the interposer’s thickness and BGA standoff. A WiHD (wireless HD) digital frame was successfully transmitted at 4 Gb/s net (7 Gb/s raw) over 80 cm without external amplifier between 2 modules. Heat dissipation was also measured showing good spreading effect of the silicon interposer for the flip-chipped RF IC (max temperature in TX mode measured below 55°C).

The second demonstrator [13] is based on a new type of integrated and efficient antennas. This approach aims to mimic an artificial magnetic conductor’s (AMC) behavior with a near-zero reflection (at least in the frequency band of interest) allowing the reflector to be placed in the vicinity of the radiating element (from 10 µm to 20 µm at 60 GHz).

The resulting patterned structure, presented in Figure 8, is called High-Impedance Surface (HIS). This new structure allows moving towards “real 3D” integration, where the RFIC could be eventually placed directly below the antenna and feed using Through-Silicon Vias (TSV) as illustrated in Figure 9.

The 200 µm-thick interposer has been designed and micro-fabricated in CEA-Leti’s 200 mm facilities. These integrated antennas have been fully characterized in an anechoic chamber over multiple frequency points. The realized gain is reported for different frequency points in Figure 10.

Figure 8: HIS antenna fabricated on Si interposer.
A 5 dBi gain is achieved with excellent cross polarization isolation (-25 dB) and bandwidth (10 % using -10 dB). The achieved radiation efficiency extracted from measurement data is higher than 40% over the band of interest for HR silicon prototypes.

VIII. Wafer level packaging solutions – specific case of medical application

As already mentioned, silicon technology offers unique capabilities of packaging solutions done at the wafer scale, giving extremely low profile protection and with functionalized layers. New polymer materials are also available using spin coating, film lamination or molding allowing protection of the active devices at the wafer scale and replacing traditional packaging solutions carried out at chip scale.

Silicon capping is used for MEMS sensors and actuators using DRIE process for the formation of the cavities, thinning and wafer-to-wafer eutectic or polymer for bonding on active wafers. This cap can be equipped with feed through via and functionalized with residual gas getters.

Thin film encapsulation on top of a sacrificial layer can be used alternately and form a protection and hermetic coating.

In the case of medical application devices, very specific requirements are requested to fulfill the stringent specifications of compatibility and reliability of implanted systems. In particular, the packaging needs at the same time to be biocompatible, meaning that the human body will accept the presence of the device during its lifetime (or the length of medical treatment) and that the body environment (blood and bone/tissue field) will not degrade or interact with the protective layers used for the packaging.

Innovative solutions are currently developed at Leti to address this challenge in the case of silicon interposers SiP developed for cardiac implantable system to monitor the heart rate.

First, the active chips (ASIC and sensor) are bonded and interconnected on the silicon interposer wafer active face up (flip chip assembly can be also used if needed). Then a silicon wafer with cavities is bonded by AuSn eutectic joint on top of the interposer wafer to form a cap around each module. Finally a protective layer is applied all around the module (Figure 11).

Concerning the silicon cap, special attention is requested to guarantee the hermeticity of the eutectic bonding over a lifetime specification greater than 20 years corresponding to a maximum leak rate as low as 10⁻¹² atm cc/s. To characterize such a low leak, a residual gas analysis (RGA) with high sensitivity is used after pressurization of the module with Ar gas. After optimization of the bonding process, leak rate was measured at a few 10⁻¹³ atm cc/s, validating the approach.

The choice of the final protective layer has led to the evaluation of a wide panel of materials and depositions techniques reported elsewhere [14] looking for criteria of both biocompatibility and biostability. For biocompatibility systemic in vitro cytotoxicity tests were carried out using MDS protocol. For biostability, corrosion rates (C.R.) of the packaging layers in PBS (Phosphate-buffered saline) solution were studied. Among the different layers tested, it is noticed that ZnO, SiN and SiO₂ films were not stable in 37°C PBS. Conversely Al₂O₃ and TiO₂ films were found to be very interesting bio-packaging layers. Functional modules were finally delivered using this integration approach complying with requested specifications.

To summarize, wafer level packaging technologies derived in some cases from MEMS and thin film deposition can offer appropriate solutions to fabricate SiP compatible with aggressive and sensitive environment conditions found in the IoT.

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**Figure 9.** RF SIP with HIS antenna fabricated on silicon interposer with 2 configurations of RF IC stacking.

**Figure 10.** Realized gain of the two-element antenna array in H-Plane.

**Figure 11.** Hermetic and bio-compatible SIP interposer for medical device applications using wafer level technologies.
IX. Conclusions
Even if most revenues of IoT will probably be generated on services, it is expected that many technologies will directly profit from this strongly increased hardware demand, notably in the manufacturing of innovative, miniaturized and autonomous sensor nodes. The key elemental components require measurement of environment parameters, process at a first level the associate information, and communicate the resulting values to the ambient network, while working almost autonomously. Today, the remaining challenge is to integrate all of these functions as efficiently as possible with the lowest achievable cost. Heterogeneous integration technologies, mainly based on interposer strategy and wafer level packaging solutions seem to be the best candidates to reach this goal.

References
Abstract
The Internet of Things (IoT) “things” are oftentimes described as active or smart devices and objects augmented with sensing, processing, and network capabilities. These smart objects are in the heart of the IoT concept but they alone cannot realize the full potential of IoT. The most ubiquitous objects in the IoT ecosystem, those that reside at the lowest system level and interact with the higher-level smart object, are based on the passive RFID technology. In the form of wireless passive sensors these objects are found in smart packaging, they form the backbone of the structural health monitoring systems, they provide non-invasive and continuous monitoring of physiological parameters, etc. RFID capability is already added to everyday items in the physical form of adhesive “smart” labels, enabling them to become “citizens” of the IoT ecosystem, but this “add-on” approach increases the implementation cost and oftentimes impacts negatively the host item’s form factor and appearance. It also does very little in terms of security and counterfeit prevention. On the other hand, the key economic factor that drives the deployment of the IoT is the cost at the end points. Therefore, the future of the IoT depends on developing an ultra-low-cost technology solution that can mass-produce low cost, RFID-enabled IoT objects on flexible substrates, ready for integration into everyday items. In some cases, such as in intelligent packaging, these objects will be non-obstructive and seamlessly integrated in their hosts. This integration will minimize the cost of implementation and will provide an insurmountable barrier to counterfeiters as they will need access to sophisticated and capital-intensive technologies in order to be able to alter or replicate the product’s embedded configuration. Presented are two disruptive processes for packaging of ultrathin flexible hybrid electronic systems with ICs as thin as 15-20 µm and as small as 250 µm per side. The first generation technology is a modification of the conventional pick-and-place technique and has been already demonstrated on a commercial-grade roll-to-roll assembly line with packaging rates exceeding 10,000 cph. The second generation technology uses a laser beam to scan and transfer ultrathin, ultra-small ICs for high-precision assembly onto various flexible and rigid substrates. It provides packaging rates significantly exceeding those of the conventional pick-and-place equipment. Reported are also results from integrating the resulting ultrathin flexible hybrid electronic devices into thin materials such as paper and plastics.

Key words
flexible hybrid electronics, embedded electronics, Internet of Things, ultrathin chip packaging

1. Introduction
After the World Wide Web and the Mobile Internet, we are now heading to the third and potentially most “disruptive” phase of the Internet revolution— the “Internet of Things” (IoT), defined as the worldwide network of interconnected objects uniquely addressable based on standard communication protocols [1]. The original IoT definition evolved to include three interrelated and interconnected paradigms—internet-oriented (network of smart objects), things-oriented (sensors), and semantic-oriented (knowledge). The usefulness of IoT can be unleashed only in an application domain where the three paradigms intersect [2-4]. Ashton points out that the IoT has the potential to change the world, just as the Internet did [1]. The U.S. National Intelligence Council (NIC) included IoT among the list of six disruptive civil technologies with a potential significant impact on US strategic interests [5]. NIC anticipates that “by 2025 Internet nodes may reside in everyday things—food packages, furniture, paper documents, and more” [5].

The IoT objects, or “things,” fall into several broad categories as shown in Figure 1: (a) passive objects with very limited identification features based on the Radio Frequency Identification (RFID) technology; (b) passive RFID objects with extra memory and sensing capabilities; and (c) active, or smart, objects augmented with sensing, processing, and network capabilities based on non-RFID communication protocols. In fact, some definitions of IoT are entirely based on the latest category: smart objects organized as a loosely-coupled, decentralized system of au-
tonomous physical/digital objects [6, 7]. In contrast with the passive objects, these smart objects can make sense of their environment and can interact with human users and other nearby smart objects [6]. These smart object are undoubtedly in the heart of the IoT but they alone cannot realize the full potential of IoT.

To be considered “citizens” of the IoT ecosystem, the IoT things must possess networking capabilities. Wireless technologies such as Bluetooth, Wi-Fi, Zigbee, etc. can and are utilized for that purpose. However, the most ubiquitous objects in the IoT ecosystem, those that reside at the lowest system level, are based on the passive (no on-board power) RFID technology. RFID is the enabling technology for the IoT objects as it encompasses three critical functions: object identification, data acquisition (if coupled with a sensor) and storage, and communication capabilities, all delivered in a very low-cost package. As such, the passive RFID technology is expected to play a key role in the IoT [2, 8]. This fact is recognized in the concept of the Unified Internet of Things Architecture [9], such as this depicted in Figure 1, where IoT integrates both the RFID and smart object-based infrastructures. In this concept, RFID objects support fundamental data acquisition functionalities, while smart objects assume more complex functionalities. In the form of wireless passive sensors, the RFID objects are found in packaging, form the backbone of the structural health monitoring systems, provide non-invasive and continuous monitoring of physiological parameters, etc.

II. Native IoT Items

The IoT as a technology is a step behind the IoT as a concept. Here, IoT technology is defined in a narrow sense as the practical application of engineering knowledge for creation of IoT objects. The easiest and simplest way to do that is just to add IoT functionally to an item. RFID capability is already added to everyday items in the physical form of adhesive “smart” labels, enabling them to become parts of the IoT ecosystem. This “add-on” legacy approach is in essence an adaptation of the existing label technology intended to serve the needs of a new application. As such it fails to deliver the attributes required for ubiquitous IoT applications: low cost, unobtrusiveness, security, reliability. Therefore, a change in the technology paradigm is needed to address the unique aspects of the IoT vision. New objects should be designed as native IoT items where the wireless connectivity is not added but integrated in the object. This is already done for physically large and structurally complex items such as smart homes, vehicles, home appliances, transportation and agriculture equipment, security cameras and systems, consumer electronics, etc. However, very little has been accomplished when it comes to integrating IoT functionality in most of the simple objects surrounding us.

It can be argued that the complete, all-inclusive implementation of the IoT concept will in part depend on the ability of the industry to produce intelligent item-level packaging, defined here as packaging which has the ability to sense or measure an attribute of the product. Let’s consider, for example, a scenario where an ordinary refrigerator (a smart IoT object), which, in turn, communicates this information to the human user. If this scenario is to be realized today, a standalone, disparate wireless RFID sensor would be added to the package. It is obvious that this “add-on” approach is not reliable; its application increases the implementation cost and, most probably, will raise bio- and food compatibility concerns. An intelligent package, where the sensor is seamlessly and unobtrusively integrated in the packaging material, will avoid the shortcoming of the add-on solution.

In other examples, the add-on electronic devices may impact negatively the host item’s form factor and appearance. The add-on devices that rely on laminating multiple layers of material with a chip sandwiched inside are also counterfeite-and tampering-prone as the device, which is also used to uniquely identify/authenticate the product, can be easily removed from one item and after tampering re-laminated on another. Embedded electronic solutions in the native IoT items minimize these vulnerabilities. Since the electronics are embedded within an individual layer of material, getting at it without destroying the host material is extremely difficult. Replacing a chip with an alternate and leaving behind no evidence of tampering is even more difficult.

III. Flexible Hybrid Electronics – Enabling Technology for RFID-based IoT Objects

The RFID IoT objects are predicted to be produced in volumes measured in hundreds of billions. DaCosta stressed that the key economic factor that will drive the deployment of the IoT is the cost at the end points [10]. Obviously, the future of the IoT depends on developing an ultra-low-cost technology solution that can mass-produce low-cost sensing RFID IoT objects on flexible substrates. A common assumption today is that all-printed electronics is the enabling technology that will propel a rapid growth in smart and intelligent packaging [11], and, from there, will enable the IoT implementation [12-14]. Scientists and engineers all over the world are develop-
continued from page 13

ing printed organic circuits working on the promise that novel RFID and sensor devices will be printed like today's newspaper at high speed, in large amounts, and at a very low cost. Over the last decade, there has been a significant increase in the efforts dedicated to the development and implementation of organic electronic components on flexible substrates, including display and lighting, solar cell, battery and passive electronic components (conductors, antennas, resistors, etc.). Research groups have demonstrated other types of application, such as sensing [15-17], critical for the IoT applications.

The proponents of all-printed electronics almost unanimously select the RFID tag as a technology demonstration platform because RFID tags are simple enough devices that must be extremely cheap, flexible, and are produced in huge volumes, all of these characteristics being the tenets of the all-printed electronics paradigm. It is not a stretch to extrapolate this line of reasoning to the sensing RFID objects. However, printed electronics hits a roadblock when attempts are made to print high-performance semiconductor devices such as fully-functional ICs. There is a growing consensus among researchers and practitioners that all-printed circuits of any significant functionality are still far in the future. This has given rise to the concept of flexible hybrid electronics (FHE). The U.S. Government has recognized the strategic importance of FHE releasing a solicitation for proposals to initiate and sustain a Flexible Hybrid Electronics Manufacturing Innovation Institute (FHE-MII) as part of the National Network for Manufacturing Innovation (NNMI) [18]. IoT is identified in this program as one of the major FHE areas of application. It is noteworthy to mention that the printed technology for active electronic components such as ICs is explicitly excluded from this program as it is considered by the Government to be still in the early stages of development.

FHE can be simply described as flexible, thinned silicon CMOS chips and other discrete components packaged on a conformable printed substrate. Integrating printed and CMOS electronics draws benefits from both worlds. The functions and performance necessary in data processing and modern communication delivered by the conventional CMOS technology are integrated in the cost-effective printed electronics technology with the resulting hybrid systems having potential for various low-cost, disposable electronic applications, including sensing RFID IoT objects. In a FHE RFID-based sensor, the methods of printed electronics are used to produce passives, interconnects, antennas, sensing elements, etc., using the conventional printing techniques such as screen printing, ink jet, gravure, flexography and others. Independently, discrete components such as ICs are ready for assembly. The preparation includes thinning the CMOS device to a thickness of less than 50 µm, at which thickness the inherently brittle Si becomes conformal to the flexible substrate. During the packaging step, the thinned ICs are attached to the circuitry on the flexible printed substrate. The completed device is then added to an item or, in case of intelligent packaging, the device is integrated in the packaging material (paper, cardboard, plastic sheet) during the material's fabrication process. The latter case is discussed more in detail in this text.

IV. CMOS Aspects of the FHE Technology

A sensing RFID IoT object is comprised of a sensing element(s) and a small microchip attached to an antenna. It is based on the passive RFID concept meaning it does not have an onboard power supply. It harvests the energy required for transmitting from the interrogating signal provided by a RFID reader. From a physical point of view, the RFID-enabled IoT object needs to be flexible and miniature. It needs to be miniature to accommodate a wide variety of form factors. It needs to be flexible so that it can conform to all types of surface geometries to which it is attached. If it is intended for integration, it needs also to be ultrathin to fit inside a sheet of ordinary materials such as paper and plastics.

To achieve the desired flexibility and thickness, the chip in the RFID-enabled IoT object must be less than 50 µm thick, preferably less than 30 µm. Such ultrathin chips have been around for years. For example, more than ten years ago Hitachi demonstrated a series of ultrathin silicon-on-insulator (SOI)-based RFID chips called a “µ-chip,” including a 75 µm thick 7.5 µm thick chip [19-22]. Ultrathin SOI chips have also been demonstrated by other groups [23-26]. SOI is a technology well-suited for ultrathin Si chips but it is expensive and not readily available [27]. Alternatively, the ultrathin bulk Si technology has been and is still being actively investigated, mostly in Europe [28].

Burghartz and co-authors provided an in-depth discussion on the ultrathin chip technology and applications in a recent publication [29]. However, very little has been reported in the area of ultrathin chip assembly. Various methods have been proposed with the majority of the work done using prototype equipment redesigned for handling thin silicon, mostly flip-chip die bonders with adapted tooling and special release tapes [30-33]. Detailed discussion on this method is available elsewhere [34-36] but the overall conclusion is that the conventional pick-and-place (PnP) tools cannot sufficiently handle chips with thicknesses of 50 µm or less. Furthermore, there is no PnP die bonding equipment that can handle a chip as thin as 20-25 µm or less [37]. Recently, Uniqarta has developed and successfully demonstrated a modified PnP process for assembly of ultrathin chips using temporary carriers, called Handle-Assisted Packaging (H-AP). Similar techniques have been reported by other research groups [38-40]. The principles of H-AP used for flip-chip assembly of an ultrathin die using anisotropic conductive paste (ACP) are illustrated in Figure 2. The process involves adhering a thinned wafer to a handle substrate using a temporary bonding material, singulating the wafer/handle stack, and assembling the ultrathin chips to a substrate using a conventional die bonder. The process is completed by removing the backside handle, leaving only the attached die at the assembly site, as seen in Figure 3 where a 25 µm thick RFID die is ACP-attached to the 7-8 µm thick silver epoxy traces printed on 50 µm thick PET substrate.

In high volume applications, the H-AP process can also be carried out on an R2R assembly line where adhesive dispensing, die placement, adhesive cure and handle removal are each carried out at different locations along the line. As an example, Figure 4 shows a 25 µm thick RFID die assembled using a high rate assembly line to the 12 µm thick aluminum pads of an RFID antenna on a 75 µm thick paper substrate.

The H-AP process is designed for assembly of ultrathin dies onto various substrates. It can be applied for assembly of dies with various thicknesses; however, H-AP is most efficient in the range of 15-50 µm, where the con-

The H-AP process is designed for assembly of ultrathin dies onto various substrates. It can be applied for assembly of dies with various thicknesses; however, H-AP is most efficient in the range of 15-50 µm, where the con-
conventional pick-and-place tools cannot operate efficiently, especially at high rates.

To overcome the problems with PnP handling of ultrathin chips, unique methods such as fluidic self-assembly (FSA) [41, 42] and even single bead-manipulating apparatus using micro vacuum tweezers [19] and others [38, 43] have been suggested as alternatives with various degrees of success. Using the energy of light for transferring semiconductor dies has been reported by Karlitskaya [44, 45], A. Piqué [46-50], J. Sheats [51-54] and J. Rodgers’s group [55]. The laser has the potential to place chips with transfer rates an order of magnitude higher than those achievable with the conventional PnP [56, 57]. However, the current methods suffer from significant drawbacks including low precision and placement accuracy. To address these problems, a team from the North Dakota State University, Fargo, ND, has developed and demonstrated a process called Laser-Enabled Advanced Packaging (LEAP) [34-36, 58]. A central part of the LEAP technology is the thermo-mechanical Selective Laser-Assisted Die Transfer (tmSLADT) technique designed to overcome the problems with the previously reported laser-assisted die transfer methods.

The basic concept of this method, illustrated in Figure 5, includes the use of a dual dynamic release layer (DRL) to attach the die to be transferred to a laser-transparent glass carrier. The DRL comprises both a blistering layer and an adhesive layer. tmSLADT does not rely on the kinetic energy of a plume of vaporized material or solely on the gravitational force to transfer the dice, both mechanisms used by the other groups. Instead, the laser pulse creates a blister in the blistering layer, thus confining the vaporized material within the DRL without rupturing it. The force exerted by the blister, in addition to the gravitational force of the die, initiates the transfer over the gap. This technology was used to transfer ultrathin (20-µm thick) chips as small as 250 µm per side (Figure 6a). In 2012, tmSLADT was used to fabricate and demonstrate for the first time a functional electronic device (an RFID tag) packaged using lasers (Figure 6c).

V. Device Integration within Sheet Materials

Integrating an electronic device into paper and other sheet materials can be done in a variety of ways briefly explained in the following sections.

A. Dry Lamination

In the dry lamination approach, known in the industry as “conversion,” one or two sheets of paper or plastic are
added to the RFID inlay using adhesives. This process is commonly used in the industry today to fabricate electronic tickets, access cards, RFID labels and tags, etc. The problems with this approach are discussed in the previous sections in the context of the add-on approach.

B. Single Ply Embedding

The electronic device can be embedded during the process of making a single ply of paper in a manner similar to this used to embed security threads in banknotes. The ultrathin electronic device packaged on an intermediate paper substrate is inserted into the pulp slurry right after the slurry is spread onto the moving "wire" or screen below, which vibrates to induce micro-turbulence in the stock. At this point, the fibers in the pulp consolidate around the electronic device as the water in the slurry drains through the wire. The wet sheet of paper is then pressed to further consolidate the fibers of heated drier rolls. To achieve a good quality surface finish, the sheet is rolled through a set of high-pressure rolls (calender stacks). Calendering compacts the viscoelastic paper material and changes its surface properties through pressure, friction, and heat. This process creates a complex set of stress conditions to which the brittle chip material is subjected. Preliminary experiments have indicated that ultrathin FHE devices can survive the paper making process, including the calendering step.

Examples of RFID inlays embedded in a single ply of paper are shown in Figure 7. Figure 8 shows examples of how a similar approach can be used to demonstrate embedding an ultrathin RFID inlay in a paper slurry in the paper molding process used to fabricate, for example, egg cartons and similar paper products where calendering is not used.

Experiments were also carried out for embedding ultrathin electronics in polymer sheets. The manufacturing process for these materials is based on the extrusion of a polymer melt and is completely different from the methods used to fabricate paper but, nevertheless, it still lends itself well to single-ply embedding, as shown in Figure 9.

C. Wet Lamination

Wet lamination is a process where the electronic device is embedded in the paper between two or more wet sheets of paper. Examples of RFID inlays embedded in paper using this method are shown in Figure 10.

The embedding process works well when the substrate and host materials are the same or similar, for example, a paper inlay in a paper sheet. In this case, the adhesion between the RFID inlay and the paper sheet is very strong and doesn’t allow the removal of the inlay without destroying it. Figure 11 shows the results of adhesive testing done following the recommendations of ISO 2409 since a test method for evaluating the adhesion of paper to a strip of embedded material is not currently available. ISO 2409 describes a test method for assessing the resistance of paint coatings to separation from substrates when a right-angle lattice pattern is cut into the coating, penetrating through to the substrate. The pattern is then brushed lightly with a soft brush several times back and forth along each of the diagonal lines of the lattice pattern, after which the pattern is examined for flaking. As seen in Figure 11, non or minimal flaking was observed after brushing in all test sites where a lattice pattern was cut in the host material in areas located above the embedded inlays.

In case of dissimilar material, for example PET inlays embedded in paper, adhesives such as polyvinyl acetate-
VI. Conclusions
IoT is a disruptive technology which has the potential to change the world by creating information highways in the realm of physical objects. The passive RFID sensor technology is expected to play a key role in this new paradigm. The current, legacy approach in which the IoT functionally is simply added to an item to make it a part of the IoT ecosystem fails to deliver the attributes required for ubiquitous IoT applications: low cost, unobtrusiveness, security, reliability. New objects should be designed and built as native IoT items where the wireless connectivity is not added but integrated in the object. Such objects will be produced in volumes measured in billions and even trillions. This will be economically feasible only if the industry develops an ultra-low-cost technology solution that can mass-produce sensing RFID-enabled IoT objects on flexible substrates. The advancement of the FHE concept, which combines the methods of printed electronics for passive components with the functionality of thinned flexible CMOS integrated circuits, holds the promise of delivering this capability. Critical steps in this technology are the processes for thinning and, especially, for attaching ultrathin chips to flexible substrates at high production rates and low cost. The conventional pick-and-place tools cannot sufficiently handle such chips. The two methods for ultrathin chip assembly presented in this text overcome the limitations of the traditional technology. The H-AP method is capable of attaching chips with a thickness as small as 15-20 μm using conventional Pick-and-Place tools. The LEAP technology is capable of assembling not only ultrathin but also ultra-small chips with lateral dimensions below the limits of the current PnP tools. Both methods use COTS wafers and a series of conventional operations to prepare the ultrathin chips for assembly.

The concept of ubiquitous native IoT objects requires embedding the electronic devices in thin ordinary materials such as paper and plastic sheets. This concept requires new methods where the device is integrated in the sheet material very early in the manufacturing process of this material. Methods for a single- and multiple-ply integration and lamination result in an electronic device that becomes an integral part of the sheet material and as such can be used for IoT applications such as smart packaging, financial and security documents, unobtrusive sensors, and similar.

Acknowledgment
Laser Enabled Advanced Packaging (LEAP): The author thanks his colleagues O. Swenson, N. Schneck, R. Miller, F. Sarwar, M. Semler, J. Yan, Zh. Chen, and S. Datta, who through the years provided expertise that greatly assisted the research in various capacities. The support from the staff of the North Dakota State University’s Center for Nanoscale Science and Engineering is gratefully acknowledged.

The work in this area was supported in part by the Defense Microelectronics Activity (DMEA) under agreement numbers H94003-08-2-0805, H94003-09-2-0905, and H94003-11-2-1102. The U.S. Government is authorized to reproduce and distribute reprints for government purposes, notwithstanding any copyright notation thereon. The support provided by the State of North Dakota through the EPSCoR – PDC Program is also acknowledged.

Handle-Assisted Packaging (H-AP): The work in this area was supported in part by the State of North Dakota, Department of Commerce Technology Based Economic Development (TBED) Grant Program. The collaboration of our colleagues from Mühlbauer GmbH, Roding, Germany, was very important for the success of this work. The author is also immensely grateful to his colleagues from Uniqarta – R. Kliger, Y. Atanasov and B. Scholz, without whom this work would not be possible.

Smart Paper: The support provided by K. Doelle, SUNY Syracuse, NY, and by our partners in a number of paper companies was invaluable. The team from Uniqarta – Y. Atanasov and B. Scholz – spent endless hours making sure the idea of integrating two very different technologies – the ancient papermaking technology and the innovative ultrathin flexible hybrid electronics – becomes a reality.

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Novel PCB Technologies Enabling Smarter IoT Applications

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Abstract

Be it the trillion-dollar economy dreamed up by Cisco Systems at one extreme, or the multitude of small crowd-sourced projects at the other, there is no denying that IoT is capturing minds and making the news. Each company is vying for a piece of the pie, with semiconductor suppliers scrambling to call the latest releases “IoT-ready.”

The printed circuit board (PCB) industry is well aware of the IoT revolution, and is of course finding innovative ways supporting this trend. The three main characteristics of IoT electronic modules are: (i) low cost; (ii) small size; and (iii) high power efficiency. AT&S embedded component packaging (ECP®) is a potential technology fulfilling such requirements. ECP® consists of placing active and passive components within the PCB itself, the system can:

- be more integrated, as components disappear from the surface, making space for additional functionality, larger battery or simply fit in a smaller housing,
- have lower losses, as stacking SMT components on top of the embedded allows for short connections, thus lowering connection resistance and parasitic effects,
- be created faster, to enable dimensional and functional integration without relying on complex and costly SoC design,
- reduce costs due to the loss of separate component housings and reduction of overall systems PCB size (bare die size is only a fractional part of the chip package).

Starting with a backgrounder on common embedding technologies currently available from leading suppliers, the article will present recent advances from AT&S’s ECP® (Embedded Component Packaging). Expanding from that field, the document will explore its future and extreme applications, such as high-power (multi-kW) and fine-pitch fields for industrial and automotive devices, showing the scalability of the technology and the evolutions supported by the EU-funded EmPower project.

Keywords
embedding, power, SiP, system-in-package, reliability, sensor, IoT, security

1. Introduction

Communication with everything, everywhere at any time leading to increased information flow, better usability and improvement of daily life. Conflicting reports are appearing with regards to IoT (Internet of Things) or IoE (Internet of Everything). Some companies claim that it will provide the next boost to the semiconductor industry, while others caution that the desired ubiquity will require a dramatic drop in ASP, which would counterbalance the volume increase. Depending on the final application, low cost, miniaturization and high power efficiency, i.e., leading to a low power consumption, are essential requirements which must be considered to manufacture IoT electronic modules (Figure 1).

AT&S® Embedded Component Packaging (ECP®) technology fulfills such requirements in an increasing number of market segments. No matter if only a few passive components or multiple ICs ranging from low to high power at fairly high frequencies should be integrated into the PCB, embedding is taking hold of all application fields. The integration of components (passives and actives) within the PCB body allows not only increasing the real estate on the external layers, but also having a shorter path to the component in z-direction. A decreased length of the copper tracks leads to the reduction of the impedance, meaning reduced losses and high power efficiency. As already mentioned, in IoT devices the low price for the whole electronic module is of high relevance. Besides the performance improvements characterizing ECP modules, users are banking on the economies of scale enabled by large-panels format adopted in PCB production. Indeed, one standard PCB panel measures 457*610 mm, corresponding to about 3.8 off 300 mm wafers. A further price reduction will also come once the larger lots of ECP-based IoT penetrate the market. The combination of potential savings coming from a large production format together with the lower costs of base materials is what distinguishes ECP as an outstanding technology addressing the IoT.

2. Embedding Variants

Component embedding cannot be counted to the latest breakthrough in PCB manufacturing, as companies and research institutes have worked on embedding in various shapes and functions for more than 30 years. Former quasi embedding methods similar to standard packaging processes like wirebonding and soldering combined with special cavity cuts led to a mind-set change in the industry towards a combination of adhesives and plated vias. Such
a strategy offers the best manufacturability (through close-
to-standard PCB processes) and reliability. Of course, use
of embedded layers (either resistive and/or capacitive) is
widespread, especially for MEMS-microphone substrates,
but the functionality is quite limited, and thus will not be
covered in this document.

It will instead focus on the most common component
embedding methods in general and especially provided
by AT&S (Figure 2). Although, the figure is also illustrat-
ing a 2.5D cavity for chip integration, this technology will
not be treated here as it was already discussed in a previ-
ously published paper [8].

A. Embedding processes at a glance

Based on the application area, an appropriate technol-
ogy implementing the most important features according
to the product’s specification must be selected. As an ex-
ample, Blade, developed by Infineon Technologies, was
created especially for high-power applications. By diffu-
sion soldering the die on a thick copper foil, low thermal
resistance and high thermal mass are achieved. This direct
thermal path is of particular interest for power-manage-
ment applications, targeting predominantly the server
space.

SESUB (Silicon Embedded in SUBstrate) from TDK-
EPC is a substrate-based technology. The materials and
production formats are those common in the substrate
industry, so production costs are a bit higher compared
with FR4-based versions, but much finer pitch and in-
terconnections can be created. For example, Cu pillars
with a 120 µm pitch on a 50 µm thin die are connected
to create one of the most integrated baseband modules
[2]. Typical targets include processor-based and RF mod-
ules, where the complex ICs are preferentially embedded.

UTCP (Ultra-Thin Chip Package) invented by CMST re-
spectively IMEC provides a 30 to 70 µm thick embedded
package, integrating thinned down semiconductor dies of
about 15 to 35 µm. Flexibility is reached through the us-
age of polyimide as a base material. The finished package
can be further integrated into a flexible PCB. The main
focus is on sensor systems in medicine, healthcare, sports
and consumer electronics where the necessity of small,
lightweight and flexible circuits is given.

B. Standard ECP®

With Embedded-Component Packaging, AT&S is
manufacturing the most popular embedding technology
[1]. Developed during the EU-funded HERMES project
[3], it relies on HDI-like processing of a PCB core contain-
ing the die.

Being simple, sturdy and capable of heterogeneous in-
tegration makes it an ideal candidate for small system in
package (SiP) solutions.

C. ECP®-P

The first evolution of Standard ECP® called ECP®-P
for PARSEC (PARtially-exposed Surface-Embedded Com-
ponent) addresses high-power applications. The die is
bonded within the core with one side left exposed. Micro-
vias connect the encapsulated side, while full-surface
plating takes care of the other one.

The technology is being developed within the EmPow-
er [4] EU-funded project, with other partners including
Continental and STMicroelectronics. Having a direct Cu
connection from the die enables very-high powers, with
targeted applications ranging from footprint-compati-
ble power diode as replacement for DPAK versions (50
W class), to full modules for electrical vehicles (50 kW
continued on page 22
Due to the encapsulation on five sides of the component anchoring it to a finished core, lower warpage and more flexibility in build-up choice is achieved. One important consequence is the accommodation of dice up to 12*12 mm in size, for applications as varied as processors or high-power components.

D. ECP®-C

The latest variant of ECP® called “-C” for centre core, extends its capabilities for heterogeneous SiPs. By first processing the core, then placing the components within a cavity for encapsulation with an epoxy, the interconnects to the die are created through microvias when the additional layers are laminated around the centre core.

3. Applications

As mentioned earlier, each embedding flavor has its own sweet spot, which will appeal to one aspect of IoT or the other. Current IoT systems are ranging from environmental monitoring, over medical and healthcare systems to transportation, manufacturing and even more. From the products’ point of view, the diversity of applications can be lessened to some basic electronic circuits an IoT device contains.

A. Sensors

Be it for monitoring the device itself, interacting with the user or the environment, or any other reasons, sensor integration is at the core of IoT. Of them, microphones are of particular interest. They are expected to be found in smart homes (to pick up spoken commands from the user, like Amazon’s Echo or Google’s OnHub), obviously mobile phones and smart cars (for active noise cancellation), but also to monitor the operating conditions of machineries (vibration monitoring). On the specific case of smartphones, analysts such as Yole Développement expect the number of components to increase from the current two (front and back recording) to five or even seven to improve functionality (including surround recording, localization and other gimmicks to be invented). This increase will require a drop in size and pricing to fit the bill of materials and the available space, without compromising on performance.

A further final advantage is linked to electrical performance. A low-cost PCB-based substrate typically uses 50 µm wide, 25 µm thick Cu tracks. Comparatively, wire-bonding would use a Cu wire with a diameter of 25 µm.
This 60% improvement of linear resistance can positively affect power consumption.

<table>
<thead>
<tr>
<th>Section</th>
<th>Linear resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wirebond 0.0005 mm²</td>
<td>1.22 mΩ/mm</td>
</tr>
<tr>
<td>PCB track 0.0013 mm²</td>
<td>0.48 mΩ/mm</td>
</tr>
</tbody>
</table>

Table 1 – Linear-resistance comparison between wirebond and PCB track of typical dimensions.

B. Power

In high-power electronics, wirebonds are often a limiting factor to high-frequency switching. This comes from the fact that the contact point is the largest point of interconnect, and the wire itself has a much smaller diameter. By comparison, the microvia (so the connection to die) is the smallest one, thus the limiting factor. A first-level comparison between QFN and equivalently-sized embedded package showed that inductance of each interconnect should be about 30% smaller [5].

New power architectures are being developed to take advantage of the high switching frequency enabled by GaN-on-Si and other III-V-based products. Flagship products such as the Dart from FLNix show a dramatic size reduction of the power supply, freeing up space for an increased payload. A rule of thumb is that an increase of the switching frequency by a factor ten permits a volume reduction by a factor two [6].

C. Security

In the last few years, news organizations have reported about the various security testing conducted by researchers on connected devices, be it cars, fridges or LED lights. Each time a new hole was detected, the targeted company pledged to do better and to not be caught again. One common theme across those stories is that vulnerabilities were mostly linked to poor software implementation. Once software becomes more secure, attackers will try to find the next-best venue, which might require physical access to the processors and memories. Therefore, developments of active anti tamper electronic packages are already in progress. Various types of physical attacks can be detected, resulting in the erasure of the electronic data contained [7]. Of course, security is a constant race of improving technology (both for offense and defense), and no system is ever safe, but embedding will provide an additional tool to protect valuable data.

D. Communication

WiFi, Bluetooth, ANT, Cellular and many more communication standards can be found in the latest products for IoT applications. Modules, realizing one of these communication interfaces, do have a decisive characteristic in common: the amount of SMT passive components for external circuitry resulting in a fairly large spaced dimensioning of the PCB. Additionally, integrated microstrip antennas are scaling the required space to a certain extent. When embedding capacitors as well as resistors directly beneath the integrated circuits into the organic material of the PCB, not only the miniaturization aspect can be emphasized, signal integrity is improved according to reduced track lengths and thus, minimized parasitic effects.

Several famous communication-module manufacturers are currently evaluating the benefit of embedding compared to standard printed circuit boards, leading most probably to novel products in the upcoming months.

4. Conclusion

IoT enabling embedding technologies provided by AT&S were discussed in this article. Different ECP® approaches adjusted to a diversity of products, support electronic devices in improvement of miniaturization, electrical and thermal performance. Within this work we mainly focused on “Internet of Things” applications. Particularly, packages related to sensor-, power-, security and communication systems were addressed.

Of additional note is one of the deliverables of EmPower. Atotech is finalizing its double-sided wafer-plating line, with dissemination expected after project completion in 2017. Offering the semiconductor world the possibility of creating large Cu pads on both sides, even on thin wafers (as the line is compatible with the TAIKO process from DISCO Corporation), will open the supply chain for innovative packaging architectures, especially on embedding.

5. Acknowledgment

The authors would like to thank the team from the EmPower project for the data provided.

6. References

System-in-Package for the Next Big Thing at Device Packaging in Sunny Arizona

By Thomas Goodman, Izinus Technologies, tgoodman@izinus.com

What is the Next Big Thing in electronics: IoT? Smarter smartphones? Autonomous driving vehicles? More important, how will our industry develop and produce the necessary systems to enable these products? These questions and more were addressed at the IMAPS Global Business Council’s half-day plenary session on System Integration and Package Assembly & Supply Chain Implications, held for the second year in a row as an integral part of the Device Packaging Conference in Fountain Hills, Arizona, on March 16, 2016.

The GBC event was kicked off by Bill McClean, President of IC Insights, who asked the question, “Are IC Industry Cycles Dead or Just Sleeping?” Mr. McClean started his talk with an analysis of the effect of currency exchange rates on market growth rates and forecasts. The worldwide IC market showed a -1% growth rate for 2015 when calculated using that year’s exchange rates. However, at 2014 exchange rates, the growth rate becomes a +3% increase. To get a real view of market growth, he suggested looking at unit volume: as shown in Figure 1, in 2015 quarterly IC unit volume continued to grow on the 6% trend line in place since 2009.

After examining the trend of IC market growth compared with that of worldwide GDP, Mr. McClean noted that both have evened out since 2011. Hence, he contends that the cycles are not dead, but are in fact just sleeping. Based on his IC Industry Cycle Model, Mr. McClean says that determining what comes next is easy; the difficult part is in knowing when it will come. However, he noted that cycles will typically start with radical departures from a current trend.

He also noted that there has been a large increase in M&A activity in the IC industry: over $103 billion in agreements were made in 2015, versus about $63 billion in total from 2010 to 2014. The landscape of the Top 10 worldwide semiconductor sales leaders changes significantly when M&A activity is taken into account: the Broadcom/Avago merger moves the two companies from the bottom of the Top 10 to number five, while the merged NXP/Freescale moves into the Top 10 at number 8. Mr. McClean predicted that M&A activity would continue but likely not accelerate.

Mr. McClean did note that M&A offers were very prevalent in China due to large infusions of cash from central and provincial governments; however, only two IC suppliers were acquired by Chinese groups in 2015 in addition to three deals with OSAT suppliers.

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Table 1. Devices and advanced packaging in today’s wearables. Source: from TechSearch International
E. Jan Vardaman, President of TechSearch International, followed with a discussion on “Hardware Opportunities for a Connected World.” There are a number of areas where the use of connected Smart Systems is producing benefits in our lives, including healthcare, industrial automation, automotive electronics, entertainment, home automation and energy production. She noted that the smartphone, being a tool with diverse wireless connectivity and sensors, will play a key role in controlling and accessing connected devices.

Smartphones and other handheld or wearable connected products present special design and performance challenges. In addition to being user-friendly and comfortable, some of these products must always be “on” — for example, health monitors can never go to sleep! Low-power design is critical for these products. Furthermore, they must be able to withstand a multitude of environmental stresses: UV light, sweat, mechanical stress, thermal/moisture cycling in washers and dryers, cleaning fluids, water, sunscreen and others. A wide variety of advanced packaging is employed in these products to meet reduced form factor and cost targets. A list of devices and advanced packaging used to interconnect them in various wearables is given in Table 1. Another key factor for acceptance of these products, noted Ms. Vardaman, was appropriate and pleasing design; a health-monitoring product for a senior citizen is of little value if it never worn due to being cumbersome or unattractive.

Ms. Vardaman then discussed new competencies required to enable future connected smart systems, including microcontroller firmware design, MEMS design, and technology and software algorithms. One excellent example she provided of seamless connectivity of all these systems is in the Connected Factory and Industrial Automation. Production and assembly machines must verify that they are making product correctly, and they are increasingly outfitted with a variety of sensors to detect color, rotation, speed, roughness, warpage, and even sound (the signature ‘click’ generated by a successful connector insertion can be evidence of a job well done).

Sensors and online process monitoring and control are being employed to avoid unplanned downtime and other failures. Ms. Vardaman said that unplanned downtime costs are over $1 million per hour in automotive manufacturing. Factory-wide online monitoring and control can require the integration of thousands of tools, sensors and systems, as well as a functioning IT infrastructure of hardware and software. One example of this is the image sensor-based control system diagrammed in Figure 2. Systems of this type even have applicability beyond a factory setting, she noted, as they are also used in camera surveillance and face recognition, gesture interfaces for gaming, and augmented reality devices.

Rozalia Beica, Chief Technology Officer of Yole Development, assessed the current and future state of System-in-Package (SiP) with her talk on “SiP Trends in Handsets and Mobile Applications.” She defined SiP as two or more components with different functionalities packaged in a system or sub-system. Thus, it is a platform that can bring together disparate technologies such as CMOS, BiCMOS, GaAs and GaN within the same package. This is an important trend in mobile electronics and packaging, as she noted that the smartphone will be the gateway to IoT.

Figure 2: Embedded vision: factory-wide online monitoring and control.

In future smartphones, Samsung is said to be integrating an applications processor/memory and eMMC (em-

Simon could perform basic address, phone book, calendar and notebook functions (in addition to being able to make and receive calls), it also had the capability to host ‘apps’ such as mapping, games and spreadsheets through a cartridge slot in the phone body. As the comparison of past and current phone characteristics in Figure 3 shows, device, display and packaging technology have brought us a long way to our current generation of smartphones!

Ms. Beica described how Moore’s Law scaling alone has inherent limitations in the ability to address future market requirements in smartphones. This has driven the development of advanced packaging technologies such as SiP to enable increased miniaturization, functionality and performance at lower cost. SiP is already a dominant packaging platform in smartphones that has brought integration and miniaturization to a number of applications; indeed, Ms. Beica showed a teardown of the iPhone 6s Plus that boasts a total of 13 SiP that support diverse functions and components such as PA modules, Wi-Fi modules, SAW filters, an antenna switch and a Front End Module. By contrast, Samsung’s Galaxy S6 and Huawei’s Ascend Mate 7 each have seven SiP onboard.

In future smartphones, Samsung is said to be integrating an applications processor/memory and eMMC (em-

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bedded multimedia controller: flash memory with flash controller) in a SiP in its Galaxy S6 edge+; this will enable a 40% reduction in mounting area. Apple, on the other hand, has announced that it will package its A10 processor for the iPhone 7 in TSMC’s InFO fan-out WLP with through-package vias.

Ms. Beica notes that SiP integration is clearly a major trend in smartphone evolution. OSATs such as Deca Technologies, Amkor, ASE and SPIL, and foundries like TSMC and Samsung are developing more complex Fan-out WLPs to meet this market need. Roadmaps show that the original single-chip FOWLP technology currently in use for baseband and other ICs is being used as a platform for development of multi-die solutions with interposers, package-on-package (PoP) mounting and face-to-face mounting. A sample roadmap Ms. Beica showed from STATS-ChipPAC is given in Figure 4.

Jim Walker, Vice President of Research at Gartner, followed with an analysis of where our industry at large is headed in his talk, “IC Industry Consolidation and the China Effect.” Mr. Walker noted that the PC and smartphone industries are maturing and that manufacturers are eyeing IoT as a hot new market. Market entry through development of technology, manufacturing, markets and/or customer base is expensive and time-consuming. He said that with the cost of new fabs approaching $7 billion and expected design costs for an advanced-node high-end SOC in 2018 at over a half-billion dollars, acquisition of the right company can be a quick and relatively inexpensive entry into a growing market.

Mr. Walker continued by describing economic conditions that make the current environment ripe for mergers and acquisitions (M&A). One driving factor is the availability of cheap capital, with low interest rates and low valuations for chip, tool and IP companies. As interest rates rise in the future – an announced strategy of the Federal Reserve Board – the window of opportunity for investment and acquisition will shrink. Low company valuations in our industry are demonstrated by the current four-year low of the price/earnings ratio for the Philadelphia Semiconductor Index of 30 leading semiconductor company stocks.

So, Mr. Walker concluded, the ground for M&A is fertile. Indeed, the semiconductor industry closed almost $40 billion in acquisitions in 2015 (he noted that the number previously quoted by Mr. McLean was for announced mergers.) As shown in Figure 5, almost one-quarter of the companies in the Philadelphia Semiconductor Index have agreed to be acquired.

Mr. Walker continued his talk by describing China’s activity in growing its domestic IC manufacturing, and how that is affecting the industry and the economy of other nations. He explained that China has ample incentive to grow its domestic IC manufacturing as its internal markets represent 33% of the total purchasing TAM for semiconductor chip vendors. China also has greater than a $150 billion trade deficit from import/export of ICs and discretes.

China’s State Council recognizes that IC manufacturing is critical to China’s economic growth and national security, so it issued the “Made in China 2025” plan to grow domestic IC manufacturing. However, in March 2016, China unveiled a new five-year plan as the end date of 2025 was not sufficiently aggressive. Mr. Walker said that other countries are feeling threatened by China’s semiconductor goal; he noted both the head of Korea’s Semiconductor Industry Association (KSIA) and Taiwan’s president-elect made impassioned appeals to their respective governments to counter the market threat from China and maintain their countries’ edge in semiconductors.

The GBC event was concluded by Professor Rao Tummala, Director of Georgia Tech Packaging Research Center (PRC), who spoke on “System Scaling for New Era of Automotive Electronics: An Ultimate System Integration Opportunity for R&D and Supply-Chain Manufacturing Consortium.” Prof. Tummala described the coming New Era of Automotive Electronics (NAE), the main goals of which are to reduce automobile fatalities, improve driving and energy efficiency, and to improve human productivity. He noted that if a three-hour car commute to and from work for a seven-hour workday could be turned into productive time, it would open an additional three hours in the day for something enjoyable like golf.
Prof. Tummala went on to describe new technologies, an educated workforce, a global supply chain, roadmaps and standards as critical needs for NAE. However, he says the Grand Challenge for NAE is the further development of essential technologies such as displays, software, networks, engine control units, power delivery and autonomous driving. Key opportunity areas, shown in Figure 6, will be electronics for sensing, consumer function, high bandwidth, high power and high temperature.

There are still fundamental challenges to be met in developing ICs, device packaging and systems packaging to meet NAE needs. There exists a gap between transistor scaling and system scaling; pitch and interconnect density are not reducing as quickly as node dimension. This leads to a tremendous need for advances in system scaling that can be realized through development of technologies listed in Figure 7.

To address this massive development challenge, Prof. Tummala proposed a global R&D and manufacturing ecosystem where R&D, the supply chain for materials and tools, automotive components, and device, components and substrates all come together to enable the system integration required by automotive OEMs for NAE vehicles. He described the unique nature of Georgia Tech’s current industry consortium which combines competencies from all over the world in materials, tools, substrates, assembly, and technology users. The development strategy for NAE system integration at Georgia Tech starts with WLP technology, which leads to development of FOWLP. This will be extended to panel-level fan-out processing using laminate substrates, which will lead to development of panel fan-out technology on glass substrates. Georgia Tech is located in Atlanta, which is in a burgeoning ‘Automotive Alley’ of the Southeastern US, home to a host of automotive manufacturers like Ford, GM, Honda, Kia, Mercedes, Nissan, Toyota and Volkswagen.

Acknowledgement

Integration of the IMAPS GBC plenary SiP session within the DPC was reported as a major success by all chairs, speakers and attendees interviewed. Over 200 people attended the session, and most stayed through the full morning program and networked with speakers after the event. IMAPS will send out the GBC presentations to attendees. IMAPS intends to integrate an impactful GBC plenary session with next year’s DPC and also plans to include GBC keynote speakers for the morning of Oct 12th at the IMAPS 2016 Symposium in Pasadena, CA. Finally, we express appreciation to GBC sponsors Amkor Technology, ASE Group, Namics, SPTS and Shenmao Technology; and GBC chair Lee Smith (UTAC Group) and Co-chair Rich Rice (ASE).

Thomas Goodman is President of Izinus Technologies, a firm specializing in technology commercialization and business development. Goodman has over 30 years of experience in the development of new technologies and markets in microelectronics and advanced packaging, with special expertise in Japan and Asia. He holds several US patents in the area of advanced packaging and an MS degree in Macromolecular Science and Engineering from Case Western Reserve University. He may be contacted at tgoodman@izinus.com.
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Ken Kuang was the featured speaker at the March San Diego Chapter Luncheon.

Title of Presentation: How to Start Up and Grow Your Microelectronics and Packaging Business

Presenter: Ken Kuang, CEO Torrey Hills Technology

Abstract: Nine out of ten startups will fail. This is a hard and bleak truth. For high-tech startups, the survival rate is even lower. Most startup failures were due to lack of revenue. From his humble childhood selling fish to passers-by in China to accepting the 2013 Tibbetts Award at the White House for small business excellence, Ken Kuang’s inspiring story and insightful tips will empower you to take your business to the next level. No matter what role you are in, this talk provides stimulating ideas, useful strategies, and winning tactics for businesses of all sizes.

• Companies should have capability and ideology
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• Innovate beyond electronics
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The Microelectronics Foundation sponsors Student Paper Competitions in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Students submitting their work and identifying that “Yes, I’m a full-time student” on the abstract submission form, will automatically be considered for these competitions. The review committee will evaluate all student papers/posters and award a total of $1,000 to winning student(s). The selected student(s) must attend the event to present his or her work and receive the award. For more information on the student competition, go to www.microelectronicsfoundation.org.
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Ann Bell, Manager, Managing Editor, Advancing Microelectronics, (703) 860-5770, abell@imaps.org, Public Relations, Marketing, Fundraising, Advertising

Brianne Lamm, Membership & Events Manager, (919) 293-5000, blamm@imaps.org, Member Relations and Services Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support

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<td>MAY</td>
<td>5-10-16</td>
<td>5-12-16</td>
<td>International Conference on High Temperature Electronics (HiTEC 2016)</td>
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<td>10-25-16</td>
<td>10-27-16</td>
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<td>Los Gatos, California</td>
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