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On the Cover:
Microstructures resulting from a 400°C anneal for the (a) 2µm x 40µm TSV, (b) 5µm x 50µm TSV, and the (c) 10µm x 55µm TSV. Orientation with respect to the axial direction.

(a) Orientation map for 2µm x 40µm TSV. (b) Average peak width (°) for the i.) 2µm x 40µm TSV, ii.) 5µm x 50µm TSV, and the iii.) 10µm x 55µm TSV, all after annealing to 400°C.

(a) CDF plot of simulated grain size distribution throughout the whole TSV. Cross-section of simulated TSVs for the (b) 2µm and (c) 5µm diameters.
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In the electronics industry there has been a focus on the move towards 3D packaging. In this issue of Advancing Microelectronics, 3D packaging is the primary focus. We have some great authors who cover topics on 3D interconnect and 3D stacking, as well as the IMAPS conference that is focused on 3D packaging and what was discussed at that conference.

3D die stacking and TSV interconnect are standard methods used in manufacturing. Although these approaches are being commonly used, new integration methods are still being examined for upcoming and new package designs. One approach that was examined in the article “Heterogeneous Integration with High-Performance and Scalable Substrates: Si-IF (Silicon Interconnect Fabric) and FlexTrate™” is heterogeneous integration. This is being studied as an approach to be used on flexible substrates by using wafer-level fan-out. In this article three examples are presented where this technology is being used, such as 3DIC, Si-IF and FlexTrate™. By using this approach, the footprint/power can be reduced and new functionality can be provided.

Similar to the last article, 3DIC is discussed in the article “Scaling Effect of Through-Silicon Via (TSV) on Stress and Reliability for 3D Interconnects.” In this article through-silicon vias (TSVs) for 3D interconnects are studied. TSVs can be a reliability risk due to the coefficient of thermal expansion (CTE) which can lead to stresses and reliability risks. As more and more TSVs are being used the reliability risks continue to increase; although several processes have been used to mitigate these reliability risks, not all have been successful. In this article these effects and risks of increasing the number of TSVs with X-ray microdiffraction and microstructure data where studied. Comparing TSV to TGV (through-glass vias) was also investigated in this article. It was seen that TGV may improve the CTE mismatch but may have similar particle microstructures that can cause reliability risks.

In the last article, the 3D ASIP Conference is discussed which is one of the largest conferences focused on 3D technologies. At the 3D ASIP conference, author Herb Reiter experienced all the improvements that are being made regarding 3DIC from assembly houses and equipment vendors to the material side as well. Herb highlights several important talks that took place at this conference which included topics such as interconnect challenges, electronic design automation, 2.5/3D design challenges, and many others.

Based on the three articles in this issue it is obvious 3D interconnect is becoming a growing concern in the area of 3D packaging. TSV technology, die stacking, the new upcoming challenges with 3D and ideas for advanced technology were the focus for this issue.

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From One Engineer To Another®
Heterogeneous Integration with High-Performance and Scalable Substrates: Si-IF (Silicon Interconnect Fabric) and FlexTrate™

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Recent 3DIC Trends

3D stacking of dies especially stacked memory has been proliferating slowly and steadily over the last few years and revenue is expected to top a billion dollars within the next few years [1]. The primary barriers to further proliferation are cost and thermal considerations.

TSV-stacked memory manufacturers have mainly taken two approaches: face-to-back and face-to-face embodiments [2] [3]. The face-to-back embodiment is used in both the Hybrid Memory Cube (HMC) [4] and High Bandwidth Memory (HBM) [5], where relatively low-power dies such as DRAM can be stacked in layers. As shown in Figure 1(a), the disadvantage is that all connections need to go through TSVs. Signals and power for the lowest die closest to the organic packages (organic substrates) connect similarly to a 2D connection. However, signals from upper strata need to thread through TSVs even to reach adjacent layers. The face-to-back structure is useful when many dies need to be stacked. Since the number of interconnects between the stacked memories and the processor is large, a Si interposer with high-density interconnects is usually employed.

On the other hand, face-to-face embodiment is preferred when we need a very high bandwidth and low latency between two dies – such as a processor and cache. All signals and power from the organic packages must be delivered through TSVs as shown in Figure 1(b). However, inter-die connections are through fine-pitch microbumps. This reduces the latency and increases the bandwidth between the two dies. The face-to-face embodiment is limited to two-die stacking only and is preferred when one die is a high-power die and when the low inter-die latency and high bandwidth are desired, e.g., processor-on-cache memory stacking. The stacked dies are packaged in the organic substrate and assembled on a conventional printed circuit board (PCB).

CoWoS (Chip-on-Wafer-on-Substrate) produces significant scaling, power, and performance benefits by integrating multiple active dies on a full-thickness Si interposer wafers with via-middle TSVs in a face-down configuration. The 2.5D Si interposer is then processed to reveal the TSVs and form C4 bumps for connecting to organic packages. CoWoS is used for the programmable logic device integration of Virtex-72000T (Xilinx) FPGA (field-programmable gate array) [6].

Abstract

Holistic system scaling and integration is the next frontier of Moore’s law scaling. Here, we describe the recent trend of 3DIC stacking one component of this approach, and then, introduce the heterogeneous integration approach being developed at UCLA. In the CHIPS consortium, we scale the system by eliminating the package and integrating bare dies directly on Si substrates we call the Silicon Interconnect Fabric (Si-IF). Finally, we describe a novel method for the new flexible device integration FlexTrate™ to integrate heterogeneous dielets on flexible substrates with high-density interconnects by adapting Wafer-Level Fan-Out to flexible substrates.
The progress of CMOS image sensors (CISs) is divided into two categories: TSV-based and TSV-less stacking. As shown in Figure 2 (a)-(c), CISs are typically fabricated by stacking a pixel array circuit on a logic die. The dies are joined by advanced wafer bonding technologies. Figure 2 (a), (b), and (c) shows the cross-sectional structures of CISs stacked by fine-pitch solder microbump bonding with TSVs [7] or without TSVs [8], oxide-oxide direct bonding followed by TSV formation [9], and Cu-Cu hybrid bonding [10], respectively. High-density solder microbumps with a pitch of 5 mm have been reported [7]. However, fine-pitch solder microbump bonding potentially has yield concerns due to solder extrusion which can possibly short the adjacent connections [11] or reliability issues such as brittle intermetallic compounds which pose micro cracking and/or delamination during cyclic temperature loading [12]. Although direct bonding and hybrid bonding have been thought to be challenging because of the difficulty to control particle-free planar surfaces and high-cost CMP (chemical mechanical polishing) techniques, these technologies are advantageous to scaling, and most recently, they are used on an industrial scale, for example, oxide-oxide bonding with TSVs for iPhone 7 Plus CIS [9] and Cu-Cu hybrid bonding without TSVs for Samsung Galaxy S7 CIS [10]. In the former oxide-oxide bonding, the TSVs with a pitch of 2 mm or less have been formed through extremely thin Si [9]. In the latter Cu-Cu bonding, the pitches are getting finer down to 4 mm or less [13]. The latter technology without TSVs has a great advantage in reducing keep out zone (KOZ), compared to the former one [13]. However, almost all the stacked CISs except for several TSV-based CISs [7][14] need to be assembled on conventional organic packages through bonding wires. Tohoku University has presented a high-speed and highly parallel 3D image processing system (10,000 frames/s and 2M pixel resolution) with three layers consisting of pixel array, correlated double sampling (CDS), and ADC, which are connected with via-last TSVs to each other and assembled on a Si interposer with TSVs in a face-up configuration [14].

Today, wafer-to-wafer 3D integration [15] is industrially used only for two-wafer stacking such as the CIS on logic. From the point of views of production throughput and yield, die-to-wafer 3D integration is expected due to the use of KGDs (known good dies) and wafer-level processing [16]. However, die-to-die 3D integration is still employed due to the serious tradeoff between assembly throughput and alignment accuracy of dies. To address this issue, massively parallel assembly technologies such as capillary self-assembly driven by liquid surface tension have been developed [17].

CHIPS Project in UCLA

Design costs and time-to-market of SoCs (Systems on a Chip) have been escalating, while simultaneously the manufacturing cost benefits of classical CMOS scaling are saturating. On the other hand, computing models are becoming more heterogeneous and both deep learning and brain inspired “cognitive” computing are gaining importance. Parallel communication through the 3D networks of neurons used as signal paths like interconnects are critical to achieve efficient brain inspired computing. However, it is unlikely that we can just scale the human brain out of the huge gap beyond the three orders of magnitude in power and interconnect density. The methodology of 3DIC stacking is a promising candidate to solve the CMOS scaling issue and enable the parallel signal processing using 3D structure like the human brain [18][19].

Furthermore, the advent of the Internet of Things (IoT) also drives low power and low cost heterogeneous integration. As mentioned above, 3DIC stacking is not limited to homogeneous integration such as multiple DRAM stacking. Separately manufactured dies and components can be highly integrated to provide enhanced functionality and improved system operating characteristics. The Center for Heterogeneous Integration and Performance Scaling (CHIPS) aims to drive a much more holistic system-level integration and packaging [2][3]. The immense cost of semiconductor development and manufacturing, together with the saturation in cost-power-performance metrics, has led to a consolidation of semiconductor fabrication into mega foundries. Even more far-reaching is a similar consolidation in the chip-design area. Computing paradigms are evolving as systems become more data centric and heterogeneous. This calls for a fundamental re-thinking of IC design and manufacture. Here, we introduce the concept/strategy and key technologies of CHIPS. CHIPS is an interdisciplinary university-led consortium composed of industrial partners, universities and government agencies to holistically address the performance/scaling problem. We start from the application space, and work on development of the design environment, the integration scheme, and new materials/components will be developed. These include energy sources,
memory, sensors, passives, MEMS, and medical: all need to be integrated in the new application spaces. CHIPS is developing new methodologies and infrastructure for integrating hardened IP silicon “dielets” at fine pitches comparable to on-chip wiring levels, enabling both latencies and bandwidth comparable to on-chip values. We believe this paradigm shift will change the way to integrate systems and deliver new products significantly faster with a reduced cost.

In the CHIPS scenario, organic PCB boards are replaced by Si interconnect fabric (Si-IF) on which large numbers of heterogeneous dielets are intimately integrated electrically and in two dimensions as shown in Figure 3. The dielets could also be 3D stacks. The final wiring level will be 2-10µm pitch, and the chips communicate with each other as if they are on the same piece of silicon. Si-IFs go beyond interposers. Si interposers don’t eliminate organic packages, but add an additional level of packaging and complexity. As shown in Figure 4, Si technology in wafer-level processing has scaled by about a factor of 1,000 since the 1970s; packaging technology in board-level processing has scaled by a mere factor of three to four during the same time frame. The fine-pitch interconnect networks can produce two to four layers on the Si-IF at a reasonable cost. High thermal conductively and toughness are needed for the Si substrates used for the Si-IFs. Compared to organic packages, high-density interconnects can be formed at a high yield using wafer-level processing, which dramatically reduces the total production cost.

One key technology is system-level partitioning of an SoC into its component modules and re-integrate them on Si-IFs. Partitioning starts from an initial system specification described as a set of functional sub-blocks interacting through communication channels. System components can be selectively customized and upgraded using a divide-and-conquer method. It is likely that there exists multiple sets of candidate dielets, which satisfy the system functionality under the power, performance, reliability, and cost constraints. The dielet assembly approach allows us to choose dielets from different technologies and nodes which can potentially lead to cost and power benefits. The holistic system is finally constructed on the Si-IF where the small dielets are assembled close together through high-density interconnects. External connection to the Si-IF may be made through connectors (for power and signal), RF and optical methods (for signal).

Another key technology is die-to-wafer bonding with fine-pitch interconnects. We introduce here the results for heterogeneous integration by direct small (2-5 mm) dielet attach to a Si-IF at fine pitch using metal-to-metal thermal compression bonding (TCB). The Si-IF is fabricated using the conventional Si-based BEOL processing with up to two levels of conventional Cu-damascene interconnects with wire pitches 2-10 mm and is terminated with Cu pillars also using a damascene process. The dielets in this study are similarly prepared but terminated in Cu pads. In some cases, both pillars and pads are capped using electro-less plated Ni/Au layers that are optional. As shown in Figure 5, 10-mm-pitch Au-Au bonding is successfully bonded with a die-to-wafer flip-chip bonder to interconnect between a 5-mm-square dielet and the host Si-IF.
FlexTrate™: a New Flexible Device Integration Based on FOWLP

In recent years, the performance expectations of flexible devices using organic semiconductors is increasing. These flexible devices will further require higher performance, scalability, and functionality. NextFlex, America’s Flexible Hybrid Electronics (FHE) Manufacturing Innovation Institute, has been established to give everyday products the power of Si ICs by combining them with new and unique printing processes and new materials. However, sheet- and panel-level processing are economical, but they are not easily scaled to finer pitches. These technologies would follow in the same footsteps as the scaling of board-level semiconductor packaging as is also shown in Figure 4. The CHIPS methodology is being applied to the unique but far-reaching problems of integrating biocompatible and flexible health-related devices.

We have developed a new flexible device integration technology based on an advanced fan-out wafer-level packaging (FOWLP) process for wearable and implantable applications. In this approach, a flexible substrate we call FlexTrate™ is used to integrate an array of small heterogeneous dielets embedded in bendable and/or stretchable materials like elastomers. Here, we employed a biocompatible Polydimethylsiloxane (PDMS). In addition, fine-pitch interconnects are formed between the dielets in wafer-level processing. Figure 6 shows a typical fabrication flow for FlexTrate™. A temporary adhesive layer was formed on a 1st Si carrier. Then, more than 600 dielets (1mm x 1mm x 0.1mm) were precisely flip-chip placed on the adhesive layer. The self-assembly technology as mentioned above can be applied in this process to enhance alignment accuracy and assembly throughput [17]. Metallization is followed by the compression soft-molding of the PDMS and the subsequent multichip transfer processes. After that, 10-µm-pitch Au wirings are fabricated on the many dielets and the surrounding PDMS with a standard lithography technique at the wafer-level. Finally, the biocompatible flexible substrate with the embedded Si dielets was debonded from another 2nd carrier.

As shown in Figure 7, we have well demonstrated the fabrication of flexible substrates that have a large array of 1-mm-square thin Si dielets embedded in the biocompatible PDMS using flexible FOWLP technologies. The high-performance and scalable flexible devices “FlexTrate™” can be highly integrated with the inorganic crystalline semiconductor devices and fine-pitch interconnections formed in/on the bendable and/or stretchable substrates. We have successfully measured the relatively low resistances of the fine-pitch Au interconnects formed on the FlexTrate™ with a curvature radius of 2.5 mm or less. Leading edge applications such as neural implanted pros-

Figure 5. Test structures for Si dielet and Si-IF for TCB.

Figure 6. A typical fabrication flow of FlexTrate™ using flexible FOWLP process with a biocompatible PDMS.

continued on page 10
thetics require the heterogeneous integration of high performance and low power logic, memory and sensors at high interconnect density that is not possible using conventional printed flexible electronics with organic semiconductor devices in roll-to-roll processing.

Figure 7. Mock-ups of FlexTrate™ with 25 by 25 100-mm-thick Si dielets embedded in PDMS.

Summary

Heterogeneous integration promises to be the next generation holistic Moore's law scaling. We have presented a variety of heterogeneous integration such as 3DIC, Si-IF, and FlexTrate™ to implement them, reduce system footprint/power, and provide new functionality.

Acknowledgement

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References

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Scaling Effect of Through-Silicon Via (TSV) on Stress and Reliability for 3D Interconnects

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Abstract
Through-silicon vias (TSVs) enable full three-dimensional integration by providing high-density vertical interconnections for improved device bandwidth and power consumption. However, TSVs pose unique reliability risks due to via extrusion, which is caused by thermal stress induced by the mismatch in the coefficients of thermal expansion (CTE) for the silicon and the copper. These effects can degrade device performance and it has been proposed that optimal post-plating annealing and shrinking via dimensions can be effective in mitigating negative stress effects for TSVs. In this paper, the scaling effect on TSV stress and reliability is investigated by examining the evolution of the copper microstructure during annealing and its effect on the plasticity and extrusion statistics for 10, 5, and 2µm-diameter TSVs. TSV stress and plasticity are correlated to the cross-sectional microstructure using synchrotron x-ray microdiffraction and electron backscatter diffraction. Annealing was found to increase scatter in the grain size distribution and in the via extrusion statistics as well as significantly increase the extrusion heights for each TSV set. These results can be traced to the elastic anisotropy of copper, as the abnormal grain growth, which increases the statistical spread in the via extrusion distributions and is controlled by the strain energy originating from the CTE mismatch. Interestingly, the results from the 2µm-diameter TSVs offer no advantages over larger TSVs, as additional annealing to 400°C was found to increase the statistical variability in grain structure and via extrusion. Since such annealing processes are required for via-middle fabrication, it seems that via reliability will continue to be a challenge as TSV scaling continues.

Key words
Extrusion, Microstructure, Reliability, Scaling, Stress, TSV

1. Introduction
As semiconductor technology continues to increase transistor density and chip bandwidth, the demand for improved performance requires the development of novel architectures with optimized packaging structures. 3D integrated circuits (3DICs) incorporating through-silicon vias (TSVs) provide a crucial technology for improving wiring density, bandwidth and package form factor and power consumption [1], [2]. However, TSVs pose reliability risks due to the mismatch in the coefficient of thermal expansion (CTE) between copper and the surrounding silicon. This CTE mismatch leads to the build-up of thermal stresses [3], resulting in via extrusion, or protrusion, as well as cracking and delamination [4]. The thermal stresses also affect the electrical performance by degrading the electron and hole mobility [5], leading to the use of keep out zones (KOZ) around the via in which devices should not be placed, reducing density and restricting chip design [12-14].

As scaling continues with an increasing number of TSVs incorporated, the stress impact on reliability raises serious concerns for 3D ICs. It has been proposed that optimal post-plating annealing can be effective in mitigating negative stress effects for vias with diameter scaling [10]. The results from one study indeed show a reduction in the average extrusion when the TSV dimensions decreased from 10x100µm to 5x50µm. However, the maximum via extrusion, or the worst case, remains approximately constant after 400°C post-plating anneal [11]. This indicates that via extrusion statistics, and thus the reliability, is not improved with scaling since the portion of the maximum extrusions which control the BEOL reliability remained about the same.

In this paper, we investigate the scaling effect on TSV stresses and reliability down to TSV diameters of 2µm. In previous studies [20-23], one or two experimental methods were used to evaluate TSV scaling effects. In this work, the experimental study of TSV scaling is extended to include measurements of copper plasticity, grain size and orientation, and TSV stress behavior in addition to via extrusion statistics. The results are combined with simulations of copper microstructure during annealing in order to trace the factors controlling via extrusion statistics. To date, we found that the microstructure evolution under thermal annealing is closely correlated to the extrusion statistics under thermal cycling [8] [16], [19]. Here the large elastic anisotropy of copper, where E111/E100 is about 3, plays an important role in the abnormal grain growth, which is driven by strain energy and affects the grain orientation and thus the plastic deformation and extrusion statistics. The effects of scaling on microstructure together with the role of elastic anisotropy on TSV extrusion reliability statistics are discussed. The implication of our findings on stress reliability for through glass vias (TGVs) will also be discussed.
II. Experimental Methods

Two sets of electroplated copper blind via arrays are investigated, one set with 2µmx40µm TSVs and another with 5µmx50µm TSVs, and a via pitch of 20µm for both. These two sample sets were fabricated with similar etching and filling processes, but the 2µmx40µm experienced a 250°C post-plating anneal for 1 hour, while the 5µm sample was annealed at 350°C for 30 minutes. A third set of TSVs from another supplier that measured 10µmx55µm, with a pitch of 40µm in the x-direction and 50µm in the y-direction was also included in the study. All three TSV types were fabricated with the via middle process. Contact atomic force microscopy (AFM) and optical profilometry were both used to measure the statistical variation of via extrusions. Samples were prepared for electron backscatter diffraction (EBSD) by mechanical polishing and focused ion beam milling to finish the via surface. In contrast, the x-ray microdiffraction measurements were performed on a cross-sectional surface that does not expose the copper via, and thus minimized the adverse effects of sample preparation on copper.

The x-ray microdiffraction was performed at beamline 12.3.2 at the Advanced Light Source, Lawrence Berkeley National Laboratory. The samples were mounted at a 45° angle from the incident beam and from the detector, and white beam (5-22 keV) scans were performed at room temperature. The resulting Laue patterns were analyzed using x-ray microdiffraction analysis software (XMAS) to extract orientation, strain, and peak data relating to plastic deformation in individual grains [24].

III. Results

A. Synchrotron X-Ray Microdiffraction

One of the basic mechanisms of extrusion is plasticity in copper grains near the top of the TSV under thermal cycling, which induces irrecoverable deformation [10]. Synchrotron x-ray microdiffraction provided a unique capability to measure plastic deformation in copper grains from the broadening of specific Laue peaks derived from geometrically necessary dislocations induced by plastic deformation [10], [25]. This technique was used to measure the plastic deformation for the 2µm and 5µm vias, as well as the 10µm vias from a different supplier which were all annealed at 400°C. The results are shown in Figures 1b-1d as of the average peak width (APW) in the TSVs. Here the APW was found to be localized in the tops of all the vias and with variations in the absolute magnitude across the via, which is due to irregularity of the grain structures, as shown in Figure 1a for the 2µm via. With an average grain size of less than 1µm, the distribution of the plasticity is more uniform for the 10µm via, and as the number of grains decreases, the APW distribution becomes more random for the 2µm vias. This APW variation is correlated to the extrusion statistics in Figure 5.

B. TSV Microstructure

The microstructures after a 400°C anneal were characterized by EBSD and typical vias are shown in Figure 2. Although the 5µm TSVs show a slight preference for the (111) orientation with respect to the via axis, the texture of the 2µm and 10µm TSVs is random. To correlate microstructure with extrusion, the statistical distribution of grain sizes for the top 5µm of each via is presented in Figure 3. Overall, the grain size distribution is bimodal for all the as-received vias with an average grain size of 0.4-

Figure 1. (a) Orientation map for 2µmx40µm TSV. (b) Average peak width (°) for the i.) 2µmx40µm TSV, ii.) 5µmx50µm TSV, and the iii.) 10µmx55µm TSV, all after annealing to 400°C.

Figure 2. Microstructures resulting from a 400°C anneal for the (a) 2µmx40µm TSV, (b) 5µmx50µm TSV, and the (c) 10µmx55µm TSV. Orientation with respect to the axial direction.

Figure 3. Cumulative distribution function (CDF) plot of grain sizes throughout the top 5µm for TSVs of different dimensions and annealing conditions.
0.6µm, with large grains due to abnormal grain growth. Even with the post-plating annealing, the grain structures in the as-received vias were not stabilized, as evidenced by the further spread of the large grain distribution after the 400°C anneal. To investigate the mechanism driving microstructure evolution, the grain growth was simulated with a Monte Carlo method using local energy minimization, based on the orientation-dependent grain boundary, strain, and interface energies. The simulated results (Figure 4) clearly confirm the bimodal distribution of the grain size, with the growth of large grains primarily due to the abnormal grain growth which is controlled by strain energy induced during annealing. Overall, the results are in good agreement with that observed by EBSD. The elastic anisotropy is significant here, as changing the grain orientation from (111) to (100) or to an intermediate twin orientation minimizes the strain energy. As a result, the strain energy promotes grains with a lower yield strength that are more susceptible to plastic deformation, which thus correlates the via extrusion statistics to the strain energy-controlled abnormal grain growth [26, 27].

C. Extrusion Statistics

Via extrusion statistics for the 2µm and 5µm TSVs are plotted in Figure 5. The 2µm and 5µm TSVs have narrow, normal distributions in the as-received case, but after a 3 hour anneal at 400°C, both samples have much higher extrusion and a larger data spread. The increases in extrusion and spread are both larger for the 2µm vias, despite having a smaller copper volume and surface area. The effect of grain structure on via extrusion statistics was investigated by comparing the number of grains in the top of a TSV versus its extrusion height (Figure 6). It is clear that annealing induced both grain growth and thermal stresses which resulted in significant extrusion. Figure 6 shows that the grain growth does not improve the extrusion magnitude or variation, consistent with Figure 5.

IV. Conclusion

In this study, a broad range of experiments have been performed to investigate the scaling effect on the stresses and extrusion reliability of copper TSVs. First, x-ray microdiffraction revealed local plasticity in the tops of the vias for all diameters, and showed its dependence on the variations in the grain structure and orientation. The microstructure data indicated that the initial post-plating anneal caused a bimodal distribution in grain sizes, and further annealing caused increased spreads for all via diameters. This trend is consistent with the via extrusion statistics observed, where the absolute values and variation in the extrusion heights increased significantly with annealing, and worse so for the 2µm TSV case. Overall, these results show that scaling down TSV dimensions does not improve the stress and reliability behavior, particularly when annealed at 400°C. Since such annealing
processes are required for via-middle fabrication, we expect that TSV reliability will continue to be a challenge as scaling continues. Furthermore, the results indicate that the grain structure is not well-controlled and has high variability in grain size and orientation due to the high anisotropy of copper. This leads to large deviations in the TSV extrusion, stress, and plasticity, which negatively affects the reliability due to the worst cases on the tail end of the statistical distributions which determine the BEOL reliability.

For TGVs, the CTE mismatch is significantly less, which reduces the overall strain energy. A simulation of this case shows a threefold increase in the (111)/(100) orientation ratio but with a grain size distribution similar to the TSV. TGVs may improve particular microstructure and stress characteristics, but the anisotropy of copper will continue to create high variability, making the reliability difficult to control. Further results for TSV stress and reliability will be reported.

Acknowledgment

The authors would like to thank SEMATECH and SK Hynix, Inc. for providing samples and Dr. Nobumichi Tamura for supporting the microdiffraction experiments. The Advanced Light Source is supported by the Director, Office of Science, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

References

The 3D Architectures for Semiconductor Integration and Packaging (3D ASIP) conference is one of the biggest (if not THE biggest) event focused exclusively on the 3D IC family of technologies. The December 2016 event was held even closer to San Francisco airport than in previous years. From the lobby of the SFO Marriott Hotel, we could see planes taking off and landing. Every smooth touch-down and elegant take-off confirmed how advanced airliners serve today's travel needs.

Yes, it took about 100 years to progress from the Wright brothers' first flight to today's state of the art. Likewise, the automotive industry also took ~100 years to advance from Ford's Model-T to today's luxury sedans and SUVs.

How did Boeing, Airbus, GM, Ford and many other system manufacturers reach today's state of the art? They realized that the integrated device maker (IDM) model's limitations hamper both technical progress and profitability. They formed partnerships and structured supply chains to focus development expertise and leverage economies of scale.

The semiconductor industry came to the same conclusion in the 1980s and has had to make many changes in the last 30+ years to disintegrate most big IDMs into fabless IC vendors, foundries, and assembly houses as well as EDA vendors and soft/hard IP suppliers. They also had to define new business models as well as sign-off criteria between these companies.

I had opportunities to contribute to process design kit (PDK) developments, TSMC's design reference flows, and the roll-out of several ARM IP cores. I saw first-hand how these three offerings enabled IC designers to quickly simulate their ideas and present them to management for project approval, design, and release to manufacturing.

At 3D ASIP 2016 I really enjoyed hearing about the impressive progress assembly houses, equipment vendors, and material suppliers have made. In addition, I was really surprised by how widely wafer stacking is used in image sensor manufacturing for a broad range of digital cameras.

However, I was expecting to see more IC and system vendors – the actual 3D-IC customers – at the conference. Also, I missed the enthusiastic discussions between suppliers and customers common in the GSA's 3D Working Group meetings I organized from early 2008 until the end of 2011.

Please, don't misunderstand, 3D ASIP 2016 was a well-organized and very informative conference, in a convenient location, with excellent speakers outlining their capabilities and investments to cost-reduce their products. I counted 37 manufacturing and product centric presentations and, including my own, three design-centric messages. This ratio indicates that the bridge comprising EDA design flows, assembly design kits (ADKs), and die-level IP between the many experienced 2.5/3D-IC manufacturers and potential customers is still very narrow.

Based on my experience with rolling out FPGAs, bipolar and CMOS gate arrays, cell-based ICs, and SOI technology, I am convinced that we need to complement the large investments already made in 2.5/3D IC manufacturing and wafer-level packaging with much smaller amounts of money allocated to the development of ADKs, reference design flows and die-level IP building blocks. Only then will we enable a broad range of customers to start many more 2.5/3D/WLP designs, secure returns on the large investments already made, and quickly recapture the relatively small investments still to be made.

Enough said about my objective to bridge the gap between EDA and manufacturing ASICs and other ICs. Let me highlight now some of the many excellent presentations.

A very prominent IC vendor, Qualcomm, was represented by Yang Du from their research department. He conveyed why our two-dimensional SoCs will not be able to meet future performance and power requirements. Du also stated that – from his perspective – sequential 3D processing (also called monolithic, like 3D NANDs and Leti's CoolCubes are using) and direct bonding (like DBI, Invensas offer) are the most important technologies for the success of 3D ICs.
Leti’s Pascal Vivet, chair of the design session, gave me the opportunity to be his first speaker. I, of course, tried to convey my concerns outlined earlier and explicitly asked the many manufacturing experts in the audience to work closer with EDA vendors (represented by Mentor’s Juan Rey, Cadence’s Brandon Wang and half of myself—I’m other half is solidly in the manufacturing camp). I encouraged both sides to work together on ADKs and design flows because I have seen how these two capabilities contributed to making TSMC’s wafer fabs successful.

By presenting Figure 2, I re-emphasized that IC and system designers need EDA tools, and accurate inputs from manufacturing, to walk the fine line between costly over-design and unreliable under-design, earn project approval and funding, then get their designs to manufacturing on schedule.
Juan Ray focused his 3D ASIP presentation on how Mentor Graphics addresses general 2.5/3D design challenges, like chip and package co-design. He suggested expanding the current PDKs with package and assembly information to meet the die-package co-design requirements. Ray also talked about parasitic extraction and verification with “Calibre 3D,” outlined “Sahara’s” thermal analysis capabilities, how to analyze stress effects with “Glacier” and how Mentor and Leti are working together to address EM challenges in TSVs, RDLs, and wafer-to-wafer bonding.

Denis Dutoit described Leti’s vision for how system designers can use “chiplets” (die-level IP building blocks, also called “dielets”) to quickly assemble complex subsystems on active or passive interposers. To demonstrate how powerful this concept is, Dutoit described their design steps for a 3DNoC. He also showed some of Leti’s contributions to the European ExaNoDe (Exascale Processor & Memory Node Design) and talked about the power of photonic interconnects as well as Leti’s work on multi-die IC design flows with EDA partners.

Prof. Subramanian Iyer outlined his work at UCLA’s “CHIPS” (Center for Heterogeneous Integration and Performance Scaling). “Dielets,” manufactured in the technically most suitable and lowest cost process technology when combined on an interposer, minimize form factor, interconnect delays and power. Based on his many years of experience at IBM managing ultra-complex high-performance chip designs, Iyer shared his vision of how die-level integration of heterogeneous functions will impact electronic system design in the future. The key objectives of the CHIPS program are outlined in Figure 3.

Among the many other great presentations, the very visionary message from ASE’s Bill Chen really impressed me. His Keynote was about the new Heterogeneous Integration Roadmap (HIR). After many years of contributing to the now-discontinued International Technology Roadmap for Semiconductors (ITRS), Chen reasoned how the increasing risks and cost of continued shrinking and the growing market demand for integration of heterogeneous functions, suggested replacing the ITRS efforts with the newly formed HIR team.

Also, the presentations of John Hunt and Rich Rice showed that ASE is fully prepared to offer customers advanced packaging technologies to add value and differentiation to their ICs and (sub)systems.

Mike Kelly presented a very good overview of Amkor’s current capabilities and plans. Figure 4 shows how multi-faceted today’s IC packaging requirements are and how much room for further innovation advanced packaging technologies offer. FYI, Amkor and Cadence announced in May 2016, that they are working together on a “Package Assembly Design Kit” for Amkor’s SLIM and SWIFT packages, to enable die-package co-design. This will make it easier for designers to meet performance and cost goals with Amkor’s wafer-level packages.
SPIL, now part of the same corporate umbrella as ASE, was represented by Albert Lan. He focused on outlining the importance of fan-out wafer level packaging (FOwLP) for mobile and wearable applications. Lan contrasted high-performance versus wearable packaging requirement, outlined SPIL’s manufacturing flows and explained why panel-level processing of these packages will become the most cost-effective manufacturing technology.

After enjoying Prof. Iyer’s CHIPS message, I was very glad to see that Deca Technologies is developing manufacturing processes to quickly and accurately place heterogeneous dielets in close proximity to each other on interposers. Tim Olsen explained how multi-die FOwLP, assembled with Deca’s processes, will enable system-level integration in thin and cost-effective FOwLP.

Figure 5 shows how Deca expects to enable side-by-side integration of dies. It also points out that different functions may benefit from scaling at very different rates.

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Figure 4

Figure 5

continued on page 20
So far I have only covered a fraction of all the interesting and useful messages conveyed at 3D ASIP 2016. Considering that this is already getting too long, here are quick summaries of other groups of presentations:

Digital cameras for smartphone and feature phones are the highest volume application for 3D ICs, serving as backlit image sensors. ams, Forza Silicon, ON Semi/Aptina, Raytheon, SMIC and SONY shared their accomplishments in this space.

Yole confirmed that memory cubes comprising vertically stacked dies are now the most widely used die-level IP building blocks. Tezzaron described its 4th generation memory cubes. eSilicon presented its design service capabilities and mentioned that it has already implemented more than half a dozen customer designs with HBM cubes on different interposers.

Boeing, Northrop Grumman and Teledyne, vendors to the military and aerospace segment, described how they used multi-die ICs and compound semiconductors to meet very stringent requirements.

Professors from UCSB and Ohio State talked about their research in multi-die IC technologies.

Arotech, AMAT, Besi, Corning, Brewer Science, EV Group, Samtech, SPTS, Suss MicroTec and Unimicron presented their equipment or materials capabilities and described how they contribute to the success of multi-die ICs.

Last, but certainly not least, this 3D ASIP conference also offered two tutorials. Qualcomm’s Beth Keser shared her vast expertise in FOWLP with a large audience. Prof. Bruce Kim from the City University of New York presented Electrical Modeling and Test Strategies for 3D Packages to a much smaller group, which I joined. This is another data point demonstrating the imbalance between manufacturing and design that we need to work on for 3D ASIP 2017.

Special thanks to IMAPS, who took over management of this conference from RTI, the technical organizers and session chairs of this important and informative conference. Learn more about it at http://3dasip.org/. Here’s to success in 2017.

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Symposium Technical Chair
Dr. Parshant Kumar, Draper

Preliminary Program
Keynote Lunch Speaker: Dr Livia Racz, MIT Lincoln Laboratory
“From Interconnect to Innovation in the DoD”

Sessions
RF and Microwave - Innovations and Emerging Technologies
Chairs: Tom Terlizzi, GM Systems & Dr. Chandra Gupta, Consultant
MEMS and Nano Systems
Chairs: Robert White, Tufts University & Rick Morrison, Draper
Thermal Management
Chair: Dave Saums, DS&A
Printed Electronics
Chair: Katherine Duncan, Printed Structures Group, CERDEC
Medical Device Packaging
Chairs: Caroline Bjune, Draper & Steve LaFerriere, YOLE Development
Nanoelectronics and Optoelectronics Packaging
Chair: Yi Qian, MRSI
Poster Session
Chair: Dr. Rita Mohanty

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Scenes from Device Packaging

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INDUSTRY NEWS

DYCONEX Puts Its Fourth IST Testing Machine into Service

Bassersdorf, February 07, 2017 – DYCONEX AG, a MST company and the world’s leading supplier of highly complex solutions in the area of electronic interconnect technology, recently put its fourth IST (interconnect stress test) testing machine into service and in doing so further upgraded its Center of Competence for Product Reliability.

Back in December 2014 DYCONEX opened its new laboratory for reliability testing and expanded its Center of Competence. “With our four IST testing machines at just one location, we are the leaders in all of Europe,” notes Dr. Hans-Peter Klein, Director of Quality Management at DYCONEX.

Critical applications in medical technology as well as in aeronautics and space flight cannot tolerate any compromises whatsoever when it comes to reliability. To meet these needs, DYCONEX has developed extensive and systematic methodologies that make it possible to gather solid evidence about product reliability. Towards this goal, the firm employs accelerated test methods such as the interconnect stress test. In IST tests, special test coupons that include vias are subjected to temperature cycles, after which they are measured for possible changes in resistance within the test coupon. Any corresponding increase in resistance is indicative of damage.

IST tests enhanced by additional testing schemes and analytic methods form the basis for guaranteed, measurable reliability of DYCONEX products.

About DYCONEX AG:
With more than 50 years of experience, DYCONEX AG is an international leader in the supply of highly complex, flexible, rigid-flex and rigid HDI/microvia circuit boards and chip-substrate solutions. These products are used in every application where miniaturization, increased functionality, quality and the highest level of reliability play a role.

With its headquarters in Bassersdorf, DYCONEX today has 180 employees and the company is a member of the Micro Systems Technologies Group.

About the Micro Systems Technologies Group:
The Micro Systems Technologies Group consists of four high-tech companies that offer innovative components and services for medical devices, in particular implants. Other high-tech industries that demand exceptional performance, quality and the highest levels of reliability also rely on the expertise of MST companies.

The globally active companies that make up the MST Group – DYCONEX AG (Switzerland), LITRONIK Batterietechnologie GmbH (Germany), Micro Systems Engineering GmbH (Germany) and Micro Systems Engineering, Inc. (USA) – offer their customers integrated solutions ranging from initial design through to series production.

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Master Bond EP3HTND-2Med Black is a high strength, fast curing epoxy for use in the assembly of medical devices. It fully meets USP Class VI specifications. This one-part system delivers superior resistance to a variety of sterilization methods such as chemical sterilants, Eto, radiation and especially autoclaving.

As a one-component system, EP3HTND-2Med Black does not require any mixing and essentially has an unlimited working life at room temperature. This epoxy has a paste consistency and is formulated not to flow while curing. It cures within minutes when heated at 250-300°F. The higher the temperature, the faster the cure speed. Also, it has low shrinkage upon curing.

This system bonds well to a wide variety of substrates including glass, metals, ceramics and most plastics. EP3HTND-2Med Black features a tensile strength of 5,000-6,000 psi and a tensile lap shear strength of 1,600-1,800 psi at room temperature. It is a competent electrical
insulator with a volume resistivity exceeding 10^{14} \text{ohm-cm}. The service temperature range of this compound is -60°F to +400°F [-51°C to +204°C]. EP3HTND-2Med Black is available in 1/2 pints, pints, quarts, gallons and 5 gallon containers as well as syringes. This epoxy has a 6 month shelf life when stored at room temperature in its original, unopened containers.


Applications in Research Labs and Commercial Use for EP21TCHT-1

Master Bond EP21TCHT-1 is a two-component, thixotropic paste that features thermal conductivity and electrical insulation properties. This heat resistant epoxy is serviceable over the temperature range of 4K to +400°F and maintains its properties under cryogenic conditions. It passes NASA low outgassing testing making it suitable for use in vacuum environments. Multiple research institutions, such as University of Florida, Princeton University and NASA, among others have used EP21TCHT-1 in their demanding applications.


Room Temperature Curing Epoxy Features Low Thermal Resistance

Formulated for use in demanding thermal management applications, Master Bond EP30TC is a two-component epoxy that contains a robust thermally conductive filler with very fine particle sizes. This NASA low outgassing certified system can be used for bonding, coating, sealing and encapsulating for the aerospace, electronic, optical and OEM industries.

EP30TC exhibits a thermal conductivity of 18-20 BTU•in-ft/2-hr•°F [2.60-2.88 W/(m•K)] and has the ability to be applied in sections as thin as 5-15 microns, resulting in a low thermal resistance of 7-10 x 10^{-6} K•m2/W. This compound is a reliable electrical insulator and has a volume resistivity of over 10^{14} \text{ohm-cm}. It is serviceable over the wide temperature range of -100°F to +300°F [-73°C to +149°C].

EP30TC features a low viscosity with excellent flow properties making it well suited for coating and potting applications. As a two part system, it requires a 10 to 1 mix ratio by weight. Color coding facilitates mixing with Part A being gray and Part B being clear. It can be cured at room or elevated temperatures, but to achieve optimum properties, the recommended cure schedule is overnight at ambient temperature followed by 2 to 3 hours at 150-200°F.

This system bonds well to metals, composites, ceramics, glass and many plastics. It delivers superior physical strength properties, with a tensile strength of 5,000-6,000 psi, a compressive strength of 24,000-26,000 psi and a tensile modulus of 500,000-550,000 psi. Dimensionally stable, EP30TC also has very low shrinkage upon curing and a low coefficient of thermal expansion.

This product is available for use in 1/2 pint, pint, quart, gallon and 5 gallon container kits, as well as in pre-mixed and frozen syringes.

For more information, see http://www.masterbond.com/tds/ep30tc

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SHENMAO America, Inc. Introduces Omega Aleaciones S.A. de C.V., the Exclusive Mexico Distributor of SHENMAO Solder Paste and Flux

March 2017 — Omega Aleaciones S.V. Sales and Application Engineering Team reinforces SHENMAO’s commitment to providing its worldwide EMS and OEM customers with the highest quality and technical solutions solder paste to meet the challenges of today’s SMT assembly and product reliability throughout Mexico.

Three Omega Aleaciones Sales, Service and Application Engineering Staff successfully completed Product Application Training at SHENMAO Technology, Inc. Headquarters in Taiwan.

With 11 of the 12 largest EMS companies as its customers, SHENMAO Technology, Inc. of TaoYuan City 328, Taiwan, is a global leader of superior solder materials with 10 manufacturing, technical and sales support facilities located around the world. SHENMAO America, Inc., the American subsidiary, manufactures solder paste in San Jose, CA, U.S.A., supporting a wide range of products for the PCBA and Semiconductor Industries, complemented from multiple locations in Mexico by exclusive distributor Omega Aleaciones S. A. de C. V.’s own products of wave solder bar, cored solder wire, flux and a collection of solder dross.

As the world’s major solder materials provider for 44 years, SHENMAO produces SMT solder paste, laser soldering paste, wave solder bar, solder wire and flux, solder preforms, semiconductor packaging solder spheres, wafer bumping solder paste, dipping flux, LED die bonding solder paste and PV ribbon.

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SST Vacuum Reflow Systems Introduces Model 518 Vacuum/Pressure Furnace


The new Model 518 rounds out SST’s range of radiant heated vacuum/pressure reflow furnaces. Positioned between the existing Model 1200 table top and Model 5100 production level furnaces, the 518 provides the right combination of features and value to create void-free, flux-free microelectronics packages.

Precision applications of vacuum, pressure, temperature and force create these microelectronics packages with high yields, fast production cycles and repeatable processes. Model 518 is at home in R&D labs as well as in high mix/low volume production facilities.

Graphite tooling and heating elements provide unmatched temperature uniformity and precise control over the heating and cooling cycles during production runs.

This single chamber batch furnace is full featured, but is available with numerous options to enhance performance and increase its flexibility.

As with all SST Systems, Model 518 is supported by SST’s Total Process Solution™, providing process development, recipes, tooling, and training to ensure your system is productive the day it is installed.

For over 50 years, SST Vacuum Reflow Systems has been designing and crafting the systems and processes needed to create void-free, flux-free microelectronics packages and high vacuum hermetically sealed packages. Its global customer base is serviced from Downey, California, USA, where all systems are created and assembled.
For more information, please contact SST Vacuum Reflow System at 562-803-3361
email sales@sstinternational.com
A.J. Wilson, President, sstinternational.com

TechSearch International predicts strong market growth for fan-in wafer level packages (WLPs) and fan-out WLP (FO-WLP). Driven by demand for thin, low-profile packages in smartphones, tablets, and wearable devices such as smart watches, fitness bands, and virtual reality headsets, fan-in WLPs are projected to have a >10% growth rate from 2015 to 2020. Starting from shipments of a few hundred million packages in 2015, FO-WLP shows a staggering growth rate of 82% over the five-year period. The use of FO-WLP for RF, audio CO-DEC, and power management ICs, coupled with Apple’s adoption of TSMC’s InFO FO-WLP as the bottom package-on-package (PoP) in Apple’s iPhone 7, is driving unit volume shipments. Automotive radar, connectivity modules, and other applications promise continued growth for FO-WLPs. Cost-reduction pressures are driving the development of alternatives to reconstituted wafer FO-WLP in the form of large area panel processing and flip chip on coreless or thin core substrates. Chip package interaction (CPI) is analyzed for WLPs and flip chip.

TechSearch International’s new study, Flip Chip and WLP: Market Forecasts and Technology Analysis, provides detailed analysis of the drivers for fan-in WLP, FO-WLP, and flip chip. The detailed analysis is based on the company’s 29-year history of studying markets and critical technology and infrastructure issues.

Driven by small size devices such as filters, low noise amplifiers, power amplifiers, and switches found in smartphones, flip chip growth shows >13% CAGR in unit volume from 2015 to 2020. Documentation of the continued transition to Cu pillar is provided. Flip chip applications, bump types, and pitch trends are based on extensive interviews and research. Flip chip assembly options are discussed. Growth in gold bumping for LCD driver ICs is included. A critical analysis of planned capacity and utilization is provided for each geographic region, showing projections for strong growth in China.

The 115-page report with full references provides forecasts for the flip chip wafer bumping market by application, device type, number of wafers, and die shipments. Merchant and captive capacity is included. Forecasts for fan-in and FO-WLP demand are projected in number of die and wafer shipments. Bumping, wafer level packaging, substrate suppliers, assembly equipment, underfill material, and contract assembly service providers are listed. A set of 78 PowerPoint slides accompanies the report.

TechSearch International, Inc., founded in 1987, is a market research leader specializing in technology trends in microelectronics packaging and assembly. Multi- and single-client services encompass technology licensing, strategic planning, and market and technology analysis. TechSearch International professionals have an extensive network of more than 17,000 contacts in North America, Asia, and Europe.

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IMAPS 2017
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In Memoriam
Roger Cadenhead

Dear Fellow IMAPS Members,

It is with great sadness that I report that Roger Cadenhead passed away. Up until Roger got ill, he was an active member of the society.

Roger was one of the founders of the Central Texas Chapter and was later a driving force for the North Texas Chapter. He was responsible for the ISHM Monograph entitled “Assuring the Integrity of Multilayer Substrates Prior to Assembly,” written in 1984. Also, that year he worked with me in developing and implementing the first book on Surface Mount Technology and then helped to facilitate the SMT mini-conference that went along with the book and was held at the Loews Anatole Hotel in Dallas as part of the annual symposium.

He and I jointly presented several SMT-related papers over the years. He wrote the first “ISHM Roots” for the 25th Anniversary of the Society, a daunting task to bring together all the major activities for our Society’s first quarter century. This was published in Inside ISHM. Five years later he, along with Rene Cote, updated the history. In 2002 a wide-ranging effort was organized by Roger to develop a “Certified Microelectronics and Packaging Engineer” program. Roger received a Fellow of the Society Award in 1987.

Roger was born on May 7, 1946 in Honey Grove, Texas and passed away on February 6, 2017 in Carrolton, Texas. Roger is survived by his wife, Sherry Cadenhead; children, Roger Cadenhead Jr., Kelly Reber, Chad Cadenhead, Clint Hammer, Carrie Majors and spouses; grandchildren, Maxwell Cadenhead, Elijah Cadenhead, Samuel Cadenhead, Bryce Reber, Brody Reber, Maclane Cadenhead, Campbell Cadenhead, Cooper Cadenhead, Caleb Hammer, Micah Hammer, Jared Hammer, Jaelyn Majors; sisters, Evelyn Davis, Kathy Colgrove, Jodi Greenbaum, Stacey Shudack and spouses.

We will miss you, Rog.

Greg Caswell

Exhibit at IMAPS 2017

The 2017 show is particularly special for IMAPS, as the Society will be celebrating its 50 years of bringing together the entire microelectronics supply chain. The headquarters home of IMAPS – the Research Triangle region of North Carolina – will serve as host for this special edition of the annual symposium. The city of Raleigh and the surrounding region is home to a thriving research community, a bustling technology sector, and excellent visitor amenities.

You will find the important information your organization needs to apply for an exhibit or sponsorship at the link below. Please review the critical information from IMAPS to acquaint yourself with the sponsorship and exhibit opportunities, pricing, and the application process.

IMAPS strives to make the 2017 show better than ever for exhibitors and attendees alike. For up-to-date information on all details related to the show, visit www.IMAPS2017.org regularly.

Get the complete Exhibitor Prospectus here:

Your IMAPS Member Benefits at Your Chapter Level

Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar

Student Chapter News

Binghamton University

The IMAPS Student Chapter at Binghamton University held a workshop on February 22, 2017. Approximately 40 students attended the event, with 31 students registering to become IMAPS student members. With four speakers of varying backgrounds in electronics manufacturing, the students were exposed to a wide array of topics and disciplines. The speakers were:

1) Dr. Steven Gonya, LM-Fellow, Research Scientist, Advanced Manufacturing Technology Group, Lockheed Martin

2) Dr. Luke Jenkins, Power Hardware Engineer, IBM; Research Scientist and Teaching Assistant, Auburn University

3) Dr. Mark Poliks, Technical Director, S3IP - The Center for Advanced Microelectronics Manufacturing (CAMM), Professor of Systems Science and Industrial Engineering, Binghamton University

4) Dr. Peter Borgesen, Professor of Systems Science and Industrial Engineering, Binghamton University

Advanced Technology Workshop

The International Microelectronics Assembly and Packaging Society (IMAPS) Binghamton Student Chapter is organizing a Workshop/Networking Opportunity at Binghamton University. Come Join Us:

Engineering Building – Watson Commons
Wednesday, February 22nd from 2:30 – 4:00 PM

Presentation Topics:
1. Career Opportunities for Electronics Manufacturing
   - Dr. Steven Gonya, LM-Fellow, Research Scientist, Advanced Manufacturing Technology Group, Lockheed Martin

2. Power Architecture Design in IBM Mainframe Servers
   - Dr. Luke Jenkins, Power Hardware Engineer, IBM; Research Scientist and Teaching Assistant, Auburn University

3. Applications for Flexible and Printed Electronics
   - Dr. Mark Poliks, Technical Director, S3IP - The Center for Advanced Microelectronics Manufacturing (CAMM), Professor of Systems Science and Industrial Engineering, Binghamton University

4. Concerns for Reliability in Microelectronics Assembly and Packaging
   - Dr. Peter Borgesen, Professor of Systems Science and Industrial Engineering, Binghamton University

Invite Your Friends!
Free PIZZA will be provided!
Goal
The Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT) conference brings together a diverse set of disciplines to share experiences and promote opportunities to accelerate research, development and the application of ceramic interconnect and ceramic microsystems technologies. This international conference features ceramic technology for both microsystems and interconnect applications in a dual-track technical program. The Ceramic Interconnect track focuses on cost effective and reliable high performance ceramic interconnect products for hostile thermal and chemical environments in the automotive, aerospace, lighting, solar, defense/security, and communication industries. The Ceramic Microsystems track focuses on emerging applications and new products that exploit the ability of 3-D ceramic structures to integrate interconnect/packaging with microfluidic, optical, micro-reactor and sensing functions. Tape casting, thick film hybrid, direct write and rapid prototyping technologies are common to both tracks, with emphasis on materials, processes, prototype development, advanced design and application opportunities.

Ceramic Interconnect Track
Conventional thick and thin film ceramic technologies are being revolutionized and extended through the development of low temperature co-fired ceramics, photo patterning, and embedded passive component materials and processes. These have contributed to increased circuit density, enhanced functionality, and improved performance that are being adopted for leading edge applications in wireless and optical communications, automotive, MEMS, sensors, and energy. Data communications and the Internet are driving the demand for bandwidth, sparking demand for optical communication equipment and new interconnect and packaging applications that perform at 40 Gb/sec and beyond. In under-the-hood electronics for automotive, engine/transmission control, communications, and safety applications continue to drive the growth of ceramic interconnect technology, while collision-avoidance systems are creating interest in low loss ceramic materials for frequencies approaching 100 GHz.

Ceramic Microsystems Track
Enabled by the availability of commercial ceramic, metal and embedded passives materials systems, and the rapid prototyping capabilities of the well established multilayer ceramic interconnect technology, three dimensional (3-D) functional ceramic structures are spawning new microsystems applications in MEMS, sensors, microfluidics, bio-devices, microreactors, and metamaterials. These new devices and applications exploit the ability to integrate complex 3D features and active components (e.g., valves, pumps, switches, light pipes, and reaction chambers).

In addition, the Ceramic Microsystems track of the CICMT conference targets new developments in microsystems that include fabricating 3-D micro device structures enhanced with sol-gel, advanced printing and patterning technologies, high temperature materials technologies, and emerging applications like energy harvesting. Many of these innovative applications are taking advantage of the unique ability to integrate the thermal, chemical, mechanical and electrical properties of these multicomponent ceramic-metal systems.

Special Features
• Invited keynote and international presentations on the current status of ceramic technology and future system directions.
• A focused exhibition for suppliers who support the use of the technologies.
• A technical poster session to promote student participation.
• Social events to promote new contacts.
<table>
<thead>
<tr>
<th>Planned Session and Paper Topics Include:</th>
<th></th>
</tr>
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<tbody>
<tr>
<td><strong>Ceramic Microsystems</strong></td>
<td><strong>Ceramic Interconnect</strong></td>
</tr>
<tr>
<td><strong>Markets and Applications</strong></td>
<td><strong>Markets and Applications</strong></td>
</tr>
<tr>
<td>- MEMS Technology and Markets</td>
<td>- Automotive</td>
</tr>
<tr>
<td>- Batteries and Fuel Cells</td>
<td>- Aerospace</td>
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<td>- Biological and Medical</td>
<td>- Lighting/Solar</td>
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<td>- Chemical and Biochemical</td>
<td>- Wireless/Communication</td>
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<td>- Photonics</td>
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<td><strong>Materials and Properties</strong></td>
<td><strong>Materials and Properties/Functions</strong></td>
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<tr>
<td>- Materials Integration and Nano-materials</td>
<td>- Dielectric and Magnetic Materials</td>
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<tr>
<td>- Thermal Management and Reliability</td>
<td>- Embedded and Integrated Passives</td>
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<tr>
<td>- Piezoelectric Materials</td>
<td>- Microwave/mm Wave Characterization</td>
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<td>- Optoelectronics</td>
<td>- Zero-shrink Ceramic Systems</td>
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<tr>
<td><strong>Processing and Manufacturing</strong></td>
<td><strong>Processing and Manufacturing</strong></td>
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<tr>
<td>- MEMS Manufacturing Technology</td>
<td>- LTCC and Multilayer Ceramics</td>
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<tr>
<td>- Industrial Automation and Rapid Prototyping</td>
<td>- Roll to Roll and Continuous Manufacturing</td>
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<tr>
<td>- Nano-technology/Integration</td>
<td>- Direct Write and Drop on Demand</td>
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<tr>
<td>- High Temperature Microsystems</td>
<td>- Advanced Thick Film Processing</td>
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<tr>
<td><strong>Devices</strong></td>
<td><strong>Devices</strong></td>
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<tr>
<td>- Sensors and Actuators</td>
<td>- Fine Structuring Technologies</td>
</tr>
<tr>
<td>- Micro-reactors</td>
<td>- Circuits, Antennas, and Filters</td>
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<tr>
<td>- Fluidic Devices</td>
<td>- Embedded Structures and Components</td>
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<tr>
<td>- Biomolecular and Cell Transport Systems</td>
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<tr>
<td>- Energy Conversion Systems</td>
<td><strong>Characterization and Reliability</strong></td>
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<td><strong>Characterization and Reliability</strong></td>
<td>- Characterization of Green Tapes</td>
</tr>
<tr>
<td>- Materials and Process Characterization</td>
<td>- Life Testing, Quality Issues</td>
</tr>
<tr>
<td>- Systems Reliability, Lifetime, and Failure Estimation</td>
<td>- RF Performance</td>
</tr>
<tr>
<td>- Reliability of High-Performance Microsystems</td>
<td><strong>Design, Modeling, and Simulation</strong></td>
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<tr>
<td><strong>Design, Modeling, and Simulation</strong></td>
<td>- High Frequency Design Software</td>
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<tr>
<td>- Thermal and Heat Transfer</td>
<td>- Design Rules</td>
</tr>
<tr>
<td>- Computational Fluid Dynamics</td>
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**Integrated Ceramic Technology**

**Advanced Packaging Technology**
- Next Generation Packaging Technologies
- Packaging and Integration in BioMEMS
- Packaging Issues for MEMS Devices
- Technologies for Microsystems Components and Substrates
- Packaging Standard for Microsystems
- Environmental Issues, Lead Free Systems
- Cost Reduction

**Registration & Hotel Reservations** *(Full details will be available soon)*
- 60 min from Kansai Airport by Train
- 45 min from Kyoto by Train

www.imaps.org/ceramics
SYSTEM-IN-PACKAGE (SiP) TECHNOLOGY
Inaugural Conference and Exhibition
June 27-29, 2017 | Doubletree Sonoma Wine Country
Sonoma, California USA
www.IMAPS.org/SiP

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Simon McElreay
CEO, Semblant

Urmik Ray
Principal Engineer,
Qualcomm

Dr. Dongkai Shangguan
CMO, Stats ChipPac

SiP 2017 is the first System-in-Package (SiP) conference fully dedicated to covering all aspects related to SiPs - market trends, system integration/miniaturization, and new technology innovation enablers to meet current and future SiP challenges. This conference will bring the entire SiP supply and design chain from OEM, Fabless, IDM, OSAT, EMS, EDA, silicon foundries, and equipment and material suppliers together under one roof.

Speakers, sponsors, exhibitors and attendees will focus on the insights of SiP technology in the relaxing Sonoma wine country of California, away from big city distractions.

Featuring three full days of technical sessions, panel discussions, exhibitors and local activities, SiP 2017 will provide dynamic learning and technology updates for SiP related trends and new engineering innovations from the industry’s world SiP leaders.

Speaking and presenting opportunities are by invitation from the technical committee.

Visit
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Inaugural System in Package (SiP) Technology Conference and Exhibition
June 27-29, 2017 | Doubletree Sonoma Wine Country
Learn more at www.IMAPS.org/SiP

Technical Program Preview

June 27
SiP market overview, SiP in cellphone teardown of latest cellphones, SiP innovation challenges in mobile applications, active and passive components trends, MEMS and sensors technology trends, SiP package level conformal and compartmental shielding methods, human factor impacts on SiP, and SiP opportunity in China.

June 28
RF frontend SiP, connectivity SiP (WiFi, BT, GPS...), medical and wearable SiP, power module, analog SiP, MEMS, sensors and automotive SiP, SiP miniaturization techniques.

June 29
Embedded active and passive technology, Integrated Passive Devices (IPD), thin substrate technology, Fan-out solution OSAT and foundry perspectives, water proved Products/NanoCoating technology, assembly process improvement EMS perspective, enhanced new materials for SiP design and EDA tools, EMI shielding equipment.

Sponsorship and Exhibition Opportunities
Limited event sponsorship opportunities are available and won’t last long. Contact Brian Schieman at bschieman@imaps.org to secure your organization’s sponsorship for SiP 2017 before they are filled.

A tabletop exhibition will be held in conjunction with the technical program on June 27th and 28th.

Visit www.IMAPS.org/SiP for conference updates, including the technical program, attendee and exhibitor registration, deadlines, and more. Contact IMAPS HQ to sponsor SiP 2017 or if you have any questions.
Start Searching!

IMAPS members have preferred access to thousands of digital documents and research papers from IMAPS publications, conferences and workshops—all exclusive content focused on the advanced microelectronics packaging industry.

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Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!
International Conference and Exhibition on
High Temperature Electronics Network (HiTEN 2017)

July 10-12, 2017
Queen’s College | Cambridge, United Kingdom

Conference Chairs:

<table>
<thead>
<tr>
<th>Colin Johnston</th>
<th>R. Wayne Johnson</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxford University</td>
<td>Tennessee Tech University</td>
</tr>
<tr>
<td><a href="mailto:colin.johnston@materials.ox.ac.uk">colin.johnston@materials.ox.ac.uk</a></td>
<td><a href="mailto:wjohnson@tntech.edu">wjohnson@tntech.edu</a></td>
</tr>
</tbody>
</table>

HiTEN Conference Focus:
The objective of the HiTEN Conference is to have a unique forum that brings together researchers and practitioners in academia and industry from all over the world. All styles of practical high temperature electronics design and implementation approaches are encouraged, along with a variety of high temperature application areas. Today the main semiconductor focus of HiTEN is silicon and silicon on insulator (SOI). Although, HiTEN is not simply a semiconductor-focused network, HiTEN provides a conduit for the exchange and dissemination of information on all aspects of high temperature electronics. It is a global network with users, suppliers, developers and fundamental researchers dealing in all aspects of High Temperature Electronics.

- Applications in the Aerospace, Automotive, Oil and Gas, and Geothermal industries
- Devices and applications
- Novel devices
- ASICs for high temperature applications
- Memories
- Passive components
- Power devices
- Semiconductor materials
- Contacts and metallizations
- Materials
- Packaging and interconnects
- Sealants, adhesives, solders
- Reliability and failure mechanisms
- Lifetime predictions
- Accelerated life testing
- Testing at high temperatures

The HiTEN Proceedings papers will be ARCHIVED into IMAPS’ new online research portal/library, IMAPSource® - www.imapsource.org. IMAPSource® currently features all IMAPS proceedings, journal papers, magazines, and other conference publications back to 2010. This portal is a fully searchable, user and Google Scholar-friendly database. The software allows for fully exportable citations, improved keyword and Boolean search functionality and customizable alerts, among many other features. The library is indexed by Google Scholar and many key scientific engines/indexes, and growing each day. The 2017 HiTEC papers will be added in May. For now, please visit www.imapsource.org and search. HITEN 2016 proceedings can be found at http://www.imapsource.org/toc/apap/2016/HiTEN and older HiTEC/HiTEN Proceedings can be found in our conference section: http://www.imapsource.org/loi/apap.

Accepted papers may also be considered for publication in the IMAPS Journal of Microelectronics and Electronic Packaging. For more information, please email Brian Schieman (bschieman@imaps.org).

www.imaps.org/hiten
Sponsorships Available!
www.imaps.org/hiten/HiTEN2017_Sponsorships.pdf
Join now!

IMAPS corporate memberships are designed to give your company a competitive advantage in the microelectronics packaging industry. Choose the right membership to meet your exhibition, advertising, discount registration needs and more.

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<th>Membership package inclusions</th>
<th>Premier: For organizations with more individual members or those seeking more marketing exposure</th>
<th>Standard: Our most popular corporate membership package</th>
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<tr>
<td>Number of employees who receive individual membership benefits</td>
<td>No limit to number of individual members with full online access; Up to 5 receive print magazine</td>
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<tr>
<td>Access to IMAPSsource, the microelectronics research portal</td>
<td>IP recognition allowing unlimited access for all computers in one network</td>
<td>150 downloads via two (2) selected member logins</td>
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<tr>
<td>Press releases in Corporate Bulletin</td>
<td>Up to 1 press release per bulletin (twice monthly)</td>
<td>Up to 1 press release per bulletin (twice monthly)</td>
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<td>Member pricing for exhibitor events</td>
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<td>JOBS Marketplace</td>
<td>Complimentary job postings</td>
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<td>Use of membership mailing list</td>
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<td>1x per year</td>
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<td>IMAPS.org advertising</td>
<td>Complimentary</td>
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<td>Magazine advertising</td>
<td>One 1/4 page ad included annually, plus 15% discount on any additional</td>
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<tr>
<td>Online Industry Guide</td>
<td>Includes company listing, link to website, product and service categories</td>
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<td>Global Business Council</td>
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<tr>
<td>Webinar Sponsorship</td>
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<tr>
<td>Annual dues</td>
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<td>$750</td>
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IMAPS has introduced a new level of support for corporate members. These companies have decided to participate in our Society at the Premier Corporate Member level. We are extremely grateful for their dedication to the furtherance of our educational opportunities and technological goals.
IMAPSource transitioned to membership level plans for free downloads on April 1, 2016. The number of free annual downloads included in your membership corresponds to your member type.

Non-members can enjoy articles and proceedings from IMAPSource for $20 per download.

IMAPS members are pre-registered with IMAPSource and receive a profile confirmation email from Allen Press. This will help members gain unlimited download access to IMAPSource. Non-members and guests will need to click Register Now at IMAPSource.org.

In 2017, free downloads will be subject to membership level below. Non-member downloads will be subject to a per-article charge.

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<th>2017 IMAPSource Membership Plans:</th>
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<tr>
<td>Affiliate (International Chapters/Unemployed Members)</td>
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<td>Retired/Senior Retired/Corporate International</td>
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</table>

*Unlimited package allows multiple IP range and unlimited access

Contact IMAPS HQ today for more information about IMAPSource registration, member benefits, IP range setup for Premier Corporate and Academic Institution members and more!
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<table>
<thead>
<tr>
<th>Chapter Name</th>
<th>Contact</th>
<th>E-mail</th>
</tr>
</thead>
<tbody>
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<td>Garden State</td>
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<td>Indiana</td>
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<td><a href="mailto:lwallman@sbcglobal.net">lwallman@sbcglobal.net</a></td>
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<tr>
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<td>San Diego</td>
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<td>Viking</td>
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<tr>
<td>Nordic</td>
<td>Terho Kutilainen</td>
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<tr>
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<tr>
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<th>Contact</th>
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<tr>
<td>IMAPSource</td>
<td>Brian Schieman</td>
<td>412-368-1621</td>
<td><a href="mailto:bschieman@imaps.org">bschieman@imaps.org</a></td>
<td><a href="http://www.imaps.org">www.imaps.org</a></td>
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</tr>
<tr>
<td>Indium</td>
<td>Rick Short</td>
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<td><a href="mailto:nshort@indium.com">nshort@indium.com</a></td>
<td><a href="http://www.indium.com">www.indium.com</a></td>
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<tr>
<td>Master Bond</td>
<td>Robert Michaels</td>
<td>201-343-8983</td>
<td><a href="mailto:info@masterbond.com">info@masterbond.com</a></td>
<td><a href="http://www.masterbond.com">www.masterbond.com</a></td>
<td>27</td>
</tr>
<tr>
<td>Mini-Systems, Inc.</td>
<td>Craig Tourgee</td>
<td>508-895-0203</td>
<td><a href="mailto:ctourgee@mini-systemsinc.com">ctourgee@mini-systemsinc.com</a></td>
<td><a href="http://www.mini-systemsinc.com">www.mini-systemsinc.com</a></td>
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### Advancing Microelectronics

#### 2017 Editorial Schedule

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<td>Ceramic: Thick and Thin Film</td>
<td>Sep. 8</td>
<td>Sep. 13</td>
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### IMAPS Headquarters

#### Who to Call

- **Michael O’Donoghue**, Executive Director, (919) 293-5300, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction
- **Brian Schieman**, Director of Programs, (412) 368-1621, bschieman@imaps.org, Development of Society Programs, Website Development, Information Technology, Exhibits, Publications, Sponsorship, Volunteers/Committees
- **Ann Bell**, Managing Editor, *Advancing Microelectronics*, (703) 860-5770, abell@imaps.org, Coordination, Editing, and Placement Management of all pieces of bi-monthly publication, Advertising and Public Relations
- **Brienne Lamm**, Marketing and Events Manager, (919) 293-5600, blamm@imaps.org, Corporate Membership, Membership and Event Marketing, Society Newsletters/Emails, Event Management, Meeting Logistics and Arrangements, Hotel and Vendor Management
- **Shelby Moirano**, Membership Administration, (919) 293-5000, smoirano@imaps.org, Member Relations and Services, Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support
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<td>2017</td>
<td>APRIL</td>
<td>4-19-17</td>
<td>4-21-17</td>
<td>IMAPS/ACerS 13th International Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT 2017)</td>
<td>Nara, Japan</td>
<td><a href="http://www.imaps.org/ceramics">www.imaps.org/ceramics</a></td>
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<td>4-26-17</td>
<td>4-27-17</td>
<td>2017 RaMP Workshop and Tabletop Exhibition</td>
<td>Espace Saint-Martin, Paris - France</td>
<td><a href="http://www.imaps.org/rf">www.imaps.org/rf</a></td>
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<td>JUNE</td>
<td>6-15-17</td>
<td>6-15-17</td>
<td>Advanced Technology Workshop and Tabletop Exhibition on Advances in Semiconductor Packaging</td>
<td>Binghamton University, Vestal, NY</td>
<td><a href="http://www.imaps.org/asp">www.imaps.org/asp</a></td>
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<td>6-27-17</td>
<td>6-29-17</td>
<td>System-in-Package Technology Conference and Exhibition 2017</td>
<td>Sonoma, CA</td>
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<td>JULY</td>
<td>7-10-17</td>
<td>7-12-17</td>
<td>HiTEN - High Temperature Electronics Network</td>
<td>Cambridge, United Kingdom</td>
<td><a href="http://www.imaps.org/hiten">www.imaps.org/hiten</a></td>
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<td>OCTOBER</td>
<td>10-9-17</td>
<td>10-12-17</td>
<td>IMAPS 2017</td>
<td>Raleigh, NC</td>
<td><a href="http://www.imaps.org/imaps2017">www.imaps.org/imaps2017</a></td>
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