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The move toward 3D packaging has been heavily talked about for the past 10 years. Go to any conference on packaging and there is a plethora of technical discussion of 3D. The technology is sound and the performance advantages are clear. However, cost has been one of the limiting factors here.

The beauty of the electronics industry is that companies and organizations are always innovating. One of the keys to the success of 3D is the advancement in interposer technology. This is where we have focused our search for articles in this issue of Advancing Microelectronics magazine. Most of today’s packages are made of organic materials. The choice of organics is obvious based on cost and availability. However, they present a CTE mismatch with the silicon die. This presents a significant challenge when moving towards 3D. Glass and silicon materials will match the die and present much better dimensional stability. The 1st article in this issue focuses on the advantages that glass provides such as cost and material properties. Whereas, in our 2nd article, RF technology is an application where Si interposers are being investigated. This article looks at the development of 3D RF interposer technology where key technological parameters are looked at and their RF performance is compared based on several characteristics.

Another common limitation with 3D is the limited bandwidth between the processor and 3D memory, and trying to achieve high bandwidth with low power. In this issue, a look at interposer-based and stack solution technologies is discussed including the problems associated with such systems.

The concept of 3D is often discussed around consumer technologies because of how it helps continue miniaturization while still improving functionality. In this month’s article titled High-Voltage Stacked Diode Package, the concept of 3D is permeating the high power segment for devices like IGBTs. While size is important here, the overall performance of these devices is critical. This is an excellent example of 3D outside of consumer spaces.

Having uniformity for the 3D stacked structures can also be challenging, having an in-line control of the uniformity is very important. In this month’s issue one article discusses and evaluated the various optical metrology techniques used for in-line monitoring of all process steps related to 3D IC applications. This article shows the importance and challenges that are associated with 3D control and uniformity during the process steps. This issue will discuss interposer technologies, the challenges, and ideas for advancing the technology.

We continue to strive to make this magazine full of relevant content that is enjoyed by our audience. As you read through it, please provide us feedback on ways we could make it even better. We believe Advancing Microelectronics is a great place for publishing highly technical content. If you are interested in contributing to this magazine through a technical article, please let us know and we will work with you.
President’s Message

This is my first message to the Advancing Microelectronics community as President of IMAPS. I am pleased and optimistic about our plans for the year ahead and for the future of the Society. I cannot address the future, however, without first acknowledging the continued fine work of IMAPS Executive Director Michael O’Donoghue and Director of Programs and Technology Brian Schieman along with the entire IMAPS staff who continually do more with less. I also wish to recognize the dedication of all my many colleagues who act as leaders both in the Society and to the microelectronics community at large by their dedication and service through their work on the Executive Council or one of the many IMAPS supporting committees, as Chapter leaders, as Symposium, Conference, Workshop or Session chairs or presenting or exhibiting at IMAPS events. I would like to particularly acknowledge Urmi Ray, General Chair, and Erika Folk, Technical Chair, for their great work in leading the team to create a very successful International Symposium in Florida. Each of these activities is a valued contribution that strengthens our Society and works to our mission statement to “lead the microelectronics packaging, interconnect and assembly community, providing means of communicating, educating, and interacting at all levels.”

Looking ahead, I am pleased to say that we have an excellent team on this year’s Executive Council and on the Symposium and Technical Committees, all of whom are ready to roll up their sleeves and meet the challenges that face us. Although the financial outlook has certainly improved over the last two years, our industry continues to see strong consolidation and reduced travel budgets. Additionally, as the boundary between back end of the line and first and even second level packaging blurs, IMAPS has increased direct competition from other associations including applications-oriented groups such as in Power, RF, etc. The goal is to grow our events and increase our visibility and reach in an increasingly crowded event environment. We plan to meet this challenge first and foremost by continuing to elevate our technical content and identify and focus on leading edge technologies. Matt Nowak, VP of Technology, and Urmi Ray continue to strengthen the Technical Committee and there is an exciting slate of Advanced Technology Workshops planned along with the expected-to-sell-out Device Packaging Conference, CICMT 2016, HiTEC 2016 and of course, the 49th International Symposium in Pasadena, CA. Peer and exit review of our Professional Development Courses are also in place to ensure topics that are on-point to our membership. The Executive Council is also looking at collaboration opportunities with other events to extend the IMAPS range and reach beyond our current boundaries with lower financial risk. In 2015, it was my pleasure as President-elect to present at the IMAPS All Asia Conference in Kyoto, Japan. It was a very successful event and I hope in my term as President to develop more joint initiatives.

One of the most exciting initiatives started under last year’s Executive Council and coming to fruition now is the roll-out of iMAPSource®. Our goal is to reinvigorately increase academic technical submissions by improving citation statistics via iMAPSource®. The IMAPS body of knowledge back to 2010 has been transferred to a fully searchable, user and Google-friendly database. Those of us who were frustrated with i-Know need to take a look. This is an entirely different experience. I have seen this tool provide fast and easy access to IMAPS publications with fully exportable citations, improved keyword and Boolean search functionality and customizable alerts. Brian Schieman, IT wizard extraordinaire for IMAPS, has already seen big increases in traffic since the rollout at the Symposium. IMAPS members have unlimited access until March 31 so that they can see the greatly improved capability for themselves. I urge you to try it.

We are committed to improving our reach and service to the microelectronics community but, of course, as we know, services and infrastructure improvements come with a cost. Along with focus on technical strength, and growth through technical outreach, we need to be mindful of fiscal preservation to ensure continuity of the Society and of the Microelectronics Foundation. To this end, after detailed review, we are raising the IMAPS regular individual membership fee to $95 per year and the regular corporate membership to $750 per year. This increase, the first in more than a decade, will help defray some of the transfer and maintenance costs incurred in establishing the database while we assess demand. We see visibility on Google scholar as essential to maintain relevance in the 21st century especially to up-and-coming scholars. I think this is a modest increase for the benefit it can provide and I feel strongly that the membership will see the value once they try it.

Last, I ask each of you to consider that IMAPS is what we make of it. I have been active in the Society at the local, national and international level and the technical, business, and collegial support I have received in return has been more than worth the effort. I encourage you all to get involved in some way. If you are involved, introduce a mentee or colleague to a conference or chapter meeting. The Society is its membership. Active members, new and old, make it possible for themselves. I urge you to try it.

I look forward to a busy and productive year ahead!
Progress and Application of Through Glass Via (tgv) Technology

Aric B. Shorey and Rachel Lu, Corning, Incorporated, Corning, NY USA, shoreyab@corning.com

INTRODUCTION

New initiatives in semiconductor packaging have created needs for new materials solutions. There has been substantial effort to extend interposer technology for 3D-IC stacking. Multiple solutions are being developed to address some of these needs including traditional interposers utilizing various commonly used materials as well as Fan-Out Wafer Level Packaging (FOWLP), which has become a popular consideration in an attempt to achieve lower cost [1]. Furthermore, the proliferation of mobile devices and the Internet of Things (IoT) leads to increasingly difficult requirements in RF communications. These include such requirements as the introduction of more frequency bands, smaller/thinner package size and need to conserve power to increase battery life as new functionality is introduced. Glass has proven to be an excellent solution to these challenges [2].

Glass has many properties that support the initiatives described above. These include high resistivity and low electrical loss, low or adjustable dielectric constant, and adjustable coefficient of thermal expansion (CTE). There has been much work in recent years as researchers demonstrate leveraging glass properties to achieve these objectives [3]-[6].

In order to leverage glass for many RF and interposer applications, it is often necessary to have precision vias for electrical interconnect and other functional purposes. The ability to put precision holes in glass and downstream metallization to create these vias continues to mature towards volume manufacture. Work in recent years has also demonstrated the reliability of these structures in glass [7]-[9].

Over the past several years at Corning Incorporated, there have been significant advances in the ability to provide high-quality vias in glass substrates of various formats. Examples are shown in Figure 1. The process employed provides the opportunity to leverage both through and blind vias in both wafer and panel format. The glass substrates with holes have been shown to give strength on par with bare glass, and filled vias have been shown to have excellent mechanical and electrical reliability after thermal cycle tests [9]-[11]. The approximate current best practice capabilities are summarized in Table 1 below. These represent guidance for the current TGV process, but in many cases the capabilities can be extended.

In addition to enhanced technical performance, packaging solutions must also be cost effective. Glass forming processes such as Corning’s fusion forming process, gives the ability to form high quality substrates in large formats (>> 1 m in size). The process can be scaled to deliver ultra-slim flexible glass to thicknesses down to ~100 µm. Providing large substrates in wafer or panel format at 100 µm thickness gives significant opportunities to reduce manufacturing costs. The advantages given by Corning’s fusion forming process for supplying substrates for electronics applications, has been previously reported [7], [8].

ABSTRACT

Glass provides many opportunities for advanced packaging. The most obvious advantage is given by the material properties. As an insulator, glass has low electrical loss, particularly at high frequencies. The relatively high stiffness and ability to adjust the coefficient of thermal expansion gives advantages to manage warp in glass core substrates and bonded stacks for both through glass vias (TGV) and carrier applications. Glass also gives advantages for developing cost effective solutions. Glass forming processes allow the potential to form both in panel format as well as at thicknesses as low as 100 µm, giving opportunities to optimize or eliminate current manufacturing methods.

As the industry adopts glass solutions, significant advancements have been made in downstream processes such as glass handling and via/surface metallization. Of particular interest is the ability to leverage tool sets and processes for panel fabrication to enable cost structures desired by the industry. Here, we provide an update on advancements in these areas as well as handling techniques to achieve desired process flows. We also provide the latest demonstrations of electrical, thermal and mechanical reliability.

Key words: through glass via (TGV); glass; panel
### II. Glass Material Properties

#### A. Adjusting the CTE for Carrier and Interposer Applications

Glass material properties are determined by the specific chemical make-up of the glass, making it possible to tailor glass composition to achieve a targeted CTE, thus enabling management of stack warp. Previously, we have shown examples of the material properties of two fusion formed glass types, in which it is possible to achieve very different CTE values while maintaining similar mechanical properties [7].

One of the important challenges in 3DIC stacking is reliability due to CTE mismatch and glass provides an excellent opportunity to manage warp of 3D-IC stacks but optimizing CTE. [6] Figure 2 gives an illustration of the challenge of stacking substrates with multiple CTE in an interposer application. Figure 2a schematically shows Si chips mounted on a Si interposer, which is then mounted on an organic substrate. The CTE mismatch causes failures when the substrates go through temperature cycles. However, if instead of a Si interposer, a glass interposer with CTE in between glass and organic is used, this warp can be better managed and increased reliability realized as demonstrated in work at Georgia Tech’s Packaging Research Center (PRC) and illustrated in Figure 2b [6].

Figure 2. Illustration of CTE mismatch in 3DIC stacking.

#### B. Electrical Performance

As new, higher frequencies used in RF applications are released, the electrical properties of the substrates become increasingly important. As a semiconducting material, standard silicon tends to have increased loss at higher frequencies. Work done in collaboration with the Industrial Technology Research Institute (ITRI) in Taiwan illustrates this well [14]. In this work co-planar waveguides (CPW), micro-strip lines (MS) and co-planar waveguides with 2 vias were constructed on glass and silicon substrates, and impedance matched to ~50 ohm. The structures were then tested up to 20 GHz and insertion loss was characterized. The results are shown in Figure 3. Since glass is an insulator, there is much less loss as frequency is increased beyond a few 100s of MHz. Given the importance of minimizing power loss at these higher frequencies coupled with the need to continue to reduce package size, glass provides valuable material for all applications working in the GHz range.

A good example of leveraging the insulating properties of glass is to provide high-Q inductors and capacitors in a glass-based LC network as recently described [2]. In this work, the high-Q inductors were created by utilizing solenoid inductors shown schematically in Figure 4a. The top and cross-sectional view of the fabricated inductors is shown in Figures 4b and 4c respectively. High-Q capacitance was achieved by utilizing a metal-insulator-metal construction. Figure 5 shows the MIM capacitor formed on the same TGV glass substrate.

---

**Table 1. TGV specification**

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Current Capability*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outer Diameter (OD)</td>
<td>25 – 100 um</td>
</tr>
<tr>
<td>Minimum Pitch</td>
<td>~2x OD</td>
</tr>
<tr>
<td>Type</td>
<td>Through and Blind</td>
</tr>
<tr>
<td>Wafer Size</td>
<td>Up to 300 mm</td>
</tr>
<tr>
<td>Panel Size</td>
<td>Up to 515 x 515 mm</td>
</tr>
<tr>
<td>Thickness (mm)</td>
<td>0.1 – 0.7</td>
</tr>
</tbody>
</table>

*Approximate.
The TGV IPD parts were mounted on evaluation boards and further tested for both electrical functionality and thermal and mechanical reliability, showing no performance degradation or any board-level reliability issues. The insulating properties of glass provide very high-Q performance.

**Thermal Cycle Testing**

The fabrication of thin glass interposers with Cu filled through glass vias (TGV) was done using standard back end of line (BEOL) fabrication tools with no significant modification of any of the equipment wafer handling to accommodate glass wafers. In order to test the effect of the glass CTE on the long term reliability of the glass interposers, 150 mm glass wafers formulated with two different CTEs, 3 ppm/°C and 8 ppm/°C, were used in the fabrication process.

Full thickness 150 mm glass wafers with 35 µm x 125 µm blind TGVs were sputtered with a thin adhesion layer of Ti and Cu. No barrier or additional dielectric layer were deposited in the TGVs before the metallization. Highly conformal copper seed layers were deposited using metalorganic chemical vapor deposition (MOCVD), in preparation for TGV plating. The seed layers were nominally 0.75µm in thickness, which was uniform throughout the TGVs. Electroplating of Cu was used to fully fill the TGVs and the overburden was removed using chemical mechanical polishing (CMP). High resolution x-ray imaging was used to verify the void-free nature of the Cu fill in the TGVs. To form the TGV test structures, plated Cu routing layers were patterned on both sides of the thin wafers. These routing layers were electroplated on a sputtered Ti/ Cu seed layer with no barrier covering the glass substrate. Thin wafer handling was done using 3M’s Wafer Support System (WSS). More details on the fabrication of these glass interposer test vehicle wafers can be found in previously published work [9].

After fabrication was completed, wafers from each glass type were electrically tested for continuity of the daisy chain test structures. Electrical continuity testing was done on eight test arrays, randomly chosen across the diameter of four wafers. Each test array consisted of 20 x 20 TGVs on 100 µm pitch, with each of the TGVs connected in series. The TGV test chain array, an example of which is shown in Figure 7, has testing points at the front and back of every TGV, so that any electrical discontinuity can be tracked down to the single metal link or TGV. The results of the initial round of electrical continuity testing are shown in Table 2. The combined yield of the TGVs and routing metal links was over 99.85% for both types of glass.

**Table 2. The results of 2-wire electrical continuity tests on 20 x 20 arrays of TGVs on 100 µm pitch.**

<table>
<thead>
<tr>
<th>Wafer</th>
<th>CTE (ppm/°C)</th>
<th>No. of 20x20 arrays tested</th>
<th>Yield of TGVs &amp; routing metal (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SGW3 - Wafer 1</td>
<td>3.2</td>
<td>8</td>
<td>99.97</td>
</tr>
<tr>
<td>SGW3 - Wafer 2</td>
<td>3.2</td>
<td>8</td>
<td>99.97</td>
</tr>
<tr>
<td>SGW8 - Wafer 1</td>
<td>8.1</td>
<td>8</td>
<td>99.72</td>
</tr>
<tr>
<td>SGW8 - Wafer 2</td>
<td>8.1</td>
<td>8</td>
<td>100.00</td>
</tr>
</tbody>
</table>

After this initial test, eight additional test arrays were selected from each type of glass with starting TGV array yields of 100%. These arrays were then subjected to thermal cycle testing, which consisted of 1000 cycles from -40°C to 125 °C with 1 hour cycle time and 15 min soak
time at each temperature extreme (JEDEC JESD22-A104 condition G). An intermediate test point of 500 cycles was also done. The results of electrical testing at 0, 500 cycles, and 1000 cycles are shown in Table 3. Figure 8 shows the TGV profile after 1000 thermal cycles. Note that there is no cracking or delamination seen.

<table>
<thead>
<tr>
<th>No. of thermal cycles</th>
<th>Wafer</th>
<th>CTE (ppm/°C)</th>
<th>Yield of TGVs &amp; routing metal (%)</th>
<th>Median chain resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 cycles</td>
<td>SWG3-Wafer 1</td>
<td>3.2</td>
<td>100.00</td>
<td>10.4</td>
</tr>
<tr>
<td></td>
<td>SWG8-Wafer 2</td>
<td>8.1</td>
<td>100.00</td>
<td>6.7</td>
</tr>
<tr>
<td>500 cycles</td>
<td>SWG3-Wafer 1</td>
<td>3.2</td>
<td>100.00</td>
<td>15.4</td>
</tr>
<tr>
<td></td>
<td>SWG8-Wafer 2</td>
<td>8.1</td>
<td>100.00</td>
<td>13.5</td>
</tr>
<tr>
<td>1000 cycles</td>
<td>SWG3-Wafer 1</td>
<td>3.2</td>
<td>100.00</td>
<td>16.6</td>
</tr>
<tr>
<td></td>
<td>SWG8-Wafer 2</td>
<td>8.1</td>
<td>100.00</td>
<td>15.9</td>
</tr>
</tbody>
</table>

Table 3. The results of 2-wire electrical continuity tests on eight known-good 20 x 20 arrays of TGVs on 100 µm pitch before and after thermal cycle testing.

III. Form Factor

Another valuable aspect of leveraging glass as a semiconductor packaging substrate is that the forming processes lend themselves to providing large form factors [7], [8]. This is important as the IoT will require billions and even trillions of devices and sensors. Being able to utilize economies of scale given by panel processing is very important.

Handling of ultra-thin glass in standard wafer or panel processing operations can be a challenge. However, solutions are being developed. Corning’s Advanced Lift-off Technology (ALoT) is a carrier-based solution that is designed to be compatible with high temperatures (> 450 C) without outgasses, as well as maintaining compatibility with important process chemistries such as cleaning (SC1, SC2, etc.) and metallization. The process is shown schematically in Figure 11.

Recent work has shown significant progress in the ability to process glass panels > 500 mm in size [15]. An important outcome of this work demonstrated one advantage of using glass in this application. Specifically, that the increased stiffness and thermal stability of glass relative to current solutions results in improved flatness (see Figure 9).

In Figure 9a, the profile of a 508 mm x 508 mm panel size glass substrate with two layers build-up after pre-cure processes is shown. Figure 9b shows the profile of organic substrate after same processes. There is ~3 x better warp-performance for the glass based substrate. This has important implications in that the improved flatness of the glass based substrate enables finer lines and spacing for redistribution layers relative to organic substrates. This allows high performance devices to be fabricated in a panel format, which provides substantial opportunity for both cost effective and high quality solutions.

In addition to scaling glass substrate size, it is possible scale the process to deliver ultra-slim flexible glass to thicknesses down to ~100 µm (see Figure 10). Providing large substrates in wafer or panel format at 100 µm thickness gives significant opportunities to reduce manufacturing costs because there is likely to be no need for grinding and polishing operations.

Figure 8. Cross section SEM image from an interposer test vehicle in SGW3 glass after 1000 thermal cycles. These were measured to be from 17 µm to 19 µm in diameter at the wafer backside and 35 um diameter at the front side.

Figure 9. (a) Warpage measurement result of glass substrate after two layers build-up; (b) Warpage measurement result of organic substrate after build-up.

Figure 10. Manufacture of high quality ultra-slim flexible Corning® Willow® Glass provides substantial opportunities to deliver substrates for TGV that do not require post processing.

Figure 11. Schematic showing an approach for handling thin glass through metallization.

continued on page 10
continued from page 9

The approach is to apply a surface treatment on a glass carrier wafer to prevent permanent bond at high temperatures, while maintaining enough adhesion strength to enable via and surface metallization. The thin metallized glass TGV wafer will then be mechanically de-bonded and processed further. This approach is relevant for wafers and panels.

Work recently at RTI International in Research Triangle, NC, has been done to demonstrate the feasibility of utilizing the ALoT structure to perform metallization of the vias. Glass with 100 um thickness and ~30um diameter through vias was provided on a carrier. RTI then applied the seed layer and via fill using a process consistent with the method used to fill blind vias [9]. However, instead of back grinding to expose the bottom of the vias, with ALoT the thin glass is peeled off mechanically as shown schematically in Figure 12. Figure 13 shows the 150 mm bonded wafers.

Figure 12. Cartoon of leveraging ALoT technology to metallize through vias in 100 um thick glass.

Figure 13. Image of 100 um thick glass with 30 um diameter vias temporarily bonded onto a glass carrier using ALoT technology.

Figure 14 shows the result after via metallization and overburden removal from the top surface. The thin glass completed processes for via metallization, overburden removal and Chemo-Mechanical Planarization (CMP) and very good planarity of the Cu and glass surface was achieved. After completion of top surface CMP, the wafers were mechanically de-bonded and an SEM image of the TGV on the back surface was collected to evaluate the ability to achieve good planarity without any post-processing (e.g., there was no planarization of the back surface). Figure 15 shows an SEM image of the back surface TGV after de-bond. There is work to be done to achieve perfect bond and planarity, but the result shows the feasibility of using this approach to effectively fill TGV in thin glass. Optimization of this method provides exciting opportunities to dramatically enhance cost effectiveness of providing thin glass solutions by eliminating back grinding operations and enabling further downstream process optimization. Furthermore, while this demonstration was completed in 150 mm wafer format, it is scalable to 300 mm wafer and even panel formats.

Figure 15. SEM image of bottom of metallized via after de-bond (no polishing).

V. Conclusion

Glass has a number of properties that make it an exciting material for various packaging applications. The electrical performance of glass gives reduced electrical loss relative to silicon. This becomes even more important at high frequencies, which will be used for next generation mobile networks. The important implication would be the ability to increase smart phone functionality while maintaining or extending battery life.

Adjusting material properties like CTE generates tremendous incentive for using glass as a TGV substrate for 2.5D and 3D applications in multiple forms. Furthermore, the ability to form high-quality glass in thin, large sheets enables a number of opportunities to reduce cost. Handling technologies that provide means to effectively process ultra-thin glass are being demonstrated.

Well-formed through and blind vias have been demonstrated and existing metallization technology can be leveraged to generate very good Cu filling performance in glass in both wafer and panel formats. Reliable performance of Cu-filled vias in glass has been demonstrated. These developments make glass an exciting material for next generation packaging applications.
Acknowledgment

The authors would like to extend sincere thanks to their development partners at RTI International, Industrial Technology Research Institute (ITRI) and Georgia Tech’s Packaging Research Center (PRC).

References


Towards 200mm 3D RF Interposer Technology

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Abstract
With the advent of modern and autonomous electronics, applications using RF (radio frequencies) up to millimeter waves and beyond are proliferating. The systems integration becomes increasingly challenging due to the variety of devices and passives that typically compose such RF modules, and careful choices of materials are needed for low loss interconnects. One way to minimize RF losses is to integrate the module with high performance interconnect using Si technology, where the different devices are mounted on the interposer and the passives are integrated into the silicon. Thanks to TSV (Through Silicon Via) technology and use of High Resistivity Si substrates, it is possible to have small form factor modules. Such an integration approach allows benefit from the well-established base of 200mm foundries together with the recent progress made in High Resistivity substrate manufacturing.

In this work, the process development of a 3D RF interposer technology based on a 200mm process line is reported. The build-up contains 2 levels of metals processed by Cu damascene technology, including a thick 2µm top metal for the lower frequencies applications, an integrated MIM (Metal Insulator Metal) capacitor and use of through silicon vias in 5kOhm high resistivity 85µm thick substrates. The TSVs are 20µm diameter and 85µm deep made in via first manner with via reveal using temporary carrier handling. Various RF passivation techniques for the silicon have been investigated and a comparison to quartz based on similar test structure is discussed.

A variety of passive devices, transmission lines and filters have been processed and characterized. The technology yields 1µm pitch interconnect routing layer, a line loss of 0.34 dB/mm at 40 GHz, and high quality factors inductors larger than 30.

Key words: Interposer, High Resistivity Silicon, Integrated Passive Devices, Through Silicon Vias

I. INTRODUCTION
The ability of integrating high quality components onto a 3D Silicon platform has been demonstrated on multiple occasions [1,2]. CMOS (Complementary Metal Oxide Semiconductor) manufacturing techniques can be used to produce such interposers and be able to use extremely high density interconnects that cannot be realized with standard laminate technologies [3]. In order to realize such 3D modules, via middle approach is used that has the potential to eliminate the drawbacks of high loss dielectric used in via last [4]. Such approach is compatible with the industry mainstream for interposers nowadays: via middle.

In this paper, the process technology used for RF interposers and study of the impact of key technological parameters, such as surface treatment [5] and CMP (Chemical Mechanical Polishing) related design rules on the RF performance of the build-up are discussed. It is demonstrated that high quality passives can be produced in a standard foundry environment.

II. TECHNOLOGY DESCRIPTION
Starting from a 5kOhm-cm HR (High Resistivity) substrate, the wafers are treated for surface RF passivation (see comparison between treatments later in the next paragraphs), then processed with through silicon via in a via middle manner. The TSV are 20µm in diameter and 85µm deep. The first metal level is 0.6µm thick whereas the second metal level is 2µm thick to offer low resistivity for the low frequency range. Once the front side of the wafer is completed, the wafers are mounted onto a temporary carrier to proceed to TSV reveal. The complete build up is shown on Figure 1.

A 0.5um diameter via level forms the vertical interconnect between the 2 Cu layers, while a MIM structure of TaN/SiO2/TaN is formed directly on top of the first Cu layer. The MIM structure is designed to achieve a capacity density of 1fF/µm². The top plate of the MIM doubles as a resistive layer to form resistor lines. The sheet resistance of this layer is targeted at 50 Ohm/sq.

On Figure 2, a SEM view of the thick metal is shown, resistor and cap module. On Figure 3, the TSV connection to the first Cu level is shown and on Figure 4 the high density routing layer made in 2 µm thick Cu with 1 µm L/S design rules is visible.

The entire process flow is executed in IMECs clean room which is 200mm CMOS compatible processing fab.

III. IMPACT OF SUBSTRATE TYPE ON CPW LINE
The resistivity of the substrate and microwave losses are of utmost importance on signal integrity. The transmission performance of co-planar waveguide (CPW) lines based on various substrates is studied. As can be seen on Figure 5, the substrate needs to be both of high resistivity larger than 1.5kOhm cm and treated to reduce impact
of mobile charges at the surface of the substrate. A comparison to 200mm quartz substrate processed on the same platform is shown on the same plot.

![Figure 5: Impact of substrate type on CPW line performance.](image)

**IV. INDUCTOR PERFORMANCE: IMPACT OF DESIGN RULES CONSTRAINTS AND PROCESS TECHNOLOGY**

In the next section, inductor performance is reported. The performance of such type of device is very sensitive to process variation and RF losses and is therefore a very good indicator of the suitability of the technology.

**Multi-turn inductors**

On Figure 6, a top view picture of the realized inductor is shown. On Figures 7 and 8, the Q (Quality) factor and the inductance values for simulation, HR Si + Sipos (Semi Isolating Poly Silicon) surface passivation and thinned HR Si+ Sipos, are shown. As can be seen, there is a very good matching between simulation and measurements for the 2 nH inductor with 3.5 turns and inner radius of 50 µm.

![Figure 6: Top view of multi-turn inductor.](image)

![Figure 7: Q factor of "2nH" multi-turn inductor as a function of frequency.](image)
B. Impact of dummies and slotting

During fabrication, copper dummy structures and perforation of wide Cu lines are typically used for Cu damascene process. Such dummies and perforation rules are there to minimize Cu density variation over the wafer for better planarization and thickness control during the Cu CMP step.

The presence of Cu structures potentially influences the performance of the RF device. Design variations in “dummification” and perforation were evaluated to have a better understanding of the impact of damascene design rules.

On Figures 9 and 10, the impact of the slotting and perforation of the signal lines on the inductor performance of a half coil inductor with radius of 150 µm is plotted. The slotting layout is shown on Figure 11.

It is seen that slotting and perforation affect the Q to a large extent but not with respect to inductance value and self-resonance. It is believed that this is due to the increase of resistance of the inductor trace.

Figure 12 shows that there was no difference between a coil that had dummies inside compared to a dummy-free coil as long as the dummies are sufficiently far away from the signal lines, here 20 µm. The layout of the test structures is shown on Figure 13.

C. Impact of surface passivation treatment on inductor performance

Several techniques have been reported to reduce losses; according to our findings, this can be achieved in multiple ways. On Figure 14, the Q factor of a “2nH” half coil inductor is plotted. It highlights the importance of high resistive silicon in combination with different surface passivation methods: deposition of SiPos, a-Si or Poly Si. The next Figure 15 shows the inductance values. There is no major difference seen between various passivation techniques, a-Si, Poly-Si, and SiPos for high resistive silicon wafers.
D. Mismatch between simulation and measurements of half coil inductors

Although results for several passivation techniques are very similar, performance for the half coil inductor is not in agreement with simulations for frequencies above 5GHz. Figure 16 shows the comparison of measurements on SiPos passivated high resistive Si, with simulation for perfectly passivated silicon, and with measurements on unpassivated high resistive substrate.

The root cause of these losses is currently still under investigation. It is possibly related to the large area of this half coil inductor design, because the effect is less visible on the smaller area multi-turn inductors (Figure 7).

V. PASS BAND FILTER EXAMPLE

Besides the single passive characterization, several filters were realized. On Figure 17, the layout of a simple bandpass filter is shown with 2 half coil inductors and 4 MIM capacitors. Figure 18 shows the measurements of filter characteristics together with the simulated behavior.

The device functions as a bandpass filter at 5GHz.

VI. SUMMARY

In view of characterizations performed above, it can be concluded that excellent performance is achieved by this Si platform up to 40 GHz. The 3D TSV interposer yield RF losses of 0.34dB/mm which are very close to the one to quartz indicating proper RF passivation treatment. On top of this, the impact of the dummies and slotting typically induced by CMP-related design rules was investigated and it is demonstrated that high Q factor inductors, larger than 30, passive components can be realize with fine pitch lithography, despite such design rules constraints. However, for large inductor structures, a decay in Q factor is observed, a phenomenon that cannot be explained by either metal dummies or substrate/surface losses. It appears that this is size related, keeping in mind that, normally, large inductors values have no purpose for mm-wave designs.

VII. CONCLUSIONS

In this paper, fabrication of RF interposers, using 200mm CMOS compatible platform, is reported. The process has been developed and devices have been characterized, showing performance comparable to low loss material such as quartz. Adequate surface passivation technique have been producing very low line loss. The technology appears to be very suitable for high performance RF and mm wave 3D system in a package.

For the large device, such as half coil inductors, a parasitic behavior is observed that cannot be explained in

continued on page 16
a trivial manner by damascene dummies, substrate losses or substrate thickness. Specific radiation patterns or interaction with the measurement equipment might be the root cause of this.

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References
Goal
The Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT) conference brings together a diverse set of disciplines to share experiences and promote opportunities to accelerate research, development and the application of ceramic interconnect and ceramic microsystems technologies. This international conference features ceramic technology for both microsystems and interconnect applications in a dual-track technical program. The Ceramic Interconnect track focuses on cost effective and reliable high performance ceramic interconnect products for hostile thermal and chemical environments in the automotive, aerospace, lighting, solar, defense/security, and communication industries. The Ceramic Microsystems track focuses on emerging applications and new products that exploit the ability of 3-D ceramic structures to integrate interconnect/packaging with microfluidic, optical, micro-reactor and sensing functions. Tape casting, thick film hybrid, direct write and rapid prototyping technologies are common to both tracks, with emphasis on materials, processes, prototype development, advanced design and application opportunities.

Ceramic Interconnect Track
Conventional thick and thin film ceramic technologies are being revolutionized and extended through the development of low temperature co-fired ceramics, photo patterning, and embedded passive component materials and processes. These have contributed to increased circuit density, enhanced functionality, and improved performance that are being adopted for leading edge applications in wireless and optical communications, automotive, MEMS, sensors, and energy. Data communications and the Internet are driving the demand for bandwidth, sparking demand for optical communication equipment and new interconnect and packaging applications that perform at 40 Gb/sec and beyond. In under-the-hood electronics (for automotive, engine/transmission control), communications and safety applications continue to drive the growth of ceramic interconnect technology, while collision avoidance systems are creating interest in low loss ceramic materials for frequencies approaching 100 GHz.

Ceramic Microsystems Track
Enabled by the availability of commercial ceramic, metal and embedded passives materials systems, and the rapid prototyping capabilities of the well established multilayer ceramic interconnect technology, three dimensional (3-D) functional ceramic structures are spawning new microsystems applications in MEMS, sensors, microfluidics, bio-devices, microreactors, and metamaterials. These new devices and applications exploit the ability to integrate complex 3D features and active components (e.g., valves, pumps, switches, light pipes, and reaction chambers).
In addition, the Ceramic Microsystems track of the CICMT conference targets new developments in microsystems that include fabricating 3-D micro device structures enhanced with sol-gel, advanced printing and patterning technologies, high temperature materials technologies, and emerging applications like energy harvesting. Many of these innovative applications are taking advantage of the unique ability to integrate the thermal, chemical, mechanical and electrical properties of these multicomponent ceramic-metal systems.

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I. Introduction

High bandwidth, low latency and less power for memory interfaces has been a requirement for the last few decades. Industry has progressed from slow SDRAM in interface running at 66MHZ to DDR4 running at 1600MHz providing 3.2Gbps data transfer rate. But the main architecture did not change drastically. But in the last few years, new memory architectures are being introduced by industry with a goal of achieving high bandwidth with low power. These standards are Wide-IO/1-2, HBM (high bandwidth memory) and HMC (hybrid memory cube).

One thing common to the above mentioned new memories is their application in vertical stacked or the 2.5D/3D architecture. Wide IO offers high bandwidth using 64 IOs per channel for 4 or 8 channels, HBM increases the IO count to 128 bit per channel, while HMC pushes towards much less IO count with very high speed Serdes IO. Given these different new memory standards with different set of advantages and disadvantages, the design space for a system architect has increased considerably to decide on the optimum solution. This paper will focus on a few technological aspects of the decision making process while choosing between these new technologies coming into the market and puts some light on what can be done to cope with these new challenges.

Two technological options being looked towards for these memories integration are shown in Figure 1. An interposer solution is more looked towards in these years because of less difficulty in manufacturing and reliability as compared to the full 3D stack integration using TSVs [1].

HBM is specifically designed for 2.5D interposer solution and provides a reasonable bandwidth with a moderate number of IOs. But it must be kept in consideration that all of these technologies internally do depend on TSVs for their internal working which still is a factor yet to be seen in terms of reliability as mass production of one of these devices starts and we start to get the yield results. Pure 3D stacking of memory onto logic die is challenging due to Active TSVs and heat problems, so industry is looking to first cross effectively the 2.5D barrier and then go towards the 3D milestone.

In the rest of this paper, the main challenges in each of the three emerging memory technology integration will be discussed along with some possible solutions and to find an optimal solution. Logic die to be interfaced with memory on an interposer has to be sized based on the memory selection for interface and the technology chosen for the interposer. Wide IO is suitable for interposer applications but the increase in bandwidth is smaller than what one can get from HBM and HMC. The main challenge for HBM is efficient routing on the interposer to achieve the required bandwidth while handling the cross talk and lossy interposer effects. The most important design problem for HMC is high power usage leading to large heat dissipation, effective cooling strategies requirement, and connecting large Serdes IP Blocks on HMC to pads on memory die along with Serdes block on the memory controller interface along with its routing to the controller PAD. How does the routing distribution layer affect the signal quality/integrity on the memory die and then the controller die. Route and place for copper pillars or micro bumps is not streamlined and poses a great challenge to companies that still stick to the old peripheral Wirebond PAD to C4 ball routing rather than moving to Area array PADS on top of IO Block to reduce the routing interconnect loss. This paper tries to look at these main challenges for each technology and describes the huge increase in design space for a memory system architect.

II. Logic Die Dependencies

A. Die Size

In 2.5D integration, the choice of 3D memory type and interposer technology decides the size of the logic die and interposer size as shown in Figure 2.

To understand this, take the example of a Wide IO-2 interface requiring 8 x 64 channels with total bandwidth
of 409.6 Gbps. The total number of IOs required is 512. To achieve this interface, suppose that two technologies can be used. One is the Cu Pillar technology with pitch size of about 200µm and other is copper pillar technology with pitch of about 110µm. So, if we only had to connect the IO signals with interposer (ignoring for now the power ground connections), then 512 IOs can be adjusted using:

- Cu Pillar technology (110 µm pitch) in a 3×3 mm2 die which can provide up to ~700 (=3000/110)2 connections to interposer
- C4 bump technology (200 µm pitch) in a larger die of 4.6×4.6 mm2 die which can provide up to ~529 (=4600/110)2 connections to interposer

It should also be noted that power/ground connections generally are an order ~1.5 times the number of signals in the die. But with interposer integration of memory and logic using small copper pillars for large IOs and bandwidth also needs almost double the number of power/ground connections. Also, the number of these power connection from die to interposer increase due to small size of copper pillar tip where electro migration effects can really cause a problem. So to avoid these electro migration effects, it is much better to increase the number of power/ground connections as much as possible considering the worst case minimum current density possible for the interposer power copper pillar connections.

B. Logic Die Pad-to-Bump Routing

In interposer-based solutions, when the logic die is being designed for the memory interface, there are two main options just like the Flip chip designs.

- Peripheral IO Pads
- Area IO Pads

In each of the above methods, in the end for connection to the interposer, there is a grid of Bump Pads for Copper pillars or C4 Bumps. There is a requirement for one or more RDL (routing distribution layer) for routing from Peripheral/Area IO pads to the bump pads for copper pillar or C4 Bumps. In Peripheral IO Pad placement in classical manner, there are combinations of long and short interconnects which have to routed from peripheral pads to grid area bump pads. If there is a specific width of RDL, then the width of RDL is specified by the current density requirement for a specific number of power/ground connections. This large metal width can pose routing congestion problems and the design may need multiple RDLs for routing.

In area IO, if there is free assignment of IO Pads then this theoretically can give the optimum routing solution with minimum total wire length (TWL). But in practice, it is not so easy to completely make the IO Pads freely assignable due to power ground meshing requirements and some specific IFs which makes the routing problem a mixture of Pre-assigned and Freely assignable IO Pads which need to be then routed to grid of bump pads. There is literature available on the free assignable IO Pads routed to bump pads minimizing the TWL [2], but there is no available yet algorithmic software solution to address the problem of practical designs with a mixture of Pre-assigned and Free-assignable IO Pads.

To understand the problem, see Figure 3 and Figure 4 which show the problem of heterogeneous IO Block size causing extremely variable routing length for different IOs. In Figure 3, grid of bump pads is shown along with rectangular blocks which represent the IO blocks in the logic die. We can assume that this die is for interfacing to a Wide IO-2 memory which requires small IO cells placed all over the area of the chip. In this case, since these small IO Blocks can be easily placed in a regular manner and in ideal case, just below the bumps to reduce the interconnect length. While in Figure 4, it is assumed that there is a lot of logic required to handle the serdes IO channels along with serdes large IO blocks for HMC. Since these serdes blocks are quite big in size, they cover a large part of the bump grid which makes the ratio of directly under the bump placement of IOs quite less, eventually resulting in high variability routing interconnects especially for the power ground which also are quite large in number because of high power requirements of the HMC. So, it can be concluded from Figure 3 and Figure 4 that designing of logic die for HMC and Wide-IO memories require different routing algorithms and there are quite different routing challenges along with power requirements that need to be considered in the interposer based 3D memory system design.

III. Interposer Technology

A. Dielectric Material, Metal Layers

Interposer technology greatly impacts the system design for memory logic on the interposer. Currently, for silicon interposers two different options for the dielectric material exist: namely, SiO2 and polymers. Both materials necessitate their own integration schema. For example SiO2 requires planarization steps (CMP – chemical mechanical polishing), while polymers are difficult to level. On non-planarized surfaces, the achievable resolution of line/space features is lower compared to flattened surfaces. This is because advanced lithography faces severe limitations on flat surfaces. On the other hand, every CMP step increases the overall costs.

The manufacturing processes for SiO2-based stacks are derived from the (upper layer) metallization processes in classical 65 nm or 45 nm technology nodes. Typically, up to five layers are fabricated for such stacks. The resulting minimum line/space is in the range of 100 to 500 nm. These metallization technologies are usually combined with TSVs with a diameter of 10 µm. The majority of the
SiO2-based interposers directly expose the TSVs on the backside to mechanical and chemical-mechanical processes without the deposition of additional metallization layers. On the other side we have polymer-based stacks with 2 or 3 metal layers on top as well as 2 or 3 metal layers on the bottom side. In this approach the TSV diameters are also 10 µm but the metal line/space is in the range of 8 µm to 10 µm. This option is especially interesting for low cost interposers because most of the chemical-mechanical process steps are cut out and also the masks for the lithography are cheaper due to lower resolution requirements.

If SiO2-based stacks are applied, smaller line/spaces are possible in comparison to the polymer approach, while the TSV diameters are comparable. As a result we have the same parasitics for the TSVs in both cases. But on the other side, the parasitics for the interconnect structures differ a lot (see Table 1). The smaller interconnects of SiO2 stacks should result in smaller capacitances because the area for coupling is much smaller. The relative permittivity of SiO2 is 3.9 and 3-4 for polymers. Hence, assuming identical dielectric thickness the influence on parasitic capacities is comparable.

Then again the polymer approach offers a higher flexibility with regard to the polymer thicknesses. Polymers can be deposited in fine graded steps with a high thickness (e.g., 10 µm dielectric heights, Table 1, Polymer 2). These thick layers result in reduced parasitic capacitances compared with SiO2 based stacks (54 % reduction in our examples).

Furthermore, the interconnect resistances of polymer-based stacks are smaller because of the larger interconnects. The cross section area of interconnect structure on polymer technology is 25 times larger compared with the SiO2 technology.

As a result it can be shown that the RC delay as a first order approximation for the interconnect delay can be better controlled on interposers with polymer stacks. If the polymers are thick enough, the RC delay of polymer stacks is 30-50 times smaller compared to SiO2 stacks (see Table 1).

Summarizing the previous facts, the realization of interposer interconnects with a length of up to 2 cm becomes a very hard challenge. Compared to chip layouts we do not have the possibility to place buffers to drive long wires.

To give an example prototype, Figure 8 shows an interposer designed and fabricated at Fraunhofer. It is a silicon interposer with a polymer material used as dielectric for the metallization (parameter values close to polymer 1 in Table 1). On the left side the pads for the Wide IO-memory are visible, on the right is the processor footprint. The dimension of the whole module is smaller than a 1 cent coin, which illustrates the capability of this integration technology for high performance yet compact applications.

<table>
<thead>
<tr>
<th></th>
<th>Polymer 1</th>
<th>Polymer 2</th>
<th>SiO2</th>
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<tbody>
<tr>
<td>w (µm)</td>
<td>10</td>
<td>10</td>
<td>1.2</td>
</tr>
<tr>
<td>s (µm)</td>
<td>10</td>
<td>10</td>
<td>0.8</td>
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<tr>
<td>l (cm)</td>
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<td>1</td>
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<tr>
<td>t (µm)</td>
<td>3</td>
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<td>h (µm)</td>
<td>3</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>e_r</td>
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<td>3</td>
<td>3.9</td>
</tr>
<tr>
<td>R (Ohm/mm)</td>
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<td>18</td>
</tr>
<tr>
<td>C (F/mm)</td>
<td>187</td>
<td>113</td>
<td>246</td>
</tr>
<tr>
<td>RC-delay (ps/cm)</td>
<td>1.37</td>
<td>0.83</td>
<td>44.28</td>
</tr>
</tbody>
</table>

Table 1: Parameter values of three different interposer technologies based on different dielectric materials (compare with Figure 5). Width w, spacing s, length l, thickness t, resistance R, and the RC-delay are related to the interconnect (wire). Height h, relative permittivity e_r, and the capacitance C are related to the dielectric material.

B. Relation Between Technological Options and Routing

Figure 6 illustrates the impact of the technology decision (i.e., polymer-based vs. SiO2-based interposer) on the conditions for interconnect routing. The increased width and spacing of interconnect structures on polymer-based interposers require a minimum of 3 metal layers for the break out routing of pads with a 40 µm pitch (Figure 6, left). In comparison for SiO2-stacks only 1 metal layer is needed in the same example (Figure 6, right). This assertion is true for signal nets only. Power/ground interconnects aren’t manufactured with the smallest possible line/space because the resulting resistance would be too high. Such high resistances imply problems with static and dy-
namic voltage drops and also with electromigration. Furthermore, only if the netlist graph is planar (i.e., without crossing edges on a 2D plane) a single metal layer can be sufficient. Thus, in realistic scenarios at least 2 metal layers are required even for SiO2 stacks.

IV. Multi Physical Effects

There is a combination of electrical, mechanical and thermal challenges in 3D memory system design. These three different physical aspects have varying degrees of effect in HMC, HBM and Wide I/O system design because each of these runs at different bandwidth, consumes different power along with hugely different number of IOs (compare Wide I/O to HMC). Main electrical issues in all three designs are crosstalk noise, delay in the interposer/PCB interconnect and power ground induced noise due to high switching. Also, HMC and HBM have logic dies at the bottom representing the controller for DRAM dies stacked on top which is completely new for companies and steps must be taken to ensure the logic die problems are solved in the system design.

Thermal heat removal issues aggravate due to the ever increasing performance requirements, which within a given technology typically correlate with power consumption. Figure 7 illustrates common interdependencies [3]. The amount of physical side effects caused by heat dissipation is increasing in 2.5D and 3D integrated systems since more active devices are packed into smaller volumes. The thermal design is therefore an important part of the whole system design. If the thermal problems of a system cannot be solved the resulting product is not manufacturable.

If the design is for Wide I/O, then TSV related issues, mechanical stress and heat are the main factors which are also common with the HBM and HMC designs. But the HMC design suffers from higher speed design challenges and requirements which are not so significant at slower speed ~2Gbps Wide I/O memory interface interconnects. Also, it should be considered during the design process that HMC needs specific Phy for serdes and a controller IP only for serdes itself along with the controller part of the DRAMS stacked on top of the logic die in HMC. These Serdes Phy IPs may come with other restrictions which can significantly change the design process and degrees of freedom.

V. Conclusion

In this paper, different technological options were compared for memory logic 2.5D integration. Logic die size, routing requirements and metal layers of interposer dependency on 3D memory chosen for the system integration is explained in detail. It shows that the memory system architect must now think in several new dimensions never seen before to effectively choose the 3D memory and integrate it into the system.

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High-Voltage Stacked Diode Package

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Abstract
The Army is moving to a more electric force with a number of high-voltage applications. To support this transition, there have been efforts to develop high voltage (15-30 kV) single-die 4H-silicon carbide (SiC) bipolar switches and diodes. However, packaging these high-voltage devices has proven to be challenging since standard packaging methods cannot withstand the high voltages in a compact form. Therefore, this work aims to develop a compact prototype package with improved size, weight, and power density by stacking diodes. The stacked diode approach allows elimination of almost half of the wire-bonds, reduces the board size by 45%, and reduces the package inductance. A module has been designed, fabricated, and tested which is the first 30 kV module reported in the literature to stack two high-voltage diodes in a series configuration. The package has a number of features specific to high-voltage packaging including (1) two fins that extend the perimeter of the package to mitigate shorting, and (2) all the leads were designed with rounded corners to minimize voltage crowding. Hi-pot tests were performed on the unpopulated package and showed the package can withstand 30 kV without breaking down. The completed package with the stacked diodes showed avalanche breakdown occurring at 29 kV. The complete package was then compared to an equivalent discrete diode module and showed a 10X reduction in size. During a clamped-inductive load test the stacked diodes showed lower parasitic capacitance, faster reverse recovery time, and lower turn on energy as compared to the discrete diode packages.

Key words: 3D chip stack, high-voltage packaging, power electronics, stacked diodes

1. Introduction
Development of next-generation switches and diodes is under way for pulsed and continuous power applications requiring ultra-high voltage operation. Technological advances in epitaxial growth greater than 100 µm have enabled the design and fabrication of silicon carbide (SiC) devices with blocking voltages exceeding 10 kV [1]-[3]. These state-of-the-art devices are currently being considered for an increasing number of Army applications including survivability and lethality systems, radar systems, medical systems, materials processing, air/water purifications, electro-photography, and power transmissions.

In addition to device fabrication challenges, existing power electronics packaging limits device capability and performance. In many implementations, devices are derated due to package limitations. Additionally, the devices typically occupy only a small percentage of the actual package making the package large and heavy. Packaging techniques must be developed to support high-voltage handling capabilities in compact form.

Present high-voltage switches are typically gas switches or high-voltage relays and they operate in a vacuum, sulfur hexafluoride (SF6), hydrogen, or transformer oil. Gaseous electronic switches have a number of disadvantages: low durability, large size, high manufacturing and maintenance costs, and short operating life. Therefore, silicon IGCTs (Insulated Gate Bipolar Transistors) have slowly replaced gas switches in some fields for improved reliability; however, operation at very high voltages requires the stacking of several devices in series to be able to withstand the high electric field. In addition, higher currents require the parallel connection of devices. The increase in volume and complexity might also warrant additional requirements such as isolation barriers, creepage constraints, cooling, and multiple gate drivers [6]. Therefore, CREE is developing single-die 4H-SiC bipolar switches which have many advantages over gas and silicon switches: wide band-gap, greater thermal conductivity allows operation at greater current densities, and a higher critical field allows for significant reduction in size and volume.

High-voltage devices in the 15-30 kV class are a new area of research. Therefore, standard packaging has not yet been developed to support such high voltages. Current power module packaging comprises devices soldered to a DBC (direct bonded copper) substrate which are soldered to a heat spreader which is attached by a thermal interface material (TIM) to a heat sink. This packaging method has three primary failure locations [7]-[9]: the DBC [10, 11], wire-bonds, and large area attach. A DBC substrate is two layers of copper sandwiching a thick ceramic, either aluminum nitride (AlN) or aluminum oxide (alumina). The present standard ceramic thickness is 0.025” which can withstand <10 kV. DBC having 0.040” thick ceramic is also available that can withstand <15 kV. Thicker DBC (specifically silicon nitride based) is being developed but is very costly. This leads to the need to develop a reliable high-voltage module which eliminates the DBC.

The present 15 kV high-voltage packages for SiC high-voltage switches are 65.5 mm long, 28 mm wide, and 19 mm tall, two of which are shown stacked in Figure 1 to achieve a 30 kV package. This package was designed strictly as a testing vehicle for single-device evaluation of...
SiC JBS (Junction Barrier Schottky) diodes and IGBTs and not optimized for size; however, an alternative package does not exist [5, 6]. For operation above 15 kV, at least two diodes must be connected in series. Therefore, the goal of this research is to develop a compact 30 kV high-voltage package with improved size, weight, power, cost (SWaP-C), and reliability. The improvement is achieved using a new approach to packaging which stacks the high-voltage diodes.

II. Proposed High Voltage Package

The new prototype package is shown in Figure 2 and has dimensions 37.75 mm x 28 mm x 26 mm. The two 15 kV stacked diodes are shown in the center. The prototype package is 10X smaller and weighs significantly less than the previous package, as is shown by the size comparison in Figure 1. The new package has eliminated the three primary failure locations of existing power electronics modules: wirebonds, DBC, and large area attaches. Cost is reduced by eliminating the expensive DBC and using a low cost ABS (acrylonitrile butadiene styrene) 3D printed housing. ABS was used as a proof of concept at low temperatures; in a commercial package, a more robust plastic can be used if desired.

Figure 2: Picture of the complete stacked diode assembly with the main features called out.

The prototype package is 10X smaller and weighs significantly less than the previous package, as is shown by the size comparison in Figure 1. The new package has eliminated the three primary failure locations of existing power electronics modules: wirebonds, DBC, and large area attaches. Cost is reduced by eliminating the expensive DBC and using a low cost ABS (acrylonitrile butadiene styrene) 3D printed housing. ABS was used as a proof of concept at low temperatures; in a commercial package, a more robust plastic can be used if desired.

Figure 3 shows in red the novel high voltage aspects of the package. To reduce the likelihood of voltage breakdown through air, three methods were implemented: (1) fins, acting as voltage breakdown barriers, were designed around the perimeter of the package; (2) the leads were placed on opposing sides to maximize the distance between them; and (3) the leads were designed with rounded corners to mitigate voltage crowding. This package is a potential precursor to putting a stacked diode pair onto a DBC board which has many benefits: elimination of almost half the wirebonds, almost a 50% reduction in board size and inductance reduction.

III. Package Fabrication

There were a number of complexities associated with fabricating the stacked diode packages: making the devices solderable, allowing proper electrical isolation, and lead spacing. In addition, proper alignment of the five layer stack and placement of the leads on the stacked assembly was critical. After a number of design iterations, the final six step assembly process is as follows:

Step 1: Metalize top of diodes to make solderable using evaporated 50 Å Titanium / 1 μm Nickel / 100 Å Gold on the active electrical contact area. The bare die diodes have an existing top side aluminum metallization which is ideal for wirebonding but is not compatible with solder. The diodes are 8 mm square with a 3 mm square active area in the center. The large perimeter is necessary for voltage isolation.

Step 2: Fabricate the Kovar pieces for soldering to the devices in the stacked assembly. Gold plated Kovar was chosen for use in the stacked assembly due to its close coefficient of thermal expansion (CTE) match to silicon, availability in the lab, and solderability. The available Kovar in the lab was 0.5 mm, so it was first necessary to solder two pieces together using gold-tin (AuSn) preforms to achieve the desired 1 mm thickness for voltage isolation. One side of the Kovar was also pre-tinned using a AuSn preform to eliminate the majority of preforms needed for the stacked assembly. This was done on a 1 inch square of Kovar which was then cut into 3 mm squares to match up with the active area on the top of the diodes. The completed structures are shown in Figure 4. Three of these simple, identical structures are necessary for each assembly.

Figure 4: Pre-tinned 3mm square pieces of Kovar for use as electrical contacts and spacers in the stacked assembly.

Step 3: Create stacked diode assembly by aligning using an aluminum fixture in a solder reflow oven. Figure 5 shows the assembly process used to create the stacked assembly. A five part reusable aluminum fixture was machined to maintain alignment during the reflow process. continued on page 24
continued from page 23

It consisted of four identical T-shaped pieces to align the stack and an outer ring to hold the T-shaped pieces in place. The five layer stack was assembled (Steps 3a-c). One side of each of the Kovar pieces was metalized with AuSn to act as a preform and one additional larger AuSn pre-form was needed in the center of the stack (Step 3b). Then the remaining fixture pieces were put into place (Step 3d). Finally, a calibrated weight was placed on top of the stack and the assembly was reflowed in a SST solder reflow oven (Step 3e). The completed five layer stack of alternating Kovar and diodes is shown in Figure 6.

Step 4: Fabricate the leads and assemble them with the device stack. The leads were first machined out of copper and the ends were pre-tinned using tin-lead (SnPb) solder, shown in Figure 7. The curved shape of the lead reduces voltage concentrations. The two smaller holes are for alignment during soldering as well as the locations of the screw attachments in the package. The large hole is also used for alignment as well as electrical connections.

The leads are then soldered to the chip stack using a wood solder fixture, shown in Figure 8a, to align leads and solder to the middle of the side Kovar pieces. Two screws are permanently glued into the fixture for initial alignment of the leads, shown in 9a. Figure 8b shows a cross section of the assembly indicating the stacked diode assembly and the locations of the alignment pins with the wood block.

The solder assembly process is shown in Figure 9. The leads are first placed onto the fixture through the permanent screws, then tightened into place with additional alignment created by another screw (Step 4a). Next, Step 4b, the stacked diode assembly is placed vertically between the leads and aligned using square ceramic pieces on each side. The assembly is then hand soldered using SnPb on each side (Step 4c). SnPb has a much lower melting temperature than AuSn so there is little chance of reflowing the AuSn during the lead attachment process. Last, solder wick is used to remove excess solder on one side to ensure it sits flat in the housing (Step 4d).

Step 5: Assemble the housing. The two-part housing, shown in Figure 10, is fabricated using a 3D printer out of ABS plastic. The two fins encircling the housing (perimeter fins in the Figure) are necessary to prevent voltage breakdown through air between the leads. The two ledges on each side of the housing are for lead attachment.
An exploded view of the housing assembly process is shown in Figure 11a. First an epoxy layer (Hysol E20HP) is applied to the top of the lower part of the housing. Then the leaded assembly is placed onto the epoxy and the screws are tightened into place which align the assembly into the housing, shown in Figure 11b. Two staggered screws are located on each side to absorb any lead stress before it reached the diodes. In addition, the screws are in opposite directions to reduce the likelihood of voltage concentrations on any one side of the module. The top part of the housing is then epoxied into place ensuring no gaps where encapsulant can leak out or locations of voltage breakdown. Figure 11c and d show the front and top views of the assembled package.

Step 6: The final step in the assembly process is encapsulation, a critical step in high voltage modules. The chosen encapsulant was Sylgard 572. The liquid encapsulant was poured into the package and then deaerated in a vacuum oven (Figure 12a) to eliminate any bubbles present in the encapsulant. The final cured encapsulant is clear and shown in Figure 12b.

IV. Experimental Results

High potential (hi-pot) testing was initially performed on a package without devices to assess where and at what voltage breakdown occurred. The package consisted of the plastic housing, leads, and encapsulation without the device stack. A corona camera was used to visualize the location of the breakdown. The mockup design had electrical breakdown around the perimeter at 28.5 kV. The corona camera images of the breakdown are shown in Figure 13 where flashover occurred around the perimeter from the screws. This led to a redesign of the package with an increased fin height and successful hi-pot testing >30 kV.
Avalanche breakdown testing was next performed on a packaged part with functioning devices and the breakdown occurred at 29 kV with a leakage current of 3.7 µA. The blocking characteristics of the stacked diodes are illustrated in Figure 14.

Next, the experimental diodes were subjected to dynamic testing using the clamped-inductive circuit shown in Figure 15. In this case, the diode package was connected across the inductive load and acted as a clamping diode to protect the IGBT switch.

During clamped-inductive load testing, the discrete and the stacked diode packages were compared against each other during switching transitions. Figure 16 shows the IGBT’s collector-to-emitter voltage $V_{ce}$ and collector current $I_c$ waveforms as a function of time. When comparing the plots of collector voltage, both waveforms displayed minimal voltage overshoot, which means the diodes are clamping the voltage rapidly as expected. When comparing the plot of collector current, there was significantly less overshoot with the stacked diodes, which indicates the compact package had lower parasitic capacitance. Figure 17 shows the current waveforms of the diodes during the switching events. The stacked diodes showed lower reverse recovery peak current and time as illustrated by the amplitudes. The turn on energy for the stacked diodes was about 25% less than the turn on energy for the discrete diodes (8.6 mJ for the discrete and 6.7 mJ for the stacked).

V. Conclusions

High voltage SiC devices in the 15-30 kV class are a new area of research. Therefore, the packaging has not yet been optimized to support such high voltages. This paper has shown a stacked diode package with reduction in size, parasitic elements, and energy losses over larger previously tested packages. A repeatable, relatively simple six step fabrication method has been outlined achieving a module capable of withstanding 29 kV. The module is also inexpensive and relatively stress free. Innovative aspects of the high voltage module include: stacked diodes, wirebondless module, elimination of large area contacts, and opposing leads and perimeter fins to reduce voltage breakdown.

Figure 14: Leakage current of stacked JBS diodes.

Figure 15: Clamped-inductive switching schematic.

Figure 16: IGBT switching characteristics of both the stacked diode module (left set of graphs) and discrete diode packages (right set of graphs).

Figure 17: Diode current waveforms for the stacked diode module (left) and discrete diode packages (right).
Acknowledgments
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References
Control of 3D IC Process Steps by Optical Metrologies

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I. Introduction
The use of Through-silicon via (TSV) to conquer the third dimension enables keeping a very small form factor and opens up the way to stack far more than two dies.

Among the 3D process integration flow, key 3D process steps were identified and characterized in order to quantify their specific intra-wafer dispersion signature.

One of the key success factors for this technology is maintaining the wafer uniformity across the whole process flow. Several of the major 3D integration process steps are known to create strong non-uniformity across the wafer, namely:
- Through Silicon Via (TSV) etching
- Wafer/carrier bonding and thinning
- TSV reveal etching

Each of these 3D process steps generates a specific non-uniformity signature, and these add up to a cumulative dispersion on the final wafer.

The development of non-destructive optical metrology techniques is therefore critical in order to provide information on the dispersion of the related key parameters of TSV depth, carrier and glue thickness, Remaining Silicon Thickness (RST) – the thickness of the silicon on top of the TSV after thinning – and the copper nails dimension, i.e., the height of the TSV extrusion after the TSV reveal process.

In this paper, we evaluated several optical metrology techniques for the intra-wafer uniformity control of the specific process steps mentioned previously. The metrology capability was evaluated through a repeatability test. The accuracy was verified, where possible, with reference techniques or at least double-checked with comparative techniques.

For the interconnect steps, full field optical metrology techniques have been studied to assess the impact of the environment on the copper pillar height measurement.

II. Optical Metrology Techniques
In this section, we describe the optical metrology techniques used for the intra-wafer uniformity measurements of the key parameters associated with the 3D process steps.

A. Optical Head Configuration
Figure 1 shows an internal view of the patented FOGALE optical system developed and used for the experiments [1]. It includes a top optical head with microscope objectives designed to allow thickness, gap and etch depth measurements by Near-Infrared (NIR) Optical Coherence Tomography (OCT) combined with white light or infra-red microscopy, wafer shape profiling and nails/pillar height by visible full field interferometry [2, 3, 4].

Mapping can be performed with a fast, motorized XY translation of the aperture 300mm wafer chuck.

By using the NIR OCT, a TSV depth patented method consists of using a beam spot size larger than the TSV diameter [3]. Two groups of waves are coming back from the top and bottom of the measured TSV and give directly the TSV depth without aspect ratio limitation. The combination of this technique with white-light microscopy in...
the same optical path allows the user to position the spot very precisely and also to obtain top CD.

For silicon, glue and carrier thickness measurements, a commercial system with a dual-probe IR low-coherent Michelson interferometer operating at a wavelength of 1.3µm was used. The specific dual probe configuration where two interferometers are located on different parts of the sample (top and bottom) allowed obtaining individual and total thickness measurements on the same location of the stacked structures.

The principle of the Michelson interferometer operating system is illustrated in Figure 3. The sample is illuminated with a light beam, and a dependence of the reflected light intensity against the interferometer’s reference arm length, is mathematically processed. The light is generated by a light source (LS), split by a beam splitter (B), directed, through lenses L1 and L2, to a moving reference arm element (R) and to a sample (W), reflected back, collected together with the same beam splitter, and directed into a detector (D). When the optical path from a beam splitter to a reference arm element R is equal to a path to sample surface, an interference peak happens. For the case of multi-stacked structures, the resulting diagram will present several peaks corresponding to each interface. The thickness of the individual layers can be calculated from the distance between the two peaks divided by the layer’s material refractive index [5].

B. Multi-Wavelength OCT in Spectral Mode

By using a 1.31µm Super Luminescent Diode (SLD) as a light source for the NIR OCT, the minimum measured thickness is limited to 20/n µm (n being the refractive index of the layer to be measured). To decrease this value, it is necessary to increase the source bandwidth in order to decrease the signal width. To reach silicon thickness measurement capability down to 1µm, the SLD is replaced by a halogen lamp and the signal is analyzed by a spectrometer. The Fourier transform of the signal gives the thickness value directly.

C. White Light Chromatic Confocal

For surface profiling metrology, the White Light Chromatic Confocal technique can be applied [4]. As shown in Figure 4, this technique uses a custom lens with very large axial chromatic aberration. Thus every wavelength of the large-spectrum source is imaged in a different plane. The one focused on the surface is more coupled with the detector than the others. As there is a unique correspondence between wavelength and distance, the spectrum returned allows extraction of the distance at which the surface is lying.

D. Full Field Interferometry

As shown in Figure 5, full field interferometry is using an interferometric objective for microscopy. The optical view of the sample is converted to an elevation map using interferogram processing techniques. The height of each pixel is determined independently one to each other with a nanometer level accuracy in a single scan. Lateral resolution depends on the objective magnification and camera pixel size.

Light is emitted by a selectable light source (So). A beam splitter (Sp) splits the light beam in two half beams marked as 1 and 2. This device is integrated inside the interferometric objective. One of the two beams is reflected by a reference mirror (M), the other is reflected at the sam-
E. Process Steps Characterization

For this study, we used an interposer product from a 65nm node technology with middle TSVs of 10µm diameter and 75µm depth. A production lot was run through all the process steps to the TSV reveal process where copper extrusions are formed at the surface of the stacked wafers. For TSV depth measurement, some wafers were extracted from the production lot. For the bonding, thinning, and TSV reveal process steps, the same production wafers were measured along the 3D process integration flow.

F. Through-Silicon Via Etching

The NIR OCT technique from Fogale was tested to characterize the TSV depth of the etching process. Four wafers from the same production lot were selected at different slot positions (1, 2, 7 and 15) to quantify the intra-lot etching process variability. One individual TSV was measured inside each lithography scanner field in order to perform full map measurement. This leads to 110 individual TSV measurements per wafer.

Repeatability tests were run through 30 static repetitive measurements on the same wafer using a specific 17-point mapping. The 1-sigma repeatability for single via measurement was calculated to be around 0.03µm, which is very low compared to the depth value (0.04%).

To check for the accuracy of this optical technique, comparative XSEM analysis was performed on one of the Middle TSV wafers. As presented in Figure 7, the TSV depths obtained by XSEM at center, mid radius and edge of the wafer correlate very well with the optically measured values ($R^2 = 0.9997$). Nevertheless, an offset of about 3.5% was found between the two techniques, XSEM-measured depth values being systematically larger.

<table>
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<tr>
<th>Depth (µm)</th>
<th>Wafer position in production lot</th>
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<tr>
<td></td>
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<tr>
<td>Minimum</td>
<td>71.65</td>
</tr>
<tr>
<td>Range</td>
<td>5.23</td>
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</table>

Table I. TSV Depth Measurements Across the Lot

Overall, the FOGALE metrology technique was therefore found reliable for the process control of TSV depth, as well as for characterization of the intra-wafer spatial signature.

G. Silicon Bonding and Thinning

Following the Middle TSV etch process, the production lot was run through multiple process steps to perform all the backend metallic connections. Wafers were then bonded on glass carriers with an adhesive layer consisting of 80µm thick resist. At the bonding and thinning steps, we focused on analyzing the Total Thickness Variation (TTV) of the individual layers and of the Remaining Silicon Thickness (RST).

Glass carriers are known to exhibit significant variation. The individual layers and the total stacked layers were measured with IR interferometry described previously. The glue thickness was found to be quite stable, with a small TTV of around 1µm, whereas the glass carriers TTV showed a range of up to 5µm. After the Si grinding process, the individual thickness measurements provide clear evidence that the TTV of the Si grinded layer is dominated by the initial glass carrier TTV. This is illustrated in Figure 7, where two different glass carrier shapes (convex and concave) as well as the corresponding Si grinded signatures are presented. To generate those simplified graphs, we used the full map thickness data and averaged the values along the different radius from the center wafer in order to get an estimated average profile.

From Figure 7, we observed clearly that the glass carrier and the thinned silicon signatures are reversed. This is actually fully predictable, as the grinding process tends to generate stacked Glass/Grue/Silicon wafers with very low TTV values. During the process, the thickness variability of the glass carrier is then simply reported on the grinded silicon layer.

At the grinding process step, we evaluate the combination of NIR microscopy, IR interferometry and IR multiwavelength spectrometry from Fogale to measure the Remaining Silicon Thickness (RST) above the TSVs [1]. This configuration allows the equipment to position the NIR beam precisely at the bottom of the TSV. We tested the technique on several stacked wafers with different glass carrier TTV signatures to obtain full map data (Figure 8).

A repeatability test was run through 30 static repetitive measurements on the same wafer using a specific 17-points mapping. The 1-sigma of repeatability for RST
measurement was calculated to be around 0.03µm for typical RST values around 20µm. Assessing the accuracy of the results is difficult due to the fact that stacked silicon wafers on glass are very difficult to characterize by SEM cross section analysis. Nevertheless, the RST values found were consistent with the post-grinding silicon thickness measured at a TSV-free location on the wafer, and the TSV depth measured at the etching process step.

Figure 7. Glass and silicon thickness variation across wafer diameter for the case of (a) convex glass signature, and (b) concave glass signature.

Finally, we investigate the validity of the reported TTV for the various thicknesses. The TTV reported for the RST measurement were actually in coherence with our expectation. Figure 9 shows a schematic representation of the intra-wafer signature for the two cases of glass shapes. For the case of Wafer A with concave glass shape, the glass and glue TTV were previously measured and found to be about the same amplitude of 1µm but reversed in sign. The RST TTV then simply results from the TSV depth signature, which was measured around 3µm (Table II). In the case of Wafer B, where the glass carrier is convex in shape, the Glass and Resist TTV are cumulative leading to higher TTV values. For the specific case, the resulting TTV is of the same amplitude as the TSV depth TTV but in reverse sign. The very low value for TTV of the RST can be simply explained by a direct compensation effect between both contributions (Table II).

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<table>
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<tr>
<th>Wafer</th>
<th>TTV (µm) within 120mm radius</th>
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<tr>
<td></td>
<td>Glass</td>
</tr>
<tr>
<td>Wafer A</td>
<td>-1</td>
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<td>Wafer B</td>
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Table II. TTV Evolution Along Process

We conclude that we can predict the TTV of the RST within 1µm based on the Glass, Glue and TSV etch pre-measured TTV signatures through (1):

\[ TTV_{RST} = TTV_{Glass} + TTV_{Glue} + TTV_{TSV	ext{-Etch}} \]  

(1)

Overall, we found that the RST measurements provided by the optical technique were stable and the resulting TTV consistent with the individual signatures.

H. Through-Silicon Via Reveal

The last step of the 3D integration flow studied here concerns the TSV reveal process, which consists of a backside process etching the RST layer in order to reveal the bottom of TSVs named copper nails. The height of those extrusions is targeted to be about 5µm from the top of the silicon backside surface. The height of the copper nails was measured for the full map by White Light Chromatic Confocal from Fogale (Figure 10).

Not only the height values, but also the intra-wafer dispersion of the copper nail height is critical for further process integration steps. We found that there are strong differences in behavior between wafers from the same production lot. To explain these differences, we studied, for wafers A and B, the TSV reveal etching profile signature with delta of pre/post measurement of the silicon thickness layer at the location on the wafer free of any TSVs and using the same average profile methodology as before (Figure 11).
We found that the plasma etching profiles vary significantly depending on the shape of the glass carrier. This is probably due to thermal or charging effects acting differently depending on the thickness of the insulating carrier. There is then a new intra-wafer signature of the final etching process that needs to be taken into account to understand the final copper nail height signature. In Figure 13, we schematized the various signature contributions including this final TSV reveal step.

Table III reports the copper nail height measured for wafers A and B. The nail heights of the two wafers are found to differ strongly in terms of intra-wafer signature. This is the consequence of both the glass carrier shape leading to different RST TTV, and the TSV reveal etching process signature being strongly impacted by the glass shape (Figure 12).

We found that the final copper nail height TTV signatures for Wafer A and Wafer B are in agreement within 1µm with the predicted values through:

\[
TTV_{\text{nails}} = TTV_{\text{Glass}} + TTV_{\text{Glue}} + TTV_{\text{TSV Etch}} + TTV_{\text{TSV Reveal}}
\]

Therefore, by knowing the Glass, Glue, TSV Etch TTV as well as the TSV reveal signature, we can predict the copper nails TTV. A benefit could be to adapt the TSV Reveal etching process to the RST signature in order to optimize the final copper nails signatures.

### Statistical Analysis of TSV Process Steps

#### Uniformity

To quantitatively analyze the model quality and measurement precision with respect to the spatial signature, the site level measurement data post TSV etch, bonding, thinning, and reveal have been aligned and loaded in a semiconductor data analysis system [6]. Here, “site” refers to a fixed position within the lithographic reticle field, of which there are 110 per wafer. The analysis is split in two parts: validation of the effects of the glass carrier shape and bonding on the pre-reveal remaining silicon thickness; and validation of the coherency of the measured copper nail height with the initial TSV etch depth and the remaining silicon thickness post-reveal.

The first analysis models the pre-reveal RST as a function of the thinning process, starting with the glass carrier and glue profile. Figures 13 and 14 show the measured RST vs. the modeled maps and site-level values. We observe good correspondence of the spatial wafer profiles as well as good linearity, with a Pearson $R^2 = 0.672$. The residual standard deviation of 0.68 µm is small compared to the median thickness of the (glass+glue) stack, which was measured at 833 µm.

We found that the final copper nail height TTV signatures for Wafer A and Wafer B are in agreement within 1µm with the predicted values through:

The second analysis validates the coherency between the TSV etch measurement (NIR OCT) and the post-reveal measurements (WLCC) for RST and copper nail height. Figure 15 shows the measured copper nail height vs. the theoretical nail height, calculated as the difference between the TSV etch depth and the remaining silicon thickness post-reveal. A good linearity is observed, with a Pearson $R^2$ value of 0.713. A mean offset of 3.1 µm is present between actual and modeled heights. In view of the results of Sec. IIIA, the offset is probably dominated by the TSV etch measurement.
For smaller copper nails diameter, confocal chromatic and other line scanning techniques have lateral resolution limitations (Figure 16). Full field interferometry is then the technology of choice for diameters below 3µm (Figure 17).

III. CONCLUSION
We have studied the benefit of various optical metrology techniques for the in-line uniformity control of 3D stacked wafers. Multiple optical technique configurations were implemented and allowed the monitoring of all process steps related to 3D IC applications. Through analysis of the complete set of measurement data collected, we demonstrated the impact of the dispersion of each process step on the final copper nail height signature. The study raised the importance of the glass carrier TTV control and/or selection. The glass shape is demonstrated to have a high impact on the silicon thinned TTV layer and the TSV reveal etching process leading to copper nails TTV signature strongly dependent on the stacked wafer configuration.

REFERENCES

Acknowledgment
Part of the work presented in this paper, was supported by the European EUREKA CATRENE program (MASTER 3D project).
In Memoriam – Ron Chalman

It is with deep sadness that IMAPS, on behalf of Chalman Technologies, announces the loss of an ISHM/IMAPS original member, Ron Chalman. Ron died on January 24th at the age of 80 after a long battle with pancreatic cancer.

Ron joined ISHM (IMAPS) in 1967, the year our Society began, and was an active participant locally in California and on the national level, presenting papers and sharing his expertise with the microelectronics, assembly, and electronic packaging industry professionals in attendance.

In the 1970s and the early 1980s, he was Vice President and General Manager of Tekform Products Co. in Anaheim, CA, and was heavily involved in the development of hermetic package design and technology. He consulted with JEDEC to develop some of the early hermetic standards covering this topic. In 1986 he fulfilled a dream and founded the rep firm Southern California Technical Services (later becoming Chalman Technologies), where he worked with his sons, daughter, and others until recently.

Survivors include his wife Marlene Chalman, two sons, three daughters and twelve grandchildren.

In lieu of flowers the family suggests donations in Ron’s name to either of the following charities:

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1201 W. La Veta Ave.
Orange, CA 92868
www.choc.org
714-997-3000

Wounded Warriors Project
PO Box 758518
Topeka, KS 66675-8518
http://www.woundedwarriorproject.org/
or call: 877-958-2233

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<td>NXP Semiconductors</td>
<td>BridgeWave Communications, Inc.</td>
<td>SP KTN</td>
<td>IMAPS France</td>
</tr>
<tr>
<td>Phone: +31 24 363 4411</td>
<td>Phone: 408-567-6951</td>
<td>Phone: +61 7 7330 748149</td>
<td>Phone: +33 (0) 1 56 04 53 44</td>
</tr>
<tr>
<td><a href="mailto:michel.de.largent@nxp.com">michel.de.largent@nxp.com</a></td>
<td><a href="mailto:Sean.Cahill@maximintegrated.com">Sean.Cahill@maximintegrated.com</a></td>
<td><a href="mailto:paul.huggett@espktn.org">paul.huggett@espktn.org</a></td>
<td><a href="mailto:brigitte.braus@airbus.com">brigitte.braus@airbus.com</a></td>
</tr>
</tbody>
</table>

Program Committee:

| Hansu Birl – HB Technology, Brazil | James Haley – Omet | David Virissimo – Arnetek |
| Mumtaz Bora – Peregrine Semitech | Casey Krawiec – Quix-Pak | Renzhe Zhao – Huawei |
| Liang Cai – Integra | Iris Labadie – Kyocera | Chris Hunt – IMAPS UK |
| Martin Goetz – Northrop Grumman | Andy Longford – IMAPS UK | Keith Arber – IMAPS UK |
| Ramesh Varma – Northrop Grumman | Ray Patel – Pacific Rim Scientific | Wei Fan – Momentive |
| Bill Ishii – Torrey Hills Technologies, LLC | Vern Styrer – AGC | Hannah Going – Accel RF |
| Carl Edwards – Adv. Materials Innovations | |

RF and Microwave Packaging Workshop Focus:
The objective of the RF and Microwave Packaging Workshop is to provide a unique forum that brings together scientists, engineers, manufacturing, academia, and business people from around the world who work in the area of RF and Microwave packaging technologies. This workshop enables discussion and presentation of the latest RF and Microwave technology. To help bring together the international community, this workshop is being co-sponsored by IMAPS-UK and will be the first in a series of joint workshops on RF and Microwave packaging between IMAPS and IMAPS-UK.
Sessions planned in the following areas:

<table>
<thead>
<tr>
<th>Emerging Technologies</th>
<th>New Design/Materials</th>
<th>New Applications</th>
<th>Current Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>• 60 GHz Personal Area Network (PAN)</td>
<td>• New Power Amplifier Design</td>
<td>• Military / space</td>
<td>• Medical electronics</td>
</tr>
<tr>
<td>• Short Wave IR Packaging</td>
<td>• Beyond LDMOS</td>
<td>• Optoelectronics (night vision, thermal weapon sight, etc.)</td>
<td>• Wearable electronics</td>
</tr>
<tr>
<td>• Nanopackaging</td>
<td>• Thermal Management</td>
<td>• High Power Electronics</td>
<td></td>
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<tr>
<td>• 3D RF/MW</td>
<td>• New Uncooled IR Sensors</td>
<td>• Space / Extreme Environments</td>
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<tr>
<td>• New and Disruptive Technology</td>
<td>• Plastic RF/MW Packaging</td>
<td>• MEMS/NEMS</td>
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<tr>
<td>• EMI Shielding for RF/MW Packaging</td>
<td>• RF MEMS</td>
<td>• Biomedical</td>
<td></td>
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<tr>
<td>• Wafer Level Packaging for Microwave and MM/Wave Applications</td>
<td>• Low loss, wide BW, high power interconnects</td>
<td>• Telecomm</td>
<td></td>
</tr>
<tr>
<td>• Packaging Issues for Wide Band Gap Semiconductors</td>
<td></td>
<td>• Reliability</td>
<td></td>
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<tr>
<td>• SIP</td>
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<td>• MMIC</td>
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<td>• Automotive</td>
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<td>• High Speed Electronics</td>
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</table>

Awards will be given in the following categories: Best ATW Paper; Best Session Papers; and Best Student Paper.

Student Competition sponsored by the Microelectronics Foundation:

The Microelectronics Foundation sponsors Student Paper Competitions in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Students submitting their work and identifying that "Yes, I'm a full-time student" on the abstract submission form, will automatically be considered for these competitions. The review committee will evaluate all student papers/posters and award at least one student author with a $1,000 check at the ATW/Conference. The selected student must attend the event to present his or her work and receive the award. The Foundation will return the registration fee for the winner. The winner must pay for travel and lodging expenses.

No formal technical paper is required. A reproduction-ready 2-page extended abstract with figures and graphs included, if necessary will be required for the abstract booklet on Feb 21, 2016.

Accepted papers may be considered for publication in the IMAPS Journal of Microelectronics and Electronic Packaging.

All Speakers are required to pay a reduced registration fee and are required to attend the entire Workshop to maximize opportunities for interaction with registered attendees. All authors and attendees find that this IMAPS Workshop format is a proven forum for informal but highly effective networking between attendees and speakers.

If you are having problems with the on-line submittal form, please email Ken Kuang at kkuang@torreyhillstech.com or call (858)559-6666.

Official RF and Microwave Packaging Workshop site: www.imaps.org/_rf
Advanced Technology Workshop
Chip-Package Interactions with Fan-Out Wafer Level Packaging
April 6-7 | www.imaps.org/cpi
DoubleTree, Mission Valley, San Diego, CA

CPI 2016 Focus:
The International Microelectronics Assembly and Packaging Society (IMAPS) will host an Advanced Technical Workshop in San Diego on CHIP-PACKAGE INTERACTIONS WITH FAN-OUT WAFER LEVEL PACKAGING on 6-7 April, 2016. Fan-out wafer level packaging is a rapidly growing segment of the semiconductor packaging industry. Miniaturized mobile and IOT applications are driving the need for thin, low cost packaging with high pincount to chip area ratio. As fan-out packaging is being extended to thinner and larger form factors and applied to 2.5D/3D system-in-package solutions, chip-packaging interactions (CPI) including warpage, mechanical and electrical stress effects, are potential barriers to wide scale adoption of this promising technology. This workshop will provide a venue for papers, poster sessions, and brainstorming discussions, bringing together product designers with the fan-out packaging supply chain to explore cost-effective solutions to the CPI challenges, including new materials, design techniques and EDA tools, and process flows and equipment.

Sessions are being planned in the following areas:

**Process Technologies**
- Effects of process technologies
- SIP
- Advanced Processes for enabling fan-out
- Scaling fan-out - issues and readiness
- Fan-out as 3D Packaging
- Approaches to “die-last” fab, packaging, or substrate
- Pushing RDL line width and space

**New Design/Materials**
- Material/process interaction
- Novel materials for enabling fan-out
- Molding compounds

**Quality & Reliability**
- Warpage effects
- Form Factor effects
- CMOS BEOL/FEOL effects
- Mechanical and Design reliability
- Fan-out in the Automotive world - reliability requirements
- Process control of fan-out - in-process through to test - assuring reliability
- Reliability in a SIP world

**Design Tools**
- EDA Tools and readiness for all different fan-out approaches
- Stress Aware Design

Please contact Brian Schieman by email at bschieman@imaps.org if you have questions.

www.imaps.org/cpi
Exhibit at IMAPS 2016!

49th International Symposium on Microelectronics
October 10-13, 2016

www.imaps2016.org
Exhibition - October 11-12, 2016
Pasadena Convention Center
Pasadena, California

Early Exhibit Deadline: March 31, 2016
For more information, please contact Brian Schieman at (412) 368-1621, bschieman@imaps.org or (919) 293-5000.
Epoxy Technology Inc. Announces 50 Years of Adhesive Excellence

Contact: Robin Dickie
Strategic Marketing Manager
Epoxy Technology, Inc.
+1 978-667-3805, x247

(Billerica, MA) – February 17, 2016 – Epoxy Technology Inc., a leading manufacturer of high performance specialty epoxy, UV and Hybrid adhesives, is celebrating 50 years of adhesive innovation and excellence. Since 1966, EPO-TEK® products have been synonymous with high performance and reliability. EPO-TEK adhesives are routinely specified by design engineers worldwide for critical assembly projects in a multitude of industries.

Epoxy Technology was founded in 1966 by Frank W. Kulesza. As a pioneer and visionary in the adhesive industry, Frank sought to replace eutectic solder in hybrid microelectronic assemblies with what, at the time, were truly new and innovative ideas. Combining his Chemical Engineering degree from Northeastern University with his practical knowledge and experience at IBM, Frank formulated some of the world’s best known and most relied upon epoxy adhesives, still in use all over the globe.

Joan Bramer, Global Sales and Marketing Director says, “Epoxy Technology Inc. is very proud of its 50 years of adhesive excellence; continuing to stay true to Frank’s original mission: to deliver novel, specialty adhesives to customers worldwide, with the added support of superior technical expertise and customer service. As we celebrate this important milestone, we are also very thankful to our many loyal customers who made this celebration possible.”

Today, our formulators continue Frank’s formulating legacy by providing state-of-the-art adhesive products, keeping in pace with the ever changing needs of our customers.

About Epoxy Technology

Epoxy Technology, Inc., founded in 1966, is a pioneer in the development of Specialty Epoxy, UV and UV Hybrid adhesives to meet the critical performance standards of high-tech industries worldwide. Through product innovation and high manufacturing standards, EPO-TEK® is a valued supply partner to advanced technology industries including semiconductor and microelectronics, medical devices, military, automotive, optical, solar and aerospace. EPO-TEK® is a registered trademark of Epoxy Technology, Inc.

For more information on any of Epoxy Technology products or our listing of authorized distributors, visit the website at: epotek.com or contact us directly at +1 978-667-3805.
Welcome New IMAPS Members!
November-December 2015

Individual Members
Scott Baik
Christian Barjolle
Ian Blanchflower
Guy Bonhomme
Sanae Boulay
Kevin Breney
Noa Browning
Ellen Ceweski
Agnes Chaillot
Ryan Chan
Chien Hsun Chen
Dennis Chen
Jen Chen
Tsung-Wen Chen
Ya-Shu Chen
Yen Cheng Chang
Jeanne Cirmal
Nicolas Degrenne
Chelladurai Devadoss
Ben Dillinger
Jean-Luc Diverchy
Jesse Dubrowsky
Fanda Fan
Wei-jean Fang
Konstantine Farah
Timothé Ferrara
Giovanni Flores
Laura Frisk
Shan Gao
David Garcia
Benoit Goral
Arndom Goswami
Sylvano Graziani
Steven Groothuis
Jean Guilbaud
Daniel Han
Scott Hao
Seren Herslund
David Hicks
Mei-Lin Hsieh
Chia-Ping Hsieh
Che Wei Hsu
Eddy Huang
Pei Chen Huang
Aria Isapour
Rahul Jain
Camilla Karnfelt
Sulman Khan
Kap Soo Kim
Rogun Kim
Xavier Le Goarer
Luc Le Herisse
Ringmin Lee
George Lee
Sheng-shian Li
Dounan Li
Johnson Liao
David Lin
Ken Lin
Wen Lin
Yan Yu Liu
Xavier Listwan
Hou Chun Liu
Hsing Ning Liu
Patrick Lu
Paul Lu
Shiang-Cheng Lu
Sinta Lu
Liam Macshane
Zichen Mao
Yamaoka Masafumi
Kashyap Mohan
Roberto Mrad
Elizabeth Nerdig
Zack Newton
Frederic Oudart
François Pacreau
Guru Pandian
Benjamin Rhea

Isaline Richard
Matthew Roberto
Sonya Roberts
Jean-François Savard
Christina Semikow
James Situ
Yaqin Song
Fabrice Souléfet
Jean-Charles Souriau
David Strecker
Joshua Stuckner
Jack Tang
Valerie Thomas
Bernard Trencoat
Mark Vanderwalde
Scott Wang
Frank Werner
Olivia Wilson
Nathan Woods
Scott Worthington
Shi-Jeh Wu
Avri Wyshogrod
Yasmine Yan
Nerow Yang
William Ye
Sachia Yu
Your IMAPS Member Benefits at Your Chapter Level

Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar

Arizona

The Arizona IMAPS chapter kicked off what is planned to be a busy 2016 calendar of events on January 14th with a luncheon presentation titled "Enabling a New Class: The Panel Level SoC" from Tim Olson, Founder and Chief Technology Officer of Deca Technologies.

Chapter officers put this event together in just a few weeks, so were pleased to have 60 attendees and 2 exhibitors. The high interest in fan-out wafer level package (FO-WLP) technology and quality of the presentation were key factors in proceeding with an event on short notice.

The Deca presentation demonstrated how FO-WLP has grown from a niche solution as a single die package with a limited supply chain into a hyper-growth technology delivering the industry’s highest interconnect density enabling multichip integration. With Moore’s Law slowing due to economic challenges, system on a chip (SoC) designers are now partitioning monolithic silicon devices into multi-chip architectures that require tight die-to-die spacing and ultra-high density interconnect. Fan-out technology is now emerging as a key enabler of these future multichip SoC devices. However, cost, capability, yield and scale must all come together to enable mass market adoption. To address the cost and scale challenges, Deca sees the transition from wafer to panel level processing as a critical factor for future SoC architectures.

As the attached chart illustrates, Deca is targeting panel level fan-out to approach 0.5 cents/sq mm which is closer to the benchmark an OEM pays for a printed circuit board assembly. Further a fan-out SoC architecture allows designers to partition functional blocks to reduce silicon (Si) fabrication costs by keeping analog circuits in lower cost analog wafer fabs further reducing SoC device costs.

February 18 was the next IMAPS AZ meeting with Bill McClean, President of IC Insights, whose presentation was titled "Are IC Industry Cycles Dead or Just Sleeping?" Following a downturn in the global semiconductor market last year our members are very interested in IC Insights forecast and assumptions for the 2016 IC market and what economic factors will drive the next cycle.

Although a high level of uncertainty still looms over the global economy, sales of smartphones continue to reach new highs and the Internet of Things looms on the horizon. IC Insights presented its forecast for the IC market and unit volume shipments in the context of the IC industry cycle model. In order to make sense out of the current turmoil, a top-down analysis of the IC market was given and included trends/correlation as shown below in worldwide GDP growth, IC growth, electronic system sales, and semiconductor industry capital spending and capacity.
Central Texas

The Central Texas Chapter of IMAPS had a very successful symposium on February 11, 2016 with 85 attendees.


Pizza and cookies were available to facilitate networking.

The next symposium is being planned for May 10, 2016.

IMAPS JOBS MarketPlace

Your IMAPS membership provides you with the on-line JOBS MarketPlace. This is a proactive, valuable, complimentary member service for both job seekers and prospective employers. Take advantage of it to find open positions or fulfill staffing needs.

IMAPS members can post unlimited job openings at no cost. Hiring managers can search for and view resumes of industry participants at no cost by using convenient sort criteria.

Member job seekers can post resumes and/or search for current openings at no cost. Job seekers can make their search even easier by setting up a job alert so compatible openings (by industry, location, and job function criteria) will be e-mailed as they are posted.

Find out more information at http://jobs.imaps.org/home
The International Microelectronics Assembly and Packaging Society (IMAPS) is organizing the 17th Symposium on Polymers for Microelectronics. The theme for the 17th Symposium on Polymers for microelectronics is Innovations Driving a Smart and Interconnected World and will continue the event’s focus on polymeric materials for microelectronic applications including traditional and new application areas. Traditional areas covered include stress buffer materials that have evolved from PSB to RDL to fan-out packaging applications for multilayer interconnect for 2D/3D packaging. Other materials to be discussed include substrates, including flex films and encapsulate materials as well as other polymeric materials used in electronics packaging. Applications spaces include wafer/IC packaging (including WSS adhesives and patterning), additive manufacturing, medical/IoT devices/packages as well as fundamental material and characterization and properties of new/critical materials and new processes that enhance performance and lower cost will also be covered.

The 2016 Symposium will also feature several keynote presentations, a panel discussion, and numerous networking opportunities.

Keynote Speakers

**Flexible Hybrid Electronics Manufacturing Technologies as the Foundation for a Connected World**  
Malcolm J. Thompson, Ph.D., Executive Director, Flexible Hybrid Electronics Manufacturing Innovation Institute / Chief Executive Officer, Nano-Bio Manufacturing Consortium / Chief Technology Advisor, FlexTech Alliance

**Changing Requirements for Thin Film Polymers in the Next Decade of Advanced Packaging**  
Michael Töpper, Business Unit Developer, Fraunhofer Institute for Reliability and Microintegration IZM

Sessions are being planned for the following:

**Front-End of Line Applications**
- Polyimide & Alternative Polymer Passivation (PSB and RDL)
- Semiconductor Applications, CMP Pads
- Low K Dielectric Materials
- Anti-Reflective/Multi-Layer Coatings
- Photosensitive Materials
- Sacrificial Materials / Temporary Bonding

**Packaging Applications**
- Wafer Bumping
- Encapsulation (Underfill and Epoxy Molding Compounds)
- Die Attach, Adhesive & Thermal Interface Materials
- Organic Substrate Materials & Advanced Laminates
- Fan-in (Wafer Scale) and Fan-out Packaging (Embedding and RDL)
- Multi-Chip Packaging Applications
- SIP & SoP
- 3D Integration / TSV

**Structure-Property Relationships & Characterization**
- Synthesis, Applications, Modification & Tailoring
- Polymeric Characterization & Testing
- Molecular Modeling

**Emerging & Novel Materials/Manufacturing/Applications**
- Medical Applications / Biosensors / Wearable Technologies
- Sensors / MEMS / Microfluidics
- Conductive & Ferroelectric Polymers
- Optoelectronic Packaging & Waveguides
- New Processing, Equipment & Metrology Technologies
- Display Technologies
- Flexible, Transparent, Printable, or Organic Electronics
- Photovoltaics
- Additive Manufacturing Materials and Processes

Please contact Brian Schieman by email at bschieman@imaps.org or by phone at 412-368-1621
Tuesday May 3rd, 2016

Holiday Inn, Boxborough, Massachusetts

2016 THEME: 3D & Beyond

Featuring

36 Papers  Cash Awards for Best Student Papers  On-Site Employment Center
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Sponsorship Opportunities  Buffet Luncheon  Games, Raffles & Prizes

Symposium Technical Chairs

Dmitry Marchenko, Microsemi DPG and Dr. Parshant Kumar, Draper

Keynote

A Trillion Sensors for Health Care
Dr. Ahmed Busnaina, Northeastern University
Director NSF Nanoscale Science and Engineering Center

Symposium Technical Team

3D and Beyond
Maria Durham, Indium and A.F.M. Anwar, UConn

RF & Microwave - Innovations and Emerging Technologies
Tom Terlizzi, GMS Systems and Dr. Tracey Vincent, CST

High Reliability Interconnects
Mike McKeown, Hesse Mechatronics and Bill Boyce

SMT and Electronics Packaging
Tina Barcley, TAS Consulting and Mike Martel, MMC Marketing

Printed Electronics
James Zunino III, AMRDEC and Katherine Duncan, AMRDEC

Medical Device Packaging
Steve LaFerriere, YOLE Development and Tom Green, TJ Green Associates LLC

Nanoelectronics and Optoelectronics Packaging
Dr. Alkim Akyurtlu, UML and Dr. Joey Mead, UML

Poster Session
Dr. Zhiyong Gu, UMass Lowell and Dr. Rita Mohanty, Enthone

For Complete Technical Program, Registration & Information visit www.imapsne.org
Questions on Exhibiting, Sponsoring or Anything Else
Contact Harvey Smith: harveys@imapsne.org or call 508-699-4767
International Conference on
High Temperature Electronics
(HiTÉC 2016)
May 10-12, 2016

Conference Events and Technical Program
May 10-12, 2016

Tabletop Exhibition
May 10-11, 2016

Albuquerque Marriott Pyramid North
Albuquerque, New Mexico - USA

Please join us in Albuquerque, New Mexico for HiTEC 2016. Companies wishing to sponsor this conference or exhibit, or individuals interested in submitting an abstract or getting involved as a session chair, please contact Brian Schieman at bschieman@imaps.org for more information.

HiTEC 2016 continues the tradition of providing the leading biennial conference dedicated to the advancement and dissemination of knowledge of the high temperature electronics industry. Under the organizational sponsorship of the International Microelectronics Assembly and Packaging Society, HiTEC 2016 will be the forum for presenting leading high temperature electronics research results and application requirements. It will also be an opportunity to network with colleagues from around the world working to advance high temperature electronics.

Papers will be presented on, but not limited to, the following subjects:

Applications:
- Geothermal
- Oil well logging
- Automotive
- Military/aerospace
- Space

Device Technologies:
- Si, SOI
- SiC
- Diamond
- GaN
- GaAs
- Contacts
- Dielectrics

MEMS and Sensors:
- Vibration
- Pressure
- Seismic

Packaging:
- Materials
- Processing
- Solders/Brazes
- PC Boards
- Wire Bonding
- Flip Chip
- Insulation
- Thermal management

Circuits:
- Analog
- Digital
- Power
- Wireless
- Optical

Energy Sources:
- Batteries
- Nuclear
- Fuel Cells

Passives:
- Resistors
- Inductors
- Capacitors
- Oscillators
- Connectors

Reliability:
- Failure mechanisms
- Experimental and modeling results

Early Registration/Exhibit & Hotel Deadline: April 13, 2016
www.imaps.org/hitec
UPDATES FROM IMAPS

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Assembly and Packaging Society
www.IMAPS.org

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- Participate in discussions through the Memberfuse Community website
- Maintain your professional listing

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Microelectronics Research Portal

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Free downloads included with membership
Visibility and searchability of your published work through leading search engines like Google Scholar

Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!
Join now!
IMAPS corporate memberships are designed to give your company a competitive advantage in the microelectronics packaging industry. Choose the right membership to meet your exhibition, advertising, discount registration needs and more.

<table>
<thead>
<tr>
<th>Membership package inclusions</th>
<th>Premier</th>
<th>Standard</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of employees who receive individual membership benefits:</strong></td>
<td>No limit to number of individual members with full online access; Up to 5 receive print magazine</td>
<td>2</td>
</tr>
<tr>
<td><strong>Access to IMAPSSource, the microelectronics research portal</strong></td>
<td>IP recognition allowing unlimited access for all computers in one network</td>
<td>150 downloads via two (2) selected member logins</td>
</tr>
<tr>
<td><strong>Press releases in Corporate Bulletin</strong></td>
<td>Up to 1 press release per bulletin (twice monthly)</td>
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<tr>
<td><strong>Member pricing for exhibitor events</strong></td>
<td>Included</td>
<td>Included</td>
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<tr>
<td><strong>JOBS Marketplace</strong></td>
<td>Complimentary job postings</td>
<td>Complimentary job postings</td>
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<tr>
<td><strong>Use of membership mailing list</strong></td>
<td>3x per year</td>
<td>1x per year</td>
</tr>
<tr>
<td><strong>IMAPS.org advertising</strong></td>
<td>Complimentary</td>
<td>Member discount</td>
</tr>
<tr>
<td><strong>Magazine advertising</strong></td>
<td>One 1/4 page ad included annually, plus 15% discount on any additional</td>
<td>15% discount</td>
</tr>
<tr>
<td><strong>Online Industry Guide</strong></td>
<td>Includes company listing, link to website, product and service categories</td>
<td>Includes company listing, link to website, product and service categories</td>
</tr>
<tr>
<td><strong>Global Business Council</strong></td>
<td>Membership included</td>
<td>Membership included</td>
</tr>
<tr>
<td><strong>Webinar Sponsorship</strong></td>
<td>30% discount</td>
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<tr>
<td><strong>Annual dues</strong></td>
<td>$2,500</td>
<td>$750</td>
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Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!
Premier Corporate Members

IMAPS has introduced a new level of support for corporate members. These companies have decided to participate in our Society at the Premier Corporate Member level. We are extremely grateful for their dedication to the furtherance of our educational opportunities and technological goals.
The International Microelectronics Assembly and Packaging Society (IMAPS) will host an Advanced Technical Workshop on ADDITIVE MANUFACTURING and PRINTED ELECTRONICS on June 20-21, 2016. Printing technology is expected to enable the evolution of electronics from rigid boards to products that are flexible, conformal or wearable. The Printed Electronics Conference will bring together experts to report on the progress and the challenges of this emerging field. This technology is expected to impact the options for integration of active and passive components and will exploit additive approaches to advance microelectronic packaging. Conference sessions will cover the development of printable electronic materials (inks), the options for manufacturing/printing and the applications of printed and flexible electronics.

Those wishing to present at the workshop must submit a 500+ word abstract electronically no later than MARCH 31, 2016, using the on-line submittal form at: www.imaps.org/abstracts.htm. Please contact Brian Schieman by email at bschieman@imaps.org or by phone at 412-368-1621 if you have questions. Full papers are not required. A post-conference download containing the presentation material as supplied by the presenter onsite will be distributed to all attendees. Speakers are required to pay a reduced registration fee.

The Microelectronics Foundation sponsors Student Paper Competitions in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Students submitting their work and identifying that “Yes, I’m a full-time student” on the abstract submission form, will automatically be considered for these competitions. The review committee will evaluate all student papers/posters and award a total of $1,000 to winning student(s). The selected student(s) must attend the event to present his or her work and receive the award. For more information on the student competition, go to www.microelectronicsfoundation.org.
## CHAPTER CONTACTS

<table>
<thead>
<tr>
<th>CHAPTER NAME</th>
<th>MEMBER NAME</th>
<th>E-MAIL</th>
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Advancing Microelectronics 2016 Editorial Schedule

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<td>May/Jun</td>
<td>Internet of Things</td>
<td>Mar. 8</td>
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<td>Jul/Aug</td>
<td>2016 Show Issue</td>
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<td>Sept/Oct</td>
<td>MEMS and Thermal Management</td>
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<tr>
<td>Nov/Dec</td>
<td>Ceramic: Thick &amp; Thin Film</td>
<td>Sep. 8</td>
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IMAPS Headquarters

Who to Call

Michael O’Donoghue, Executive Director, (919) 293-5000, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction, Exhibits, Meetings

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Ann Bell, Manager, Managing Editor, Advancing Microelectronics, (703) 860-5770, abell@imaps.org, Public Relations, Marketing, Fundraising, Advertising

Brianne Lamm, Membership & Events Manager, (919) 293-5000, blamm@imaps.org, Member Relations and Services Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support
<table>
<thead>
<tr>
<th>Date</th>
<th>Event Description</th>
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<tr>
<td>4-5-16</td>
<td>2016 RaMP Workshop and Tabletop Exhibition</td>
<td>San Diego, CA</td>
<td><a href="http://www.imaps.org/rt/">www.imaps.org/rt/</a></td>
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<td>4-6-16</td>
<td>Advanced Technology Workshop on Chip-Package Interactions with Fan-out Wafer Level Packaging 2016</td>
<td>San Diego, CA</td>
<td><a href="http://www.imaps.org/cpi/">www.imaps.org/cpi/</a></td>
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<td>4-19-16</td>
<td>IMAPS/ACerS 12th International Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT 2016)</td>
<td>Denver, CO</td>
<td><a href="http://www.imaps.org/ceramics/">www.imaps.org/ceramics/</a></td>
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<td>4-25-16</td>
<td>17th Symposium on Polymers for Microelectronics Innovations Driving a Smart and Interconnected World</td>
<td>Winterthur, DE</td>
<td><a href="http://www.imaps.org/polymers/">www.imaps.org/polymers/</a></td>
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<td>4-21-16</td>
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<td>5-10-16</td>
<td>International Conference on High Temperature Electronics (HiTEC 2016)</td>
<td>Albuquerque, NM</td>
<td><a href="http://www.imaps.org/hitec/">www.imaps.org/hitec/</a></td>
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<td>5-12-16</td>
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<td>6-20-16</td>
<td>Advanced Technology Workshop &amp; Tabletop Exhibits on Additive Manufacturing &amp; Printed Electronics</td>
<td>UMass Lowell Inn and Conference Center, Lowell, MA</td>
<td><a href="http://www.imaps.org/additive">www.imaps.org/additive</a></td>
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<td>6-21-16</td>
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<td>10-10-16</td>
<td>IMAPS 2016</td>
<td>Pasadena, CA</td>
<td><a href="http://www.imaps2016.org">www.imaps2016.org</a></td>
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