Exhibit at IMAPS 2016!

49th International Symposium on Microelectronics
October 10-13, 2016

Exhibit at IMAPS 2016!
Pasadena Convention Center
Pasadena, California

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Exhibition - October 11-12, 2016

For more information, please contact
Brian Schieman at (412) 368-1621, bschieman@imaps.org or (919) 293-5000.
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Matt Nowak
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Iris Labadie
Kyocera America
Secretary
Bill Ishii
Torrey Hills Technology
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Michael Gervais
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Directors
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Staff
Director of Programs
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Visit www.imaps.org for links to all upcoming events
Greetings IMAPS members and the worldwide microelectronics community!

It is a great pleasure to be serving as this year’s General Chair and I am blessed to have an excellent group of committee chairs supporting me. I am excited to share some of the great things that are planned for the IMAPS 49th Annual International Symposium on Microelectronics. I look forward to seeing you at the Pasadena Convention Center in Pasadena, CA from October 10th to 13th.

The IMAPS committees and many dedicated volunteers have been working together over the past six months to prepare for the 2016 Symposium with an emphasis on bringing exciting topics that are relevant within the microelectronics community. This year’s Technical Committee, chaired by Dan Krueger, is currently preparing technical sessions with topics ranging from high reliability systems to fan-out wafer level and embedded packages. The conference theme for IMAPS 2016 is “Packaging the Connected World.” Building on the successes of the previous symposia, the technical program in 2016 will also run parallel tracks covering Emerging Applications and the Connected World, 2.5/3D Packaging and Embedded Packaging Technologies, Advanced Packaging and Enabling Technologies, Advanced Materials and Processes, and Modeling, Design, Test and Reliability.

The Symposium team received very positive feedback regarding some of the program changes from last year, so we will continue with that momentum. A tour will be offered on Monday prior to the conference and will be open to all attendees who register prior to the event. The technical program will begin on Tuesday morning with three keynote speakers who you will not want to miss! These speakers offer insight on trends in high reliability packaging and the current state of the art. The technical team is continuing to refine the peer review process in order to provide the most benefit to authors and attendees for this event. Last year’s “posters and pizza” session was the most lively poster session in recent memory and was a great opportunity for all attendees to interact and get to speak directly with the authors on their research. We will continue to look for opportunities to offer the best technical program possible.

Complementing the technical sessions, we will continue to offer multiple Professional Development Courses (PDCs) with a variety of topics to enhance and broaden your technical portfolio. These will be held on Monday, October 10, prior to the kick-off of the technical sessions. The PDC committee and IMAPS leadership have been working together to incorporate your feedback, such as refreshing some of the course material and offering courses of various lengths.

Additional updates for this year include a change in format of the Global Business Forum. This will include a set of keynote presentations on Wednesday morning, which offers a better opportunity for all attendees to attend. The exhibit show returns with more than 100 exhibitors, and the symposium committee is driving to provide more time to engage with exhibitors without conflicting with the technical program.

Beyond the exhibit hall, technical sessions, keynote presentations, and professional development courses, look for other opportunities to get involved at the conference. IMAPS continues to provide a platform for college and university students to showcase their research and win valuable prize money, including travel grants for qualifying students. The IMAPS outreach to local high school students will include a tour of the exhibit hall floor. Please look for the students and engage them about the opportunities within our community. There are also plenty of occasions to connect with friends, both current and new, throughout the conference over coffee, lunch or at the opening reception. Be sure to download the IMAPS app so you can keep up with all the activities!

We will continue to incorporate your feedback, so please share your comments with any of the leadership before, during and after the conference. I thank you for taking the time to join us at IMAPS 2016 in Pasadena! I look forward to seeing you there!
I’m looking forward to the best ever International Symposium on Microelectronics with our 49th Annual event in October. Pasadena, California serves as a perfect backdrop for our Symposium this year with innovators in science and engineering at NASA’s Jet Propulsion Laboratory, California Institute of Technology, and many nearby technology companies driving our industry every day.

I’ve been honored to work with a great technical committee to put together an exceptional technical program following the theme “Packaging the Connected World.” This is an exciting time to be part of the microelectronics, assembly, and packaging supply chain as our world becomes more and more connected and integrated. Connectivity is changing our personal and industrial worlds and that is driving new and changing challenges and opportunities for the IMAPS community.

Our 2016 Symposium builds on the success of last year’s changes with an opening Plenary Session that includes 3 keynote speakers from well-known companies in the microelectronics community that create new needs and solutions in microelectronics, assembly, and packaging. The Posters and Pizza session was an overwhelming success at the 2015 Symposium and is being continued this year. Incorporating your feedback, we will have even more opportunities this year to engage in networking and exploring the exhibits while maintaining a high quality technical program with 5 parallel technical tracks. New this year will be two special invited sessions focusing on disruptive and game-changing technologies of Fan-Out Wafer Level Packaging and Medical Applications. The technical tracks are:

- Emerging Technology and the Connected World
- 2.5/3D Packaging and Embedded Packaging Technologies
- Advanced Packaging and Enabling Technologies
- Advanced Materials and Processes
- Modeling, Design, Test and Reliability

Thanks to all of you and to the Technical Committee for making the 49th Annual Symposium on Microelectronics the best ever! It’s been an honor and pleasure to work with my team to organize the technical program and I’m excited to see all of you in Pasadena, California.

Please keep sending your feedback and ideas for incorporation into this or future symposia and look for updates on the IMAPS website at www.imaps2016.org.

Mark your calendar now for October 10th through 13th and see you in Pasadena.
Line Coding Methods for High Speed Serial Links

Abdelaziz Goulahsen¹, Julien Saade², Frédéric Pétrot²
(1) STMicroelectronics, Grenoble, France
(2) TIMA Laboratory, CNRS, INPG, Joseph Fourier University, Grenoble, France
Email: Abdelaziz.goulahsen@st.com, Julien.saade@gmail.com, frederic.petrot@imag.fr

Abstract
A line coding for high speed serial transmission is defined by two major characteristics: the maximum guaranteed run length (RL) which is the number of consecutive identical bits, and the running disparity (RD or DC-Balance) which is the difference between the number of ‘zeroes’ and ‘ones’ in a frame. Both should be bounded to a certain limit, RL to ensure reliable clock recovery and RD to limit baseline wander.

Another important parameter is the overhead predictability. This parameter could be critical for applications that need a regular synchronization but for other application, especially if variable transfer rate is handled by the upper layer protocol, a statistical value of this parameter is good enough. In this paper, we propose two programmable line codings which bound RL and RD with fix or variable overhead. The resulting overhead for the line coding we propose shows to be the lowest between the existing methods, down to 10 times lower than famous encoding methods. The fix overhead line coding is based on a generalization of the polarity bit approach and could be dynamically adapted to link quality and environment. First we propose a line coding which bounds the RL, and then we propose another one which bounds the RD. We end up by combining both methods to build a DC-balanced and Run Length limited line coding.

Key words
running disparity, dc-balance, baseline wander, line coding, clock data recovery, polarity bit inverted

I. Overview on DC-Balanced Coding
Line coding applied on data before transmission could be split into two families: variable and fix overhead. In both cases, the line coding is characterized by two main parameters: a maximum RL to guarantee frequent transitions for Clock and Data Recovery (CDR) in asynchronous links, and a bounded RD (counted: +1 for a transmitted ‘1’ and -1 for a transmitted ‘0’) to reduce Baseline Wander (BLW) [1]. The smaller the RL and RD bounds, the lesser the constraints are on the CDR unit and on the filters. This helps in reducing the receiver’s complexity, power consumption, chip area and Bill Of Material.

Line coding usually comes at the cost of additional bits, for example, the 8b/10b encoding [2] which is widely used, adds 2 bits for every 8 bits resulting in 2/8 = 25% overhead while ensuring a maximum RL of 5, and a RD bounded to +/- 3 on bit level. The 64b/67b encoding which is used by the Interlaken’s protocol, ensures a maximum RL of 64 and a RD bounded to +/- 96 [3] at the cost of 4.68% of overhead. Table 1 summarizes the characteristics of some existing high speed links line coding methods.

In this paper we propose two methods which bound the RD at the desired value. A first method with very low overhead but not fully predictable in terms of overhead cost, and a second one with a predictable overhead but at a higher cost. Both methods exhibit a very low overhead compared to all existing solutions. We then show, in both cases, we can control the run length to end up with a controlled RD and RL line coding.

In paragraph II we overview the methods that were proposed to bound the RD, outline their advantages and drawbacks. In paragraphs III to VI we present our DC-balanced coding methods and the simulation results. In paragraph VII we combine the proposed methods with our RL’s limited coding. In paragraph VIII we compare the eye diagrams obtained by the different methods.

II. Overview on DC-Balanced Coding (RD)
Since the early days of data communication, DC-balanced codes have been used to counter the BLW effect which is generally caused by AC-coupling [1] and results in reducing the eye diagram opening. BLW can be also observed in DC-coupled devices as we show in the eye diagrams in [4].

In 1986, Knuth proposed a method [5] to construct frames with an equal number of 0s and 1s. Knuth proved that any binary sequence of a specific size could be balanced by inverting, at a specific bit position, all the rest of the sequence. The drawback of this method is that this particular bit position must be sent with the frame (and should be balanced as well) for the receiver to know how to reconstruct the original frame. This will add a relative important number of bits for small frames. For large frames, the number of added bits is less important, but the RD could reach high values inside the frame before going back to zero.

A low overhead method is the polarity-bit coding. It consists of adding 1 bit to a frame of a certain size to indicate whether it is inverted or not depending on the Cumulated RD (CRD) and the RD of the frame itself; i.e., if the CRD is positive, and the RD of the frame is positive as well, all the bits inside the frame will be inverted and the polarity bit will transmit the info to the receiver. This method is used by the 64b/67b encoding; 3 bits are added to the 64 bits of the frame: 2 bits (‘10b’ or ‘01b’) to ensure a transition and indicate whether the frame is raw data or control, and 1 polarity bit to indicate if the 64 bits are inverted or not. The CRD bounds ensured by such coding could be calculated according the worst case scenario as following:
\[ CRDbounds = \pm \frac{1}{2} (\text{FrameSize} + \frac{\text{FrameSize}}{2}) \]  

(1)

Which gives for the 64b/67b encoding \( CRDbounds = \pm 96 \) for a FrameSize = 64. The overhead cost for the CRD bound is 1/64 = 1.56%. The total overhead cost is 3/64 = 4.687%.

The 64b/66b, 128b/130b and 128b/132b encoding rely on scrambling-only for the 64 or 128 bits of the frame. As we show in [4], scrambling creates a sort of balancing between 0s and 1s, so on average it reduces the CRD. It does not, however, give bound guarantees, and could reach high values, as we can see in Figure 1. The advantage of scrambling is that it does not add any extra bits, so it has no overhead.

Recently, a method that bounds the RD was presented in [6] at 0% overhead. But this method can ensure the bounds only when the data is constant or idle.

In the following section, we will introduce two new methods which bound the Running Disparity to the desired limit with a very low overhead, down to 10x lower than existing encodings in both predictable and non-predictable overhead.

<table>
<thead>
<tr>
<th>Line Coding</th>
<th>Standards</th>
<th>RL bound</th>
<th>RD Bound</th>
<th>Overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>8b/10b</td>
<td>PCIe 2.0, USB 3.0</td>
<td>5</td>
<td>+/- 3</td>
<td>25.6%</td>
</tr>
<tr>
<td>TDMs</td>
<td>HDMI (1)</td>
<td>+/- 20</td>
<td>+/- 20</td>
<td>25%</td>
</tr>
<tr>
<td>64b/66b</td>
<td>10G Ethernet</td>
<td>64</td>
<td>N/A</td>
<td>3.125%</td>
</tr>
<tr>
<td>64b/67b</td>
<td>Interlaken</td>
<td>64</td>
<td>+/- 96</td>
<td>4.687%</td>
</tr>
<tr>
<td>128b/130b</td>
<td>PCIe 3.0</td>
<td>128</td>
<td>N/A</td>
<td>1.562%</td>
</tr>
<tr>
<td>128b/132b</td>
<td>USB 3.1</td>
<td>128</td>
<td>N/A</td>
<td>1.562%</td>
</tr>
</tbody>
</table>

Table 1. Summary of some existing line coding

(1) Clock forwarded

III. Novel Method to Bound the Running Disparity Using Aperiodic Polarity Bit Insertion

The proposed method consists on calculating the CRD bit-by-bit and when the CRD reaches a positive or negative Threshold \( T \), the RD of the next packet of Size 'S' bits is checked to see if they should be inverted or not. A bit will be added after the S bits to indicate if they were inverted or not. Only when \( RD(S) = 0 \), there will be no bit added. The programming should be done according to the following logic:

- If \( CRD = +T \) and \( RD(S) = 0 \), the S bits will be inverted and no bit will be added. The receiver will know when \( RD(S) = 0 \) that the bits were not inverted by default.
- If \( CRD = -T \) and \( RD(S) > 0 \), the S bits will not be inverted and a '0' bit will indicate it to the receiver.
- If \( CRD = -T \) and \( RD(S) < 0 \), the S bits will be inverted and a '1' bit will be added to indicate it to the receiver.

This logic allows the receiver to recover the data. Figure 2 illustrates the Transmitter and an example. S bits should always be buffered and RD(S) is calculated permanently. The values of \( T \) and \( S \) should be agreed on by the transmitter and the receiver before the start of transmission and could be adjusted to the link quality and environment.

The CRD bounds ensured by our proposal are defined by:

\[ CRD\text{bounds} = \pm (T + S/2) \]  

(2)

Two conditions should be respected to ensure the bounds mentioned in equation (2):

- \( T > S/2 \)
- \( S \) is even

IV. Simulation Result for Aperiodic Polarity Bit Insertion

In Figure 6, we plot in red the CRD of a random frame of 200 Kbits scrambled, and then we apply our proposed balanced encoding for \( T = 64 \) and \( S = 64 \). The CRD for the balanced frame is shown in green. We can see that the CRD never exceeds +/- 96. The encoding we propose could be applied without scrambling, but scrambling is recommended to reduce the CRD of the initial frame, limit the CRD excursion and thereby reduce the overhead (the added aperiodic polarity bits).

![Figure 2: a. Proposed DC-balancer's block diagram; b. encoding example.](image1)

![Figure 3: Scrambled data's CRD before and after applying the proposed DC balance.](image2)

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The following figure shows an example of scrambled data’s CRD before and after applying the proposed DC balancer with T = 64 and S = 64 (CRD bound = +/-96).

Overhead estimation of the proposal

OH=added_bits / Raw_bits  

To estimate the overhead (OH) resulting from our coding, we generate random frames on Matlab, scramble them with the same scrambling polynomial mentioned in Figure 1, and then apply our line coding. The overhead is shown in Figure 4 and Table 2, and it is calculated according to equation (3) based on the simulation of 200 frames of 400 Kbits each. Averaging is then made.

Table 2. Overhead examples of the proposed method

<table>
<thead>
<tr>
<th>T</th>
<th>S</th>
<th>CRD bounds</th>
<th>Overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>2</td>
<td>+/-3</td>
<td>14.27%</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>+/-4</td>
<td>9.05%</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>+/-5</td>
<td>6.6%</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>+/-6</td>
<td>5.32%</td>
</tr>
<tr>
<td>6</td>
<td>16</td>
<td>+/-12</td>
<td>2.05%</td>
</tr>
<tr>
<td>16</td>
<td>32</td>
<td>+/-24</td>
<td>0.8%</td>
</tr>
<tr>
<td>32</td>
<td>64</td>
<td>+/-48</td>
<td>0.31%</td>
</tr>
<tr>
<td>64</td>
<td>64</td>
<td>+/-96</td>
<td>0.11%</td>
</tr>
</tbody>
</table>

Figure 4. Proposal’s overhead compared to 8b10b encoding and Interlaken’s protocol.

Table 2. Overhead examples of the proposed method

As we can see, the overhead due to our proposal is very advantageous compared to other encodings. For a CRD bounded to +/- 3, we have more than 10% overhead reduction compared to 8b10b. If we release the constraints of the CRD we can bound the CRD to low values with only few percent of overhead or even less than 1%. Compared to the Interlaken protocol which adds 1.56% to bound the CRD to +/-96, we can obtain the same bound with only 0.11% overhead which is more than 10x lower.

This method also bounds the Run Length to 2^CRD-bound. i.e., if we bound the CRD to +/-3, the RL will be automatically bounded to 6 because the worst case RL will be when going from a CRD of -3 to a CRD of +3.

We shall note that based on the frame’s 1s and 0s distribution, the overhead estimations for our proposal could be increased if scrambling is not applied, that’s why scrambling is recommended to minimize the overhead.

V. Novel Method to Bound the Running Disparity Using Periodic Polarity Bit Insertion

As defined in the overview, a periodic or aperiodic polarity bit insertion method relies on scrambled data. As also shown in Figure 1, the CRD of a scrambled data is not bounded at all only statistically reduced on a large window time.

In order to overcome this issue we use the probabilistic representation of the random logic. This representation has been used in [7] to obtain a target probability on the output of a system given the probability of the input.

Scrambled data is defined as a system where the output probability of having a “0” (P(0)) should be around 0.5 (0≤P(0)≤1) whatever the input’s probability value.

We first define the output probability for the simple logic gate by the following equation:

Inverter: P(Z=1) = 1-P(A=1)  
And: P(Z=1) = P(A=1)*P(B=1)  
P is the probability, A and B are inputs, and Z is the output.

This equation should be interpreted as follows: for the inverter: the probability of having a “1” on the output is equal to 1 minus the probability of having a “1” on the input.

Using the equations (4) to (6) we can write the XOR equation.


Using (4)+(7) we can deduct the equation for the NXOR as follows:

NXOR: P(Z=1) = 1 - P(A=1) * (1-P(B=1))+(1-P(A=1)) * P(B=1) - (P(A=1) * (1-P(B=1)) * (1-P(A=1)) *P(B=1)) (8)

The following figure shows the 3D representation of the equation (7) and (8):

Figure 5. XOR and NXOR output probability in function of the input probability.

We can notice on both curves that if one of the inputs is around 0.5 the output probability will be around 0.5 whatever the probability of the second input is. Using a simplified “fix point iteration” or fixing one of the inputs to the output (delayed) we get the following curve.

Figure 6. XOR and NXOR output probability in function of the input probability with one input connected to the delayed output.

In this curve we have excluded the 2 singularities which will be treated in the simulation section.

We now see that if one input is connected to the output whatever the second input probability value is, we will have an output probability in the range of 0.4 and 0.6 depending if we use a XOR or NXOR output. We have put
in place the needed tool to define the polarity bit implementation. Using \( P(A) \) as the message probability from 0 to 1 as not predictable, we have an output probability in the range of 0.4 to 0.6 using either the XOR or NXOR output. The choice should be made in order to always minimize the CRD. This choice (polarity bit) will be always added to the message. The disparity bound will be defined by the size of this message and could be computed by the equation (1).

Figure 7 shows a simplified implementation example.

**VI. Simulation Result for Periodic Polarity Bit**

Unlike the aperiodic polarity bit insertion, this method gives a fixed overhead versus the data processed. The overhead is given by the equation (3) with \( \text{Raw}_\text{bits}=\text{message size and added}_\text{bits}=1. \)

Thanks to this particular scrambling, the average CRD is much lower than the maximum bound. Table 3 gives the theoretical bound and simulated values, over 50e6 bits.

<table>
<thead>
<tr>
<th>(Msg (bit))</th>
<th>CRD bounds</th>
<th>Simulated CRD (5e6Bits)</th>
<th>Overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>+/- 24</td>
<td>+/-/19</td>
<td>6.2 %</td>
</tr>
<tr>
<td>32</td>
<td>+/- 48</td>
<td>+/-/24</td>
<td>3.1 %</td>
</tr>
<tr>
<td>64</td>
<td>+/- 96</td>
<td>+/-/33</td>
<td>1.5 %</td>
</tr>
<tr>
<td>128</td>
<td>+/- 192</td>
<td>+/-/47</td>
<td>0.8 %</td>
</tr>
</tbody>
</table>

Table 3. Overhead for periodic polarity bit

Using a Markov chain model for this particular scrambling method, we can estimate the time occurrence when the maximum bound is reached. Figure 8 gives this estimation.

We have mentioned that two singularities exist. This occurs when the message is constant. This repetitive message will radiate some peaks of fix frequency during the transfer. In this case the method still works but EMI and coexistence issues will occur. This case is shown in Figure 9.

To overcome this issue, the input message should be combined with a variable and predictable data. Variable for whitening the signal and predictable to have the receiver (Rx) and the transmitter (Tx) synchronized. A very simple way to do it is to use a shift register and xor the message before the processing in Rx and Tx side. The following figure shows the EMI mitigation using a simple shift register with an unbalanced RD in it.

**VII. Low Overhead RL limited Line Coding**

**Method to bound the Run Length**

In a previous article [4] we made a proposal based on scrambling followed bit stuffing, plus a method to reduce the EMI (Electro-Magnetic Interferences). Bit Stuffing (BS) consists on adding an inverted bit after \( N \) consecutive identical bits: i.e., if \( N = 5 \), whenever a run of 5 consecutive 1s is detected, the transmitter will add a ‘0’ bit after this run whatever comes next, creating a transition in at least 5 bits window. The receiver will benefit from this transition to recover the clock. It will then delete the added bit. The drawback of BS, when applied on raw data, is that the overhead could be significantly high. But in [4], we showed that if scrambling is applied prior to BS, the BS overhead decrease. The following table gives the overhead for different RL when scrambling is applied.

<table>
<thead>
<tr>
<th>RL bound</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>OH (%)</td>
<td>16.65</td>
<td>7.13</td>
<td>3.33</td>
<td>1.61</td>
<td>0.79</td>
<td>0.39</td>
<td>0.19</td>
<td>0.09</td>
</tr>
</tbody>
</table>

Table 4. Bit stuffing overhead for different values of RL

Combining controlled RD and RL.

We now need to combine both methods: the one that limits the RD (based on periodic or aperiodic polarity bit insertion), the other (BS) that bounds the RL. Analysis shows that if the two methods are put together, one will disrupt the other: i.e., if the balancing is applied after BS, the BS will be disrupted due to bit inversion and the result will be more consecutive bits than the BS has ensured. If BS is applied after balancing, balancing will be disrupted by the BS. For example, if the BS adds more 1s than 0s, the RD will end up diverging.

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One way to make both methods work together is to process the running disparity balancing by one of the previous methods described then apply a modified bit stuffing (MBS).

Instead of adding a ‘0’ bit after N consecutive 1s or a ‘1’ bit after N consecutive 0s, we will add ‘01’ after N consecutive 1s and ‘10’ after N consecutive 0s. The balancing will not be disrupted because the added RD is zero.

If we consider a pattern that has been balanced to a bound of +/-12, when we apply the modified bit stuffing for N = 5, the CRD bound won’t change, even not by 1 unit. To exceed the limit of the CRD to +13 for example, we should have a CRD to +12 and then do the MBS by adding ‘10’ so that the CRD can go to +13 when we add the ‘1’ bit. However, to have a CRD to +12 and MBS by ‘10’, it should happen with 5 consecutive 0s. In this case, it is impossible to have a CRD at +12. Thereby, the MBS will not change the CRD bounds of the balancing.

The Total Overhead (TO) of the RL limited and DC-Balanced Line Coding could be given by the following equation:

\[ TO = BO + MBSO \]

Where \( BO \) = Balancing’s Overhead and \( MBSO \) = Modified Bit Stuffing’s Overhead

VIII. Eye Diagrams Simulation

To compare the performance of the proposed line coding and to make a comparison with 8b/10b encoding and scrambling, we plot in Figure 11, using Simulink, the eye diagrams using the S-parameters of a DC-coupled PCB (Printed Circuit Board) long channel. At 10 GHz, we can see that Scrambling’s eye is the most closed, and when we bound the RD with our proposal to +/-3 and RL bound to 5, we clearly see a better opening. It is very similar to 8b10b encoding because of the same bounds.

For a 10 GHz frequency, the real throughput using 8b/10b encoding is 8 Gbit/s \((10^{-10} \times 25\% = 8)\). To have an equivalent throughput, the frequency of the link using our encoding should be 9.4 GHz \((8 \times 8 \times 17.4\% = 9.4)\) according to Figure 11.

The eye diagram is shown in Figure 11 and we can see that it has a much better opening than with 8b/10b encoding at the equivalent throughput.

<table>
<thead>
<tr>
<th>TO</th>
<th>BO</th>
<th>RL Bound</th>
<th>MBSO</th>
<th>(Total Overhead)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>2</td>
<td>+/3</td>
<td>14.27%</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>+/4</td>
<td>9.05</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>+/6</td>
<td>5.32</td>
<td>5</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>+/10</td>
<td>2.66</td>
<td>10</td>
</tr>
<tr>
<td>15</td>
<td>10</td>
<td>+/20</td>
<td>1.03</td>
<td>8</td>
</tr>
<tr>
<td>64</td>
<td>64</td>
<td>+/-96</td>
<td>0.11</td>
<td>7</td>
</tr>
</tbody>
</table>

Table 5. Overhead breakdown for aperiodic polarity bit insertion

Conclusion

In this paper, we presented two novel line codings that bound the RD with a very low overhead and show how a modified bit stuffing could be used to bound the RL. These line codings are targeting two types of application:

• Variable data rate transfer: the variation is directly proportional to the parameter used and at most in order of few percent of the total bandwidth.
• Fixed rate data transfer: where the overhead is a little bit bigger than the previous proposition but still remain in the order of few percent.

The choice could be made based on the final application. Typically for video where the blanking position is important, the periodic polarity bit insertion fits better whereas for servers, the aperiodic polarity bit insertion should be preferred.

Our low overhead line codings enables many advantages; either to have better throughput efficiency for a specific link frequency, or to have lower frequency at a fixed target throughput. Lower frequency means better eye opening, lower noise and lower power consumption.

References


Any questions regarding this paper should be addressed to the authors.
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Modeling, Design, Fabrication, and Characterization of Ultra-High Bandwidth 3D Glass Photonic Substrates

Bruce Chou, William Vis, Ryuta Furuya+, Venky Sundaram and Rao Tummala, Georgia Institute of Technology

+Ushio Incorporated, 813 Ferst Drive NW, Atlanta, GA 30332 USA
Ph: 352-359-3182, cchou36@gatech.edu

I. Introduction

With the continuously increasing bandwidth demand for IP traffic, the traffic at data centers is expected to reach 400 Gbps by 2020 [1]. Cost-effective and lower power optoelectronic packaging is an important enabling technology to meet this bandwidth demand. The 3D Glass Photonics (3DGP) interposer technology has been developed in the past to demonstrate an ultra-high bandwidth optical transceiver module at low power and potentially lower cost than silicon interposers [2], [3]. Glass substrates offer compelling advantages over silicon and organic substrates for optoelectronics packaging, namely: ultra-low loss electrical and optical material properties, a dimensional stability that enables micron level precision alignment across panel, thermal isolation capability for precise control of laser temperature, and a low cost panel-level double sided processing capability [4], [5].

The two biggest challenges in achieving cost-effective 3D glass photonic packages are: (1) the sub-um alignment requirement of single mode fibers (SMF); and (2) the high coupling loss due to mode-mismatch between SMF and the Photonic IC (PIC). The optical loss from direct coupling from a SMF to PIC edge can be as high as ~20dB due to the large mode mismatch between the silicon WG (~0.2 μm²) on die and the SMF core (>50 μm²). Two primary coupling mechanisms have been explored to overcome the mismatch: in-plane coupling; and out-of-plane vertical coupling.

In-plane, or edge, coupling using inverse taper WGs has been demonstrated, with a reported coupling loss of 0.5 dB on silicon substrates [6]. Out-of-plane vertical grating coupled directly to angled polished fibers, either vertically or horizontally, was demonstrated with coupling losses less than 2 dB [7], [8]. However, in order to achieve the desired coupling loss, active fiber alignment with a tight tilt and roll was necessary.

In this paper, we propose and demonstrate a novel out-of-plane turning structure in thin glass substrates to overcome the high cost involved in achieving the precise alignment of the fiber, as shown in Figure 1. Similar structures have been demonstrated in the past using Silicon and glass interposers [9], [10]. However, this paper presents several key innovations in the glass photonic package structure beyond previously published research. In this method, a planar optical waveguide (WG) with turning mirror is first fabricated on glass using moving mask lithography. A 90 degree cleaved fiber is then planar-aligned to the glass interposer using u-grooves formed on glass. The PICs are flip-chip bonded on the other side of the glass interposer, thus allowing light to travel from PICs to SMF through the glass interposer. The precision alignment of PIC is achieved through the self-aligned reflow of solder on copper pillars. In this paper, we present the modeling of the optical coupling from PIC to SMF using Finite Difference Time Domain (FDTD) method.

Abstract

This paper presents the modeling, design, fabrication, and characterization of ultra-low loss 3D optical waveguides integrated on a glass photonic substrate. A novel, single-step process was developed using moving mask lithography to fabricate a single mode optical waveguide with a built-in turning mirror capable of making 40° or 45° turns for vertical grating couplers or photodetectors, respectively. Planar alignment of the waveguide to fiber interfaces enable passive alignment, contributing to system cost reduction. An optical path with 1.1 dB loss from fiber to die was obtained from optical modeling, while the fabrication of single mode waveguides with built-in mirrors at <1° angular control was demonstrated.

Key words

Finite Difference Time Domain (FDTD) method, glass interposer, moving mask lithography, optical waveguides, optoelectronic packaging, single mode fiber
followed by the design and fabrication of waveguides on glass photonic substrates.

II. Modeling

Single Mode Condition

The core and cladding materials of the optical waveguides are chosen based on closely matched refractive indices and compatible processing conditions. For moving mask lithography, a positive toned optical polymer is desirable because of its linear profile with respect to exposure dosage. Hence, Cyclotene 6505 photo-definable polymer, which has a positive tone, was selected. This material also has a relatively high refractive index $n_1 = 1.56$ at C-band ($\lambda = 1550$ nm) and a capability to achieve 2–3 um resolution [11]. The lower cladding material was the glass substrate, specifically SGW3, supplied by Corning Inc., which has $n_2 = 1.49$ at $\lambda = 1550$ nm. The upper cladding material chosen was a dry-film equivalent of Cyclotene 4024 photo-definable polymer with a desirable refractive index $n_3 = 1.543$ at $\lambda = 1550$ nm. The single mode (SM) condition for the rectangular waveguide cross-section shown in Figure 2(a) was obtained by a mode solver. In this paper, an FDTD based solver from Optiwave Systems Inc., was used for the optical modeling. The variation of width ($w$) versus height ($h$) for single mode condition is plotted in Figure 2(b). In order to achieve the largest cross-sectional area, a 5 um x 4 um WG was chosen.

Turning Mirror

Taking advantage of the optical transparency of glass substrates, the turning mirrors were built on optical waveguides utilizing Total Internal Reflection of the polymer-air interface which can achieve a high efficiency optical turning without surface metallization. OptoFDTD, from Optiwave, was used to determine the turning efficiency of 40° and 45° turning structures. The 40° turning provides a 10° offset to turned signals which matches the incident angle needed to achieve the maximum efficiency for the vertical grating coupler (VGC) on the PIC. On the other hand, the 45° turning is the standard used for photodetectors (PDs) and Vertical Cavity Surface Emitting Lasers (VCSELs). The result was measured at a distance of $t = 10$ um away from the mirror because of the limitations in the computational resources. The height of waveguide, $h$, was 4 um as determined in the previous section. The resulting turning loss was 0.61 dB and 0.9 dB for the structures shown in Figure 3(a) and (b), respectively. A sweep across the turning angles showed that the +0.5 dB tolerance could be achieved with a ±2° precision for the structure shown in Figure 3(a), and ±1.4° for the one in Figure 3(b). The higher loss observed in Figure 3(b) occurred because of the visible wave leaking at the end of the turning mirror.

III. Design

The design of the novel waveguides with integrated turning structure combined the 2-D tapering to achieve better misalignment tolerance and the out-of-plane turning at the end of the waveguide to reduce mode mismatch. For simplicity, a linear taper was chosen. The design assumed that the moving mask lithography would allow single step fabrication of the core structure. The photo defined cladding was applied after soft cure of the core layer to ensure single mode operation in the wave guiding region and total internal reflection in the out-of-plane turning region. The end face was formed by dicing to allow butt coupling to single mode fibers, as illustrated in Figure 4. The design parameters used were $h = 4$ um, $w_1 = 9$ um, $w_2 = 5$ um, $l = 50$ um. 2D FDTD simulation of the waveguide structure was performed with signal launching from SMF, with $\Delta x = \Delta y = 0$ um, and $\Delta z = 5$ um. The resulting coupling loss was found to be 1.01 dB at the bottom of glass substrate, as shown in Figure 5.
To verify the improved alignment tolerance of the tapered waveguide structure, a 3D sensitivity analysis of Δx, Δy, and Δz offset was performed. The results are shown in Figure 6. For a 1dB range, the needed tolerance was ± 1.5 um for x and y, while for z it had a much higher value of 30 um. Therefore, sub-um accuracy is not required in the proposed method.

The above equation is the basis for the moving mask lithography described and demonstrated below.

Moving Mask Lithography

Moving mask lithography is a planar lithography technique that generates an oblique structure by horizontal mask translation during exposure [12]. The mask translation corresponds to a gradient exposure dose experienced by the polymer in the direction of translation. Given that the polymer had a linear development profile with respect to exposure dose, the polymer was expected to have an oblique structure upon development, closely matching the input translation. Figure 8(a) illustrates how an input translation results in an oblique structure. In practice, the moving mask method requires precise control of the exposure tool, in both the velocity of mask movement and the UV dosage, as shown in Figure 8(b). Hence, the UX-44101 mask aligner from Ushio, which has the capability to implement moving mask, was used.

To adjust the angle of the end of the waveguide, the minimum dose needed for the waveguide height was calculated using equation (1), then the horizontal traveling distance required was calculated by dividing the tangent of the angle to the waveguide height. Then the stage was programmed to move for the right amount of time to achieve a linear distribution of dose versus distance traveled. To achieve 40° entry and exit turning waveguides, an exposure with a dose ranging from zero to 350 mJ/cm² was performed over a translation distance of 6 um. To achieve 45° entry and exit turning, an exposure with a dose of 400 mJ/cm² was performed over a translation distance of 5 um.

To demonstrate this concept, 4.5 um of Cyclotene 6505 was spin coated and soft baked as described in Section IV.A. However, for this case, exposure was performed using the translation profile described above. The curing was done in a nitrogen oven, following the standard Cyclotene procedure of ramping from room temperature and holding for 15 minutes at 130 C, then further ramping and holding for 1 hour at 200 C. The results for the associated input translations are shown in Figure 9.
The resulting oblique structures were measured to be 39 and 44 degrees using SEM which matches closely to the targeted angles of 40 and 45 degrees, which was modeled in Section II.B to incur additional losses of less than 0.5 dB. Smooth sidewalls were achieved through slight reflow during curing and are helpful in ensuring low optical loss. However, visible concaveness was observed for both cases, which can occur because of the non-linear behavior of the polymer at low dose or improper curing.

**Single Ended Turning by Moving Mask Method**

Two options are available to achieve the fiber coupling at the end faces as shown in Figure 4: (a) dicing followed by edge polishing; or (b) a modification to the moving mask lithography. Dicing at waveguide edge introduces a fiber integration challenge, as fiber alignment structures such as V-grooves and U-grooves cannot be used. On the other hand, a modified moving mask method is compatible with grooves, and it does not require any additional process steps.

The modified moving mask lithography was implemented by adding a steady exposure after the completion of the moving exposure, thereby fully exposing one end of the waveguide structure. Initial results from the implementation of such a method are shown in Figure 10. While 45° facets were achieved on the turning end, the sidewall angle was not near 90° on the straight end, and measured close to 70°. During prior experiments, it was noted that Cyclotene 6505 could not achieve 90° sidewalls, as shown in Figure 7(b). With proper exposure, development, and cure, an 80° sidewall angle was achieved. However, the intrinsic behavior of the positive-toned photopolymer limited straighter sidewalls. Therefore, the effects of sidewall angle on coupling losses involved in optical fiber to waveguide transition, needed to be studied by optical modeling.

In order to model the effect of sidewall angle on coupling loss in 2D FDTD, the same setup as in Figure 4 was used, except for the fact that now $\theta_s$, the sidewall angle, was a variable. The result, shown in Figure 11, showed an unexpected dip for the coupling loss at 80° sidewall angles. Analytically, the coupling loss is a combination of mode mismatch loss and the reflection due to sidewall angle as predicted by Snell’s law. The mode mismatch loss was 0.38 dB, and it was due to the fact that the output (optical waveguide) had a smaller cross-sectional area than the input (optical fiber). The change in sidewall angle resulted in consistent increase in coupling losses, to about 0.4 dB in addition to mode mismatch loss at $\theta_s$. 

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**Figure 8.** Input translation (time vs. movement) corresponding a gradient exposure intensity (received dose vs. distance) resulting in an oblique structure (resulting WG height vs. distance), and actual implementation of moving mask lithography.

**Figure 9.** Turning single mode waveguides: (a) 40°; and (b) 45°.

**Figure 10.** One-sided turning single mode waveguides with 45° on the turning end and 70° on the straight end.

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continued on page 16
continued from page 15

= 70°. The dip at $\theta = 80°$, upon reviewing the simulated electric field, was a result of the focused cavity formed between the fiber and the waveguide at the specific angle. Therefore, the dip is repeatable with the same sidewall angle and a well-controlled $\Delta z$. A sidewall angle of $80°$ will reduce the additional loss to 0.1 dB, which makes it critical to pursue further optimization of the sidewall angle.

![Coupling loss vs sidewall angle](image)

**Figure 11.** 2D FDTD simulation of fiber to waveguide coupling loss with respect to sidewall angle of waveguide.

### V. Conclusion

In this paper, a 3D waveguide structure on thin glass substrates was proposed and demonstrated to overcome two of the biggest challenges in cost effective optoelectronic packaging, namely: sub-um alignment tolerance and high fiber coupling loss. The novel single-step process for single mode waveguide cores, along with the cladding, showed a 1.01 dB coupling loss. The alignment tolerance to reach 1dB coupling loss was found to be $\pm 1.5$ um for $x$ and $y$, and 30 um for $z$, a significant improvement from the usual sub-um tolerance levels. The fabrication of the single-step process was realized using moving mask lithography on photo-definable Cyclotene 6505 polymers provided by Dow Chemical. This modified fabrication process achieved both symmetrical and asymmetrical turning on waveguides. Also, a turning angle control of 1 degree was achieved. Further process optimization is needed to improve sidewall angle, and optical characterization is needed to verify the simulation results.

### Acknowledgment

The authors would like to thank Fuhan Liu and Daniel Guidotti for their technical guidance on the design and fabrication of the waveguide structures on glass. Also, the authors would like to thank Dow Chemical for providing the experimental optical polymer materials.

### References

Pasadena Facts

Founding
A severe Indiana winter during 1872-73 prompted a group of friends from Indianapolis to form an investment group with the purpose of moving to the warmer climate of Southern California. Sent to scout the area, D. M. Berry recommended purchasing a portion of the Rancho San Pasqual, which later became Pasadena.

Incorporation
One of the main reasons Pasadena was incorporated in 1886 was to abolish saloons and the sale of alcohol in the area. In February 1887, an ordinance was passed that banned liquor in Pasadena.

Name
The word Pasadena literally means “valley” in the Ojibwa (Chippewa) Indian language, but it has been interpreted to mean “Crown of the Valley” and “Key of the Valley,” hence the adoption of both the crown and the key in the official city seal.

Namesakes
Pasadena, Texas was named after Pasadena, California because some thought that the areas resembled each other.

An asteroid was given the name Pasadena in 1980, in part because it is a middle-sized “suburban” asteroid eight miles (13 kilometers) in diameter.

The USS Pasadena SSN-752, a nuclear submarine, is the third Navy vessel and first submarine to carry the name of Pasadena. Commissioned in 1989, the submarine has been deployed several times, including the Persian Gulf in 1993. Currently based in Pearl Harbor, the football field sized sub is known for its speed and stealth, as well as its advanced sonar capabilities and weaponry systems. The USS Pasadena was awarded the Submarine Squadron Seven Battle “E” Efficiency award for 1998. The sub’s insignia was originally designed by Walt Disney for the USS Pasadena (CL-65), a light cruiser that earned six battle stars during WW2, represented by the boxing turtle. The red rose ties the ship to the City of Pasadena. More information about the USS Pasadena can be found on the Navy’s web site or the USS Pasadena Foundation.

Official Flower
The rose (no particular variety) was adopted as Pasadena’s official flower on September 22, 1961.

Parrots
Naturalized parrots are frequently seen and heard around Pasadena. According to local legend, many were released during a 1959 fire which destroyed Simpson’s Gardenland and Bird Farm in Pasadena. Some of the parrots were probably pets that escaped or were set free. Some may have been released by smugglers attempting to avoid arrest. One common breed is the red-crowned parrot.

Rose Bowl
The Rose Bowl was constructed in 1922 on the site of a dump in the Arroyo Seco. It originally had a seating capacity of 57,000 and currently seats 100,184 people. The rim circumference is 2,430 feet (741 meters); 880 feet (268 meters) from the north to the south rim and 79,156 square feet (7,354 sq. meters) with a circumference of 1,350 feet (411 meters). The Rose Bowl is home to the UCLA Bruins football team.

Tournament of Roses
The Tournament of Roses annual parade of flower-covered floats has been held in Pasadena since January 1, 1890. It was patterned after a European festival of roses and was meant to show off Pasadena’s natural beauty and sunny climate while most of the nation lay buried beneath snow. Today, the 5.5 mile (8.8 kilometers) Tournament of Roses parade has magnificent floral floats, marching bands, equestrian units and public officials. Floats must be completely covered with flowers, greenery, or other natural material, with an average float requiring up to 100,000 blossoms. It is estimated that more than one half million roses in vials are used in each parade. The average cost of a finished float is between $75,000 and $250,000 depending on the size and mechanics of the float. About 1,000,000 people come to Pasadena to watch the Tournament of Roses.

Getting Around Pasadena

Without Your Car
Visitors, residents, workers and students can get around Pasadena without driving their cars.
That’s because Pasadena’s General Plan has as one of its seven guiding principles that Pasadena will be a city where people can circulate without cars.

Named the most bike-friendly city in LA County, Pasadena has 50 miles of bike routes to jobs, shopping centers, schools and Metro Gold Line stations. Our Pasadena Transit now operates seven routes. And MTA recently introduced a faster way to get to LAX, on the Union Station Fly Away. A new pedestrian plan is also being developed to improve the quality of sidewalks, crosswalks and paths for those who walk, whether to work, stores, transit stops or just for enjoyment.
About Pasadena

The land now famous for the Tournament of Roses, the Rose Bowl, Jet Propulsion Laboratory, and California Institute of Technology, was once occupied by the Hahamogna Tribe of Native Americans. Subsisting on local game and vegetation, the Hahamognas lived in villages scattered along the Arroyo Seco and the canyons from the mountains down to the South Pasadena area. With the arrival of the Spaniards and the establishment of the San Gabriel Mission on September 8, 1771, most of the Native Americans were converted and provided labor for the mission.

The San Gabriel Mission, the fourth in California, grew to be prosperous, with abundant orchards, vineyards and herds. The vast lands which it administered for the Spanish Crown were divided into ranchos. After the rule of California passed from Spain to Mexico, the Mexican government in 1833 secularized the mission lands and awarded them to individuals. The northeast corner of San Gabriel Mission, consisting of the 14,000 acres known as Rancho el Rincon de San Pascual, had previously been gifted in 1826 by the padres to Doña Eulalia Pérez de Guillon, noted for her advanced age as well as her devoted service to the mission. On February 18, 1835, it was formally granted by the Mexican government to her husband, Don Juan Mariné. He and his sons subsequently lost the land which changed ownership a few more times before being granted on November 28, 1843, by Governor Manuel Micheltorena to his good friend, Colonel Manuel Garfias, son of a distinguished Mexican family.

In 1886 Pasadena incorporated, largely as a measure to rid the city of its saloon. In the ensuing decade, amenities such as sewers, paved streets, and electric street lighting were installed. On January 1, 1890, the Valley Hunt Club initiated a mid-winter festival with a procession of flower-bedecked horses and carriages. This became a yearly tradition that in 1898 was formally sponsored by the Tournament of Roses Association. An added tourist attraction was the Echo Mountain incline railway which opened in 1893 and included a mountain chalet resort and the Alpine Tavern at Crystal Springs.

With growth and new development came concern for preserving the unique quality of life in Pasadena. Neighborhood and preservation groups joined forces in 1981 to defeat a proposal to build two high-rise towers in downtown Pasadena. That same year, the Pasadena Redevelopment Agency was disbanded. A citizen initiative to restrict growth was passed in 1989. It was later repealed by voters in 1992, in conjunction with revising the General Plan to respond to growth management issues.

An awakened respect for the city’s architectural treasures led to the renovation of historic homes and buildings throughout the city. Nowhere was this more apparent than in Old Pasadena, where the city’s business district first started. Revitalization of this area occurred throughout the eighties, and culminated at the end of 1992 with the completion of the One Colorado historic block. Transformed into a restaurant and entertainment center, Old Pasadena has become a major attraction in Southern California.

In the eighties, population growth accompanied development. Between 1980 and 1990, the population of Pasadena increased by 11%, becoming more racially and ethnically diverse. The largest increase was in the Hispanic population, which grew to 27.3% of the total city population by 1990. A charter amendment, approved by voters in 1980, changed Pasadena’s election system from city-wide runoffs to district-only elections. This paved the way for the election of minority candidates and a greater emphasis on neighborhood concerns. In 1993, the name for Pasadena’s elected representatives was officially changed from Board of Directors, a term associated with corporations, to City Council, a term prevalent in most city governments. A mayor was selected on a rotating basis from the senior City Council members. The City Manager, however, was responsible for the day-to-day operation of the City. And in 1998, Cynthia Kurtz became Pasadena’s first female City Manager. The same year voters decided it was time to elect a Mayor who could represent Pasadena on a city-wide basis. A former city Council member, Bill Bogard, was elected in 1999.

In 1994, the Northridge earthquake, the most severe quake in a series to hit Southern California, left Pasadena relatively unscathed. The finial atop City Hall’s dome was knocked askew and several residential chimneys were damaged. The world’s leader in seismic research, California Institute of Technology, was consulted frequently during this time by the media.

Between 1970 and 2005, Caltech’s faculty and alumni garnered 14 of the Institute’s 31 Nobel prizes. The most recent award went to Robert H. Grubbs in 2005 in chemistry, along with Yves Chauvin (Institut Français du Pétrole) and Richard R. Schrock (MIT), for their work in the development of the metathesis method in organic synthesis. Perhaps best known for its research in physics, the Institute’s faculty and alumni have also received Nobel Prizes in the fields of Physiology or Medicine, Economics and Peace.

Caltech’s satellite laboratory, Jet Propulsion Lab (JPL), was responsible for several of NASA’s successes in the 1980s and 1990s including deep space navigation and communication, digital image processing, intelligent automated systems, and microelectronics. Despite recent setbacks in the loss of the Mars probe Orbiter and the Mars Polar Lander, it is the memory of the Mars Pathfinder Mission that still remains.
In July of 1997, the world was able to watch as Rover, a robot on four wheels with a camera and extendable arms, moved over the surface of the red planet. The robot took photographs, collected rock and soil samples and transmitted scientific data back to Earth. Rover lasted considerably longer than it was originally designed before it fell silent in September 1997.

Through the end of the 1920s, Pasadena continued to enjoy a reputation as a tourist center and winter resort for the wealthy. The city had much to offer culturally. The Pasadena Community Playhouse was incorporated in 1917 and moved to the new Pasadena Playhouse in 1925. A 100-inch telescope was installed atop Mt. Wilson under the direction of Dr. George Ellery Hale in 1917. The Pasadena City Junior College District was created in 1924. The Grace Nicholson Gallery (which became the Pasadena Art Institute in 1943 and is now the Pacific Asia Museum) was completed in 1926 and the Pasadena Civic Symphony Orchestra and Civic Chorus was founded by Tuesday Musicale in 1929. The city government, which changed to a Board of Directors/City Manager structure in 1921, expanded municipal facilities. The Rose Bowl stadium and Brookside Park recreation facility were built. A 1923 city bond issue financed the construction of a handsome Civic Center, consisting of the Central Library (opened on February 12, 1927), City Hall (opened on December 27, 1927) and the Civic Auditorium (which opened in 1932).
In Memoriam
David C. Virissimo
March 10, 1960 — June 2, 2016

It is with our deepest sorrow that we inform fellow IMAPS members of the loss of dedicated member David C. Virissimo.

Dave was an active member of IMAPS since 1995 and became a Life Member in 2012. His dedication and support of IMAPS was reflected by a seemingly endless list of progressive volunteer roles with the Society, including the local San Diego Chapter, the Microelectronics Foundation, the annual symposium organizing committee and the IMAPS Executive Council. IMAPS is extremely grateful for Dave’s work on behalf of the Society. The legacy he leaves behind is unsurpassed.

Fellow colleagues have responded to the sad news with an outpouring of love and admiration. IMAPS President Sue Trulli said “Dave was totally committed to IMAPS but he was also a stalwart friend, a person with passionate ideas and beliefs” and that “he always had a way to work in a laugh or smile that enabled him to work and befriend so many different types of people.” We invite members and friends alike to reflect on Dave’s life and share his impact at http://www.featheringillmortuary.com/book-of-memories/2528911/Virissimo-David/service-details.php.

Dave was previously spotlighted as a member in 2005 (on the Member Spotlight page at www.imaps.org/membership/spotlight.htm) when he was remembered by Ken Kuang, fellow San Diego chapter friend, as “the kind of leader who inspires others.” IMAPS will again spotlight Dave on the IMAPS spotlight page over the coming weeks, along with sharing memories from the IMAPS community.

Dave was a 1984 graduate of UC San Diego, where he earned his degree in Computer Science. He became a specialist in sales and marketing for the high tech microelectronics industry for the remainder of his career.

Dave is survived by his wife Angela, his son David Jr., his daughters Maurenna and Alyssa, and many other members of his extended family. In lieu of flowers, they have requested donations to St. Madeleine Sophie’s Center (2119 East Madison Avenue, El Cajon, CA 92019-1111), an organization set up to educate and empower adult individuals with development disabilities. The David Virissimo Memorial Fund has been created for this purpose. Several of Dave’s friends and colleagues sent personal condolences.

David was always positive and made all of us work together; great friend and will be miss greatly. — Ray Pettit

Dave was a great guy, eternally upbeat, energetic and giving. Who else other than Dave could turn their vices into charitable events? The Microelectronics Foundation benefited from his enjoyment of gambling and the worst vice of all, golf, with his organization of the Texas Hold’em night at DPC and International Symposium golf tournament. He will be greatly missed. — Casey Krawiec

There is a saying that people live up or live down to your expectations — Dave consistently exceeded the highest of expectations! Whether in the workplace, the industry’s technical society, our local IMAPS Chapter, or at play, David was one who always excelled. He volunteered for any task, including the most mundane and least visible. When I asked him why he was still umpiring Little League, he responded that he “owed it to the kids, the umpires out there are SO bad…” His devotion to his family, his church, and his community was beyond exemplary. But, most of all, he excelled at just being a great friend! — Wally Johnson

Dave, you were a pillar of IMAPS. More important, a friend to so many and you made everyone’s lives brighter when in your company. You made our society, our industry, our world … a better place. I am so blessed to have been friends with you. Your smile, laughter, and friendship will be missed beyond any words can express. — Bill Ishi

Dave was and will continue to be a special light in my life. He was so open and caring when I first started working with our local IMAPS chapter. He made me laugh so many times! He was so sharp and intelligent, but he masked that with a gentleness of spirit that made him approachable to all who were blessed to know him. I know Dave is resting in peace with our Lord Jesus Christ. To Dave’s family: I will pray for you all to get through this heartbreaking time with strength from God and knowing how blessed you were to have David in your family. — Iris Labadie
Kester Launches NF372-TB Flux-Pen® and RF550 Rework Flux

ITASCA, IL, April 27, 2016—Kester is proud to announce the launch of NF372-TB Flux-Pen® and RF550 Rework Flux. These products were formulated to complement Kester’s high-reliability, no-clean product line.

NF372-TB Flux-Pen® is a zero-halogen, no-clean, low solids flux available as a Flux-Pen® for rework of conventional and surface mount circuit board assemblies. Kester NF372-TB flux passes IPC SIR testing in a raw or unheated state, ensuring Kester NF372-TB Flux-Pen®s can be safely used in rework applications, specifically those with high reliability requirements. NF372-TB Flux-Pen® residues are minimal, clear and non-tacky for improved cosmetics. NF372-TB Flux-Pen® is classified as ROL0 flux under IPC J-STD-004B. For additional information on this product, including technical and safety data sheets, please visit: http://www.kester.com/products/product/NF372-TB-Flux-Pen/.

RF550 Rework Flux is a high-reliability, zero-halogen, no-clean rework flux designed for electronic component rework and repair applications. RF550 has a gel-like consistency and is packaged in syringes for easy dispensing. RF550 can be precisely dispensed onto specific areas that require flux. After being dispensed, RF550 stays in place until soldering occurs. RF550 has excellent performance in applications requiring high reliability. RF550 is the ideal choice for QFP or BGA semi-automated rework applications, and is well suited for use with through-hole repair. For additional information on this product including technical and safety data sheets, please visit: http://www.kester.com/products/product/RF550-Rework-Flux.

For any questions or additional information, please contact either Lynnette Colby, Global Product Manager, lcolby@kester.com or Michelle O’Brien, Marketing and Communications Specialist.

Kester is a global supplier of assembly materials for the Electronic Assembly and Semiconductor Packaging industries. Kester is focused on delivering innovative, robust and high-quality solutions to help our customers address their technological challenges. Kester’s current product portfolio includes soldering attachment materials such as solder paste, soldering chemicals, TSF (tacky solder flux) materials, and metal products such as bar, solid and flux-cored wire. Kester is an Illinois Tool Works (ITW) company. ITW is a Fortune 200 company that produces engineered fasteners and components, equipment and consumable systems, and specialty products. It employs approximately 49,000 people, and is based in Glenview, Illinois, with operations in 57 countries.
Your IMAPS Member Benefits at Your Chapter Level

Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar

Central Texas

The Central Texas Chapter had a meeting on May 10, 2016 with 71 attendees for the four technical presentations. The presentations were “Cortex-A72: Current State-of-the-Art Processor,” by Aniket Saha of ARM; “DC Power Distribution Is Coming to a Building Near You: Driven by LED Lighting,” by Drew Vigen of ALGLO; “Smart Cities and the IoT: Austin Looks Forward,” by Bert Haskell of Pecan Street, Inc.; and “Additive Manufacturing for Microelectronics Packaging Applications,” by Dr. Michael Cullinan of Nanoscale Design & Manufacturing Lab at UT-Austin. Pizza was served after the meeting to facilitate networking.

The next meeting is being planned for August 16 with a factory tour in addition to the technical presentations.

Cleveland-Pittsburgh

A very successful IMAPS Cleveland-Pittsburgh Chapter meeting was held May 18, at Aerotech Corporation in Pittsburgh, PA. We had the following presentations:

• Bob Novotnak, Aerotech, who described Aerotech’s history, competencies, products, and a general overview. Aerotech is a vertically integrated company that excels in “Precision Mechatronic Design,” while offering standard motion control components and custom integrated systems for specific applications.

• Lee Levine, Process Solutions Consulting, on the role and interactions of ultrasonic energy in wirebonding. Lee, who is a noted authority on wirebonding, presented the history of the gold/copper transition and the physics behind using ultrasonic vibration in wirebonding as a substitute for heat.

• Volker Heydemann, Advantech US, describing Advantech US capabilities in additive manufacturing of electronics. Advantech US can deposit many materials, in their purest form, on almost any substrate. They have a growing list of applications in embedded passive and active electronic components.

• Johnny Vanderford, Lorain County Community College, on his curricula on MEMS and microelectronics, and how he is connecting with local employers in order to optimize training for future employees.

• Brian O’Connor and Will Land, Aerotech, took our group on a tour of Aerotech’s engineering and manufacturing areas.

In general, our chapter has two to four meetings per year, alternating between the Pittsburgh and Cleveland areas. The pacing items are (a) having a collection of presentations ready for the meeting, and (b) a company that would like to host.

San Diego

The San Diego Chapter held a technical program at Peregrine Semiconductor on May 17th. A presentation titled “Qualification of Automotive RF-IC Packages” was given by Mumtaz Bora from Peregrine. The lunch-time program was well attended. We’d like to thank Ms. Bora for her informational presentation and Peregrine Semiconductor for hosting the event.
Indiana

On May 17, 2016, Indiana IMAPS hosted its inaugural Electronics Technology Exchange at the WestGate Academy Conference and Training Center, located just outside the main gate of NSWC in Crane, Indiana. The event was a collaborative effort between Indiana IMAPS, WestGate Academy and Crane NSWC. The event featured a technical seminar with eight presentations on a variety of cutting edge topics related to the microelectronics industry, including advanced materials and electronic components, trends in electronic counterfeiting, and the effects of radiation on electronics. The technical session was followed by vendor displays that included 32 suppliers showcasing a wide variety of microelectronics products and services.

Two special displays, covering both ends of the technology spectrum, were part of the event. Delphi Electronics generously provided and demonstrated its Ford Mustang concept car. The V2E (Vehicle to Everything) delivers a super-enhanced driving experience including a high definition 3D-like instrument cluster, a driver-controlled performance display, and a separate display for the passenger. The vehicle is also able to communicate with devices both inside and outside the car. And for a bit of nostalgia, a 1973 Amana microwave oven, featuring the first electronic controls that were developed by Essex Controls in Logansport, Indiana, was also on display. This new touchplate eliminated the original mechanical dial and made the microwave oven the affordable appliance we have today.

Over 100 industry professionals attended the event. General chair Larry Wallman worked for over a year with WestGate Academy and NSWC Crane to make the technology exchange a reality. The response from NSWC Crane, WestGate Academy, attendees and suppliers was overwhelmingly positive, and they all hope to build on this success to make the Technology Exchange at WestGate Academy an annual Indiana IMAPS event.

The Indiana IMAPS chapter will hold its yearly planning meeting for officers and chairpersons in late July to plan the 2016/2017 Indiana IMAPS event calendar. Ideas for meeting topics and tours are always welcome and can be forwarded to President Larry Wallman at lwallman@sbcglobal.net.
Welcome New IMAPS Members!

March - May 2016

Individual Members
Dennis Adams
Rebecca Agapov
Hisanori Akmaru
Siddharth Alur
Sawa Araki
Markus Arndt
Hitoshi Arora
Dorra Bahoul
Eyup Can Baloglu
Ross Bannatyne
Patricia Bartlett
Raymond Bastnagel
Maria Benavides Herrera
Keith Best
John Bonistall
Steve Breed
Geoff Breneke
Roger Browne
Cole Brinkley
Harlan Brown-Shaklee
Richard Burke
Lagree Burke
Ahmed Busnana
Karen Carpenter
Tim Cheah
James Claypool
Jim Connell
Adam Cook
Jeffrey Craig
Bill De
Charles Deleuze
Juan Dominguez
James Dunlop
David DuPre
Darwin Edwards
Dennis Eichorst
Steven Enter
Annais Maurena Evariste
Claudia Fabre
Paul Feeney
Ken Flanders
Katherine Fordon
Norio Fujinoka
Greg Gibson
Joshua Gilbrech
Leszek Golonka
Rena Gradmann
Sebastian Gropp
Amy Grossman
Dan Gunter
Nam Gutzeit
Bongae Han
Justin Harms
Ahmad Hassani
Frank Haughn
Jacob Heisler
David Hepper
Tsuya Hirata
Thor Hobak
Ken Hrdina
Maggie Hu
Li-Lyng Hung
Stanley Ilpe
Tomio Inoue
David Jandzinski
Jeng Jhy-Long
Thomas Jones
Corey Juarez
Thomas Karwan
Robert Kavanagh
Bradley Kent
Ill Ji Kim
Jin Kim
Kevin Klein
Cheng-Ta Ko
Jamie Kofoid
Dharani Kothakonda
Scott Krogger
Krishna Chaitanya Kundeti
Rezwan Lateef
Dae Hyung Lee
Daeki Lee
Solomon Lekia
Laurent Lenggignon
Prayudi Lianto
Kernick Liu
Kevin Lourly
Jan Maciosczyk
Gunnar Maehlum
Sanjay Malik
Khadee Malik
Cristina Matos-Perez
Michael Merschlik
Daniel Mitan
Nakamura Mitsutaka
Kenneth Miu
Max Modugno
David Mohoric
David Moreno
Ross Muenchhausen
Cornelius Muoekwu
Robert Murphy
Souheil Nadri
Philipp Natzke
Pradeep Naray
Eric Nichols
Toshihiko Nishio
Hiroyuki Niwa
Koki Nonaka
Christopher Ober
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Mano Ricardo Gongora Rubio
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Katsuyuki Sakamoto
Shinya Sakamoto
Jebreel Salem
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Brad Thrasher
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Kazahide Uno
Hong Wang
Lei Wang
Chi-chun Wang
Jim Watkins
Shayna Watson
Matt Watson
Brenden Wells
Robb White
Frank Windrich
Frank Winter
Bulong Wu
Gary Wu
Linh Xie
Assushi Yamamoto
Trevor Yancey
Gary Yeager
Kimberly Yess
Soak Da Yoon
Sandy Zaehringer
Liuhua Zhang
Jay Zhang
Jeff Zhu

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Find out more information at http://jobs.imaps.org/home
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www.IMAPS.org

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Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!
Join now!

IMAPS corporate memberships are designed to give your company a competitive advantage in the microelectronics packaging industry. Choose the right membership to meet your exhibition, advertising, discount registration needs and more.

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<th>Membership package inclusions</th>
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<td>For organizations with more individual members or those seeking more marketing exposure</td>
<td>Our most popular corporate membership package</td>
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<td>Number of employees who receive individual membership benefits</td>
<td>No limit to number of individual members with full online access; Up to 5 receive print magazine</td>
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<td>Access to IMAPSource, the microelectronics research portal</td>
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<td>150 downloads via two (2) selected member logins</td>
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Premier Corporate Members

IMAPS has introduced a new level of support for corporate members. These companies have decided to participate in our Society at the Premier Corporate Member level. We are extremely grateful for their dedication to the furtherance of our educational opportunities and technological goals.
IMAPSource transitioned to membership level plans for free downloads on April 1st. The number of free annual downloads included in your membership corresponds to your member type.

Non-members can enjoy articles and proceedings from IMAPSource for $20 per download.

IMAPS members are pre-registered with IMAPSource and receive a profile confirmation email from Allen Press. This will help members gain unlimited download access to IMAPSource. Non-members and guests will need to click Register Now at IMAPSource.org.

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*Unlimited package allows multiple IP range and unlimited access

Contact IMAPS HQ today for more information about IMAPSource registration, member benefits, IP range setup for Premier Corporate and Academic Institution members and more!
# Chapter Contacts

<table>
<thead>
<tr>
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<th>MEMBER NAME</th>
<th>E-MAIL</th>
</tr>
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<tbody>
<tr>
<td>Angel</td>
<td>Maurice Lowery</td>
<td><a href="mailto:maurice.lowery@ngc.com">maurice.lowery@ngc.com</a></td>
</tr>
<tr>
<td>Arizona</td>
<td>Jody Mahaffey</td>
<td><a href="mailto:jody@ereach.co">jody@ereach.co</a></td>
</tr>
<tr>
<td>California Orange</td>
<td>Bill Gaines</td>
<td><a href="mailto:William.gaines@ngc.com">William.gaines@ngc.com</a></td>
</tr>
<tr>
<td>Chesapeake</td>
<td>Lauren Boteler</td>
<td><a href="mailto:Lauren.m.boteler.civ@mail.mil">Lauren.m.boteler.civ@mail.mil</a></td>
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<tr>
<td>Carolinas</td>
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<td>Interested? Contact Brianne Lamm <a href="mailto:blamm@imaps.org">blamm@imaps.org</a></td>
</tr>
<tr>
<td>Central Texas</td>
<td>Rick Prekup</td>
<td><a href="mailto:rprekup@ionsn.com">rprekup@ionsn.com</a></td>
</tr>
<tr>
<td>Cleveland/Pittsburgh</td>
<td>John Mazurowski</td>
<td><a href="mailto:jmazurowski@eoc.psu.edu">jmazurowski@eoc.psu.edu</a></td>
</tr>
<tr>
<td>Empire</td>
<td>Andy Mackie</td>
<td><a href="mailto:amackie@indium.com">amackie@indium.com</a></td>
</tr>
<tr>
<td>Florida</td>
<td>Mike McEntee</td>
<td><a href="mailto:Mike.McEntee@PrecisionTestSolutions.com">Mike.McEntee@PrecisionTestSolutions.com</a></td>
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</tr>
<tr>
<td>Greater Dallas</td>
<td>Sam Forman</td>
<td><a href="mailto:sam.forman@m-coat.com">sam.forman@m-coat.com</a></td>
</tr>
<tr>
<td>Indiana</td>
<td>Ray Fairchild</td>
<td><a href="mailto:m-ray.fairchild@delphi.com">m-ray.fairchild@delphi.com</a></td>
</tr>
<tr>
<td>Metro</td>
<td>Scott Baldassarre</td>
<td><a href="mailto:Scott.Baldassarre@aeroflex.com">Scott.Baldassarre@aeroflex.com</a></td>
</tr>
<tr>
<td>New England</td>
<td>John Blum</td>
<td><a href="mailto:jblum1@gmail.com">jblum1@gmail.com</a></td>
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<tr>
<td>San Diego</td>
<td>Mumtaz Bora</td>
<td><a href="mailto:mbora@psemi.com">mbora@psemi.com</a></td>
</tr>
<tr>
<td>Viking</td>
<td>Mark Hoffmeyer</td>
<td><a href="mailto:hoffmeyer@us.ibm.com">hoffmeyer@us.ibm.com</a></td>
</tr>
<tr>
<td>Germany</td>
<td>Ernst Eggelaar</td>
<td><a href="mailto:ee@microelectronic.de">ee@microelectronic.de</a></td>
</tr>
<tr>
<td>France</td>
<td>Florence Vireton</td>
<td><a href="mailto:Imaps.france@imapsfrance.org">Imaps.france@imapsfrance.org</a></td>
</tr>
<tr>
<td>United Kingdom</td>
<td>Andy Longford</td>
<td><a href="mailto:Andy.longford@imaps.org.uk">Andy.longford@imaps.org.uk</a></td>
</tr>
<tr>
<td>Taiwan</td>
<td>Wun-Yan Chen</td>
<td><a href="mailto:wunyan@itri.org.tw">wunyan@itri.org.tw</a></td>
</tr>
<tr>
<td>Nordic</td>
<td>Terho Kutilainen</td>
<td><a href="mailto:treasurer@imapsnordic.org">treasurer@imapsnordic.org</a></td>
</tr>
<tr>
<td>Benelux</td>
<td>Katrien Vanneste</td>
<td><a href="mailto:Katrien.vanneste@elis.ugent.be">Katrien.vanneste@elis.ugent.be</a></td>
</tr>
<tr>
<td>Italy</td>
<td>Marta Daffara</td>
<td><a href="mailto:info@imaps-italy.it">info@imaps-italy.it</a></td>
</tr>
<tr>
<td>Japan</td>
<td>Orii Yasumitsu</td>
<td><a href="mailto:ORII@jp.ibm.com">ORII@jp.ibm.com</a></td>
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<tr>
<td>IMAPSource</td>
<td>Brian Schieman</td>
<td>412-368-1621</td>
<td><a href="mailto:bschieman@imaps.org">bschieman@imaps.org</a></td>
<td><a href="http://www.imaps.org">www.imaps.org</a></td>
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</tr>
<tr>
<td>Indium</td>
<td>Rick Short</td>
<td>315-381-7554</td>
<td><a href="mailto:rshort@indium.com">rshort@indium.com</a></td>
<td><a href="http://www.indium.com">www.indium.com</a></td>
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<tr>
<td>Master Bond</td>
<td>Robert Michaels</td>
<td>201-343-8983</td>
<td><a href="mailto:info@masterbond.com">info@masterbond.com</a></td>
<td><a href="http://www.masterbond.com">www.masterbond.com</a></td>
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</tr>
<tr>
<td>Mini-Systems, Inc.</td>
<td>Craig Tourgee</td>
<td>508-895-0203</td>
<td><a href="mailto:ctourgee@mini-systemsinc.com">ctourgee@mini-systemsinc.com</a></td>
<td><a href="http://www.mini-systemsinc.com">www.mini-systemsinc.com</a></td>
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Advancing Microelectronics
2016 Editorial Schedule

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<tr>
<td>Sept/Oct MEMS and Thermal Management</td>
<td>July 8</td>
<td>July 13</td>
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<tr>
<td>Nov/Dec Ceramic: Thick &amp; Thin Film</td>
<td>Sep. 8</td>
<td>Sep. 13</td>
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</table>

WHO TO CALL

Michael O’Donoghue, Executive Director, (919) 293-5000, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction, Exhibits, Meetings

Brian Schieman, Director of Programs, (412) 368-1621, bschieman@imaps.org, Development of Society Programs, Website Development, Database Management, Communication Tools and other Technology, Exhibits, Publications

Ann Bell, Manager, Managing Editor, Advancing Microelectronics, (703) 860-5770, abell@imaps.org, Public Relations, Marketing, Fundraising, Advertising

Brianne Lamm, Membership & Events Manager, (919) 293-5000, blamm@imaps.org, Member Relations and Services Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support
## Calendar of Events

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<th>Date</th>
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<td>IMAPS 2016</td>
<td>Pasadena, CA</td>
<td><a href="http://www.imaps2016.org">www.imaps2016.org</a></td>
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<tr>
<td>10-25-16</td>
<td>Advanced Technology Workshop and Tabletop Exhibit on Thermal Management</td>
<td>Los Gatos, California</td>
<td><a href="http://www.imaps.org/thermal/">www.imaps.org/thermal/</a></td>
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<tr>
<td>11-9-16</td>
<td>FUTURECAR: New Era of Automotive Electronics Workshop</td>
<td>Atlanta, GA</td>
<td><a href="http://www.prc.gatech.edu/FUTURECAR">www.prc.gatech.edu/FUTURECAR</a></td>
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<tr>
<td>3-6-17</td>
<td>Device Packaging 2017</td>
<td></td>
<td></td>
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<tr>
<td>7-10-17</td>
<td>HiTEN - High Temperature Electronics Network</td>
<td>Cambridge, United Kingdom</td>
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