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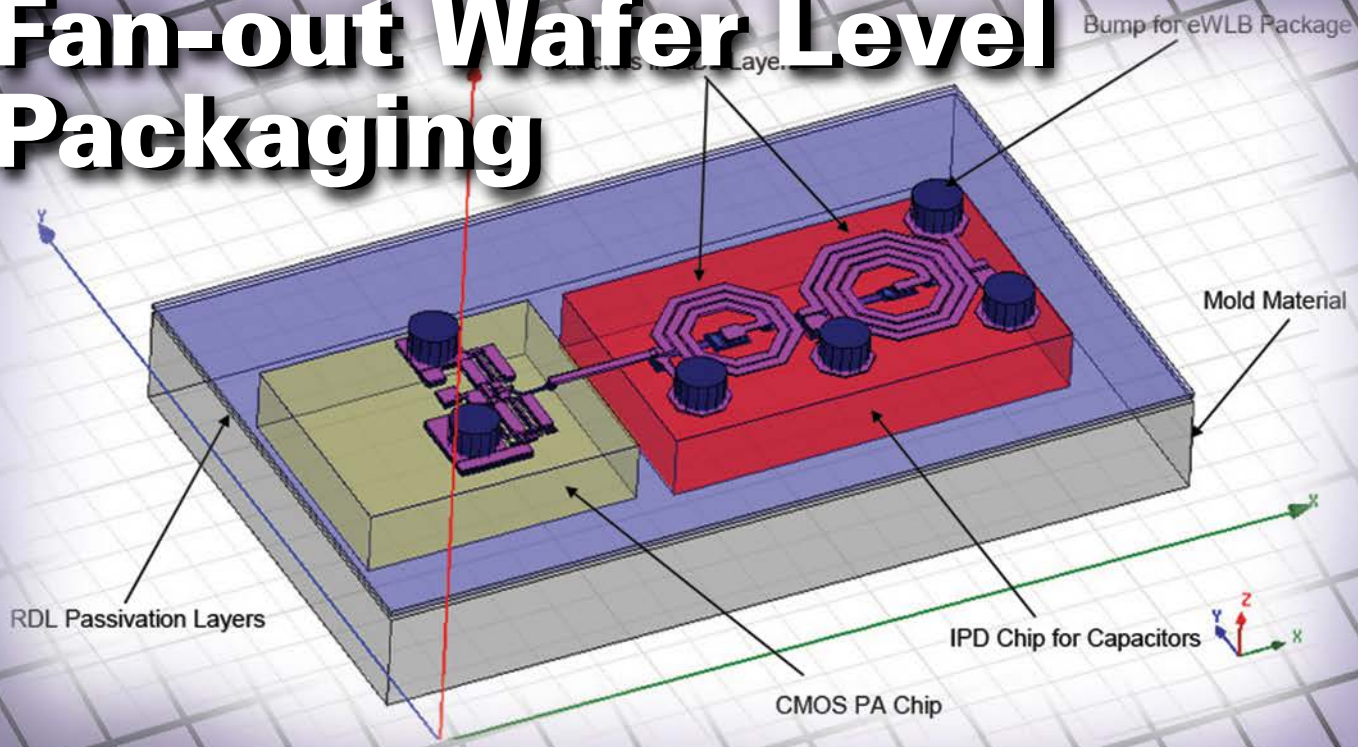
JANUARY/FEBRUARY 2018
Vol. 45 No. 1

# Device Packaging Conference and Fan-out Wafer Level Packaging

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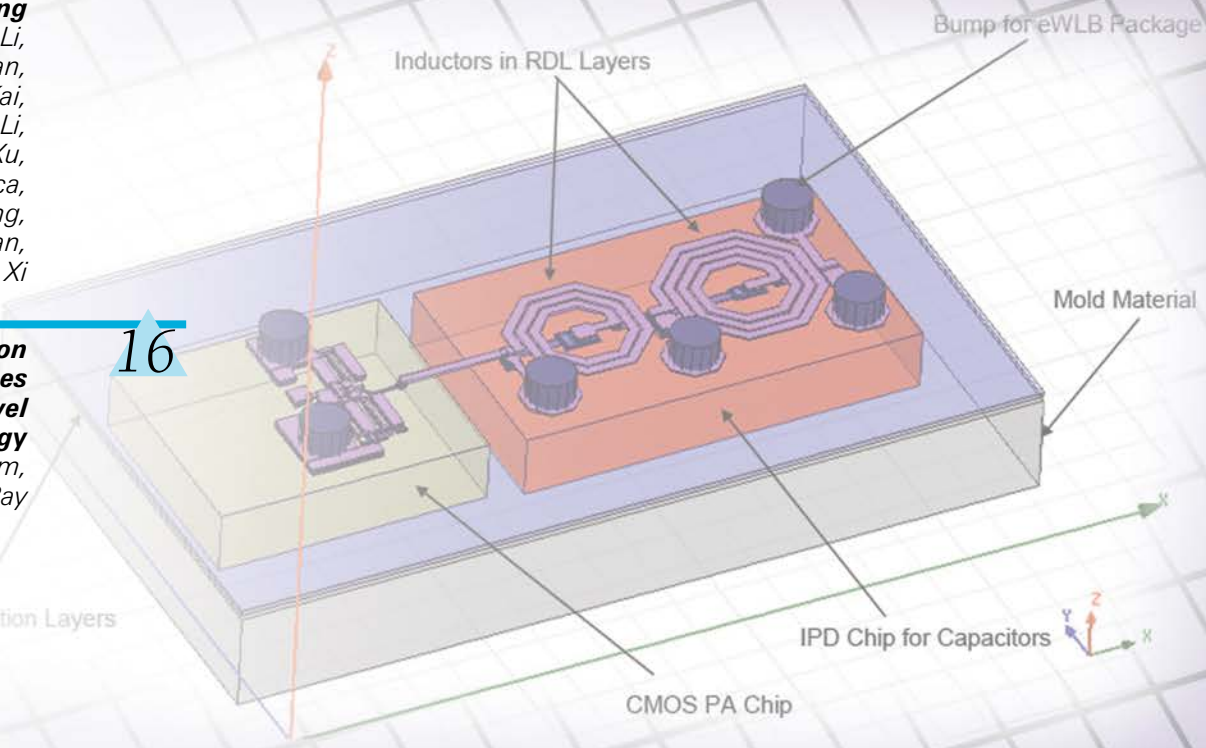


*On the Cover:*
*Illustration of a PA die and silicon IPD die embedded in mold substrate.*

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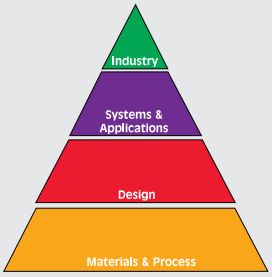


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FROM THE GUEST EDITOR

*Jon Aday – Sr. Staff Engineering Manager, Qualcomm*
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# Fan Out Wafer Level Packaging

Fan Out Wafer Level Packaging (FOWLP) has been growing in popularity as it has gained traction as a package choice in the mobile phone industry. FOWLP has been used for products of varying complexity, from the applications processor to the more simple RF, Codec, and PMIC applications. There are several different technologies being run in production as well as in development that have the potential to continue to drive this packaging technology into the mainstream. These unique FOWLP technologies all have their pros and cons in the manufacturing and business model associated with them and the articles presented here today show three different methods of making a FOWLP package.

Standard FOWLP, also referred to as advanced embedded Wafer Level Ball Grid Array (eWLB) technology, has been in production the longest. It is based on placing the die face down during the molding operation. eWLB is also a die first technology in which the package circuity or redistribution layer (RDL) is built on the reconstituted wafer. There has been quite a bit of work that has been done to transition this technology from doing single die only packages, but to also enable System-in-Package (SiP) applications by including multiple die and passives. This integration allows for significant size reductions and techniques are implemented to allow back side connections to facilitate package stacking or adding passives to the top of the package as well.

Another assembly technique of doing a face up FOWLP requires the use of copper pillars or studs to be plated on the wafer before the molding process. There are several aspects of this process that are critical to have good chip placement after molding in order to facilitate design rules for the first connection of the RDL to the reconstituted die in the panel. The coefficient of thermal expansion (CTE) of the mold and the carrier is critical in controlling the die movement after molding. The chip attach offset and molding process parameters are also critical aspects of the assembly process to control and understand the impacts on die location. A unique aspect of the face up FOWLP is that a grinding process is used to expose the cu pillar for the RDL connection. Tight controls on the back grinding step of incoming silicon wafers and the front grinding to expose the copper are needed in order to maintain a robust process.

One final technology that will be reviewed is the concept of doing a die last approach where the RDL layers are manufactured using a sacrificial carrier prior to doing assembly of the die onto the FOWLP. This also requires the wafers to be bumped and a conventional mass reflow process is typically used for bonding the die to the RDL. This technology has the benefit that for multilayer RDL applications the yield of the RDL can be verified prior to committing a good die to those locations. This technology can also be expandable to package stacking and SiP applications.

There will not be a one-size-fits-all for the different applications that are being targeted. It will be exciting the next few years as these technologies mature and evolve to handle the new packaging challenges that present themselves.

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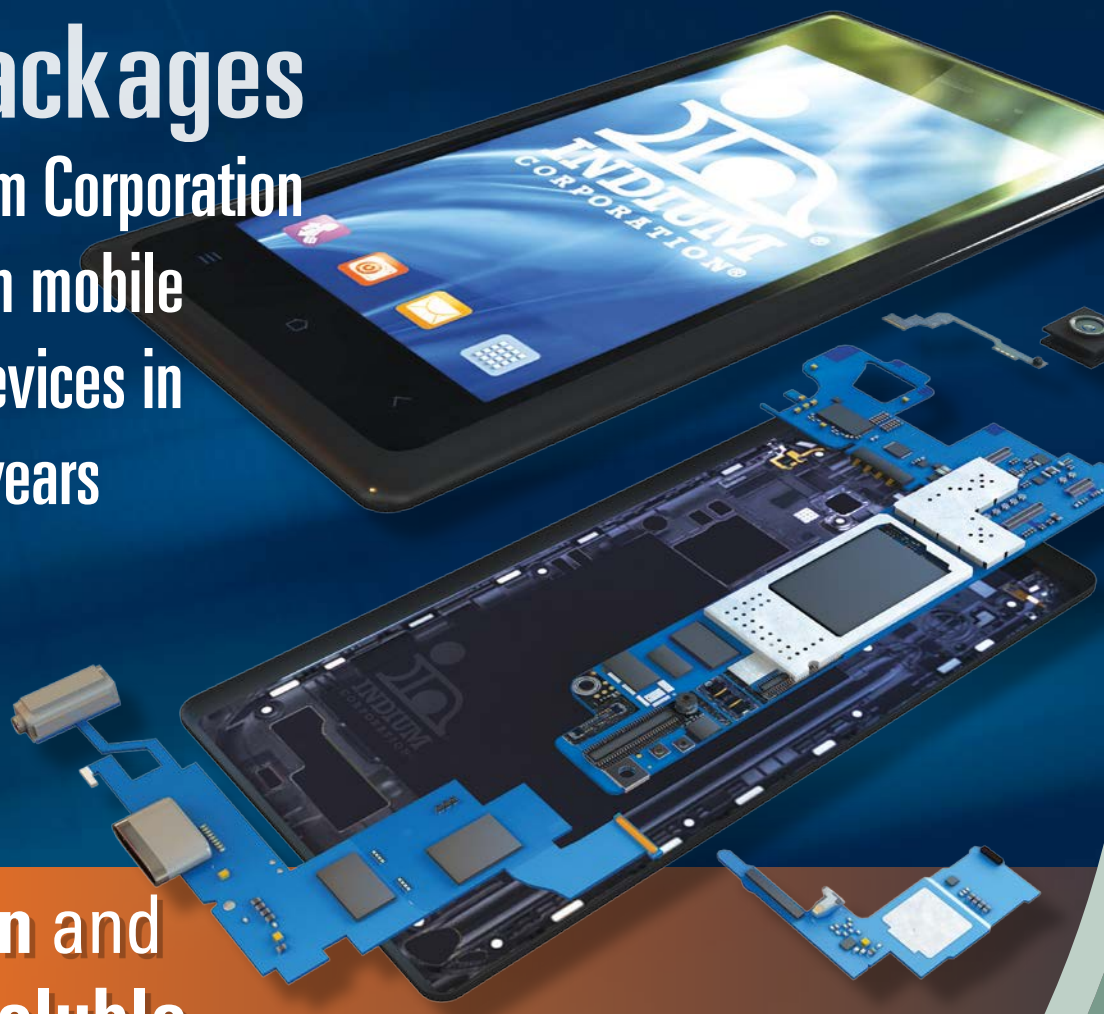


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# Silicon Wafer Integrated Fan-out Technology Packaging

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## *Abstract*

*This paper reviews Silicon Wafer Integrated Fan-out Technology (SWIFT®) packaging methodology and its performance in a typical mobile application. In addition, the advantages of a SWIFT design are reviewed in comparison to a conventional competing 3D packaging technology. Package information, electrical simulation, and reliability test data will be presented to show how SWIFT technology is poised to provide robust, reliable, and low-cost 3D packaging solutions for advanced mobile products.*

*Key words*
*FOWLP, Chip-Last, WLFO, SWIFT, PoP, Fan-out*

## Introduction

The remarkable growth in the mobile handset and tablet markets has been fueled by consumer demand for increased mobility, functionality, and ease of use. This, in turn, has been driving an increase in functional convergence and 3D integration of IC devices, resulting in the need for more complex and sophisticated packaging techniques. A variety of advanced IC interconnect technologies are addressing this growing need. These include Through Silicon Via (TSV), Chip-on-Chip (CoC), and Package-on-Package (PoP) approaches. In particular, emerging Wafer Level Fan-Out (WLFO) technology provides unique and innovative extensions into the 3D packaging realm.

Traditional WLFO technologies [1], [2] are limited in design rules and 3D integration capabilities due to the processes and equipment used for circuit patterning. For more aggressive designs, TSV processes must be incorporated, which often exceed the cost budget and design requirements for the device. Consequently, a gap exists between the design capabilities of WLFO and TSV that needs to be addressed.

A new, innovative fan-out structure called Silicon Wafer Integrated Fan-out Technology (SWIFT®) packaging incorporates conventional WLFO processes with leading-edge thin film patterning techniques to bridge the gap between TSV and traditional WLFO packages. The SWIFT methodology is designed to provide increased I/O and circuit density within a reduced footprint and profile for single and multi-die applications. The improved design capabilities of the technology is due, in part, to the fine feature capabilities associated with this new, innovative wafer level packaging technique. The fine features allow much more aggressive design rules to be applied compared to competing WLFO and laminate-based technologies. In addition, the unique characteristics of the SWIFT process enable the creation of innovative 3D structures that address the need for IC integration in emerging mobile and networking applications.

## Traditional PoP Packages

For smartphones and wearable devices, 3D PoP structures have become the de facto standard for application processor (AP) and DRAM memory integration. Laminate organic substrate technology is typically used for these designs. The two most common PoP structures used in today's advanced mobile devices are illustrated in Figure 1: a) Through Mold Via PoP (TMV® PoP) and b) Interposer PoP. TMV PoP incorporates through mold via technology to create the vertical signal path between the LPDDR top memory package and the underlying AP logic package. The memory package is directly attached to the TMVs that are located around the perimeter of the package. Consequently, custom memory must be used. Alternatively, Interposer PoP incorporates a laminate substrate on the top of the AP (bottom) package. Although this adds thickness to the bottom package, it allows standard pitch memory packages to be used, which opens up the supply chain for memory sourcing.

*Figure. 1* *a) TMV PoP* *b) Interposer PoP*

These laminate-based PoP structures have limitations that affect their ability to extend into high-speed and high bandwidth memory (HBM) applications for advance mobile devices.

- Feature size: Laminate-based organic substrates are currently limited to ~15-µm minimum line/space and 15-µm thick copper trace feature sizes. The laser drilled via diameter is also limited. These limitations restrict the designer's ability to optimize power distribution and control the impedance of critical signals.
- Z-height: The organic laminate substrate's core and pre-preg materials add thickness to the interconnection structure, which has an adverse effect on the power distribution network (PDN) impedance.
- Memory interface pitch: The current limit for TMV PoP and Interposer PoP is 0.35 mm and 0.27 mm minimum memory pitch, respectively. This is due to the physical space required for the vertical interconnect media. Consequently, the memory I/O is limited based on the overall package body size.

The above aspects of organic laminate-based PoP structures make its applications more difficult as memory bus speeds extend into the DDR4/5, PCIe, and Ethernet speeds. To address these challenges, an existing Interposer PoP device was converted to SWIFT packaging. The physical attributes were compared and the electrical performance was analyzed via simulation modeling. The following sections discuss the SWIFT structure and the physical and electrical comparison study in detail.

## SWIFT Structure

A typical SWIFT PoP structure is illustrated in Figure 2. SWIFT technology is based on wafer-level processing, incorporating the use of a carrier and thin film photolithography to pattern the fine metal and dielectric features in a multi-layer redistribution layer (RDL) structure. SWIFT is a "chip last" process which has the advantages associated with conventional organic substrates regarding yield and cycle-time. Once the chip-last SWIFT package's RDL is fabricated on the carrier, the structure is inspected, known-bad-RDL sights are identified, and the SWIFT "substrate" is placed in inventory. This allows for a shorter overall cycle time and ensures a known-good-die is dedicated to a known-good-substrate. This is not possible with "chip first" wafer fan-out technologies where the RDL process is responsible for the majority of the yield impact [3]. The chip last SWIFT technology approach also has superior flexibility and scalability, since it can support many package variants, such as 3D PoP, system-in-package (SiP), multi-dies, passive components, and variable component thicknesses. The benefits of SWIFT technology are further detailed in the following sections.

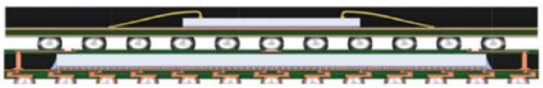


*Figure 2. SWIFT PoP Structure*

## Physical Benefits

One of the significant benefits of using wafer level packaging is the form factor reduction including the package z height. Package thickness has critical effects on the signal and power integrity since the conductive path changes as the package height changes. In addition, the thermal performance of the package also benefits from a thinned package since the resistive path would be shortened. SWIFT packaging is approximately 40% thinner compared to competing laminate-based technologies and thus provides substantial improvements.

Figure 3 shows cross-section representations of the Interposer PoP and the equivalent SWIFT PoP structures used for the comparative study. A total package thickness of 630 µm (excluding memory package) is required for a conventional Interposer PoP structure, whereas the equivalent SWIFT PoP structure results in a thickness of 390 µm – a 38% reduction in overall bottom package thickness.

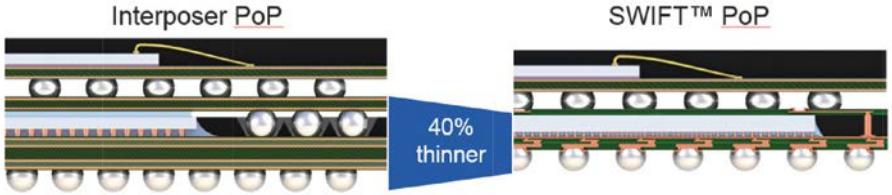



*Figure 3. Package Thickness Comparison*

The thin film organic dielectric RDL build-up and fine feature size capabilities of SWIFT packaging are the primary contributors to this dramatic reduction in z height. The overall metal layer count was reduced from five to four layers, dielectric thickness was reduced from 35 µm to 7 µm, Cu trace line/space/thickness was reduced from 15 µm/15 µm/15 µm to 5 µm/5 µm/3 µm, and via pad size was reduced from 105 µm to 25 µm. The memory interface pitch was also reduced from 350 µm to 250 µm by pattern plating tall copper pillars on the SWIFT substrate.

## Electrical Benefits

The SWIFT PoP structure was compared to the Interposer PoP design for signal integrity, power distribution networking, and impedance matching. With DDR4 memory operating with a timing margin of only 313 ps and the maximum ripple of the PDN is ±60mV, optimizing signal and power integrity is even more critical than with DDR3 [4]. There were even those who believed DDR5 would not happen because the timing budget would be consumed in the package due to PDN noise and package variability [5]. While JEDEC expected to release the DDR5 specification in 2016, DDR5 production is not expected to ramp up until 2020 [6].

Comparing a SWIFT PoP design to Interposer PoP DDR4 speeds (4Gbps), it has a 25% improvement in eye amplitude and 22% improvement in eye height. The jitter is 62% less and rise/fall time is decreased by 31%. This can be seen in Table 1.

continued on page 8

continued from page 7

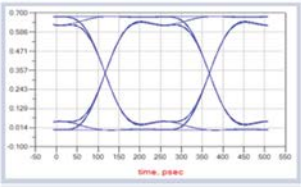
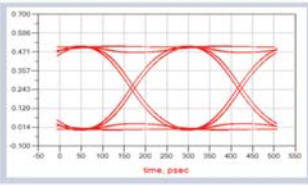
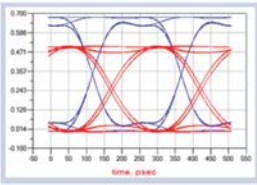
| Key Attributes | SWIFT™ | Interposer PoP | SWIFT™ Benefits |
|---|---|---|---|
| Eye Diagram DDR4 @ 4 Gbps |  |  |  |
| Eye Amplitude | 591 mV | 472 mV | ➢ 119 mV Improvement |
| Eye Height | 562 mV | 461 mV | ➢ 101 mV Improvement |
| Eye Width | 250 ps | 243 ps | ➢ 7 ps Improvement |
| Pk-Pk Jitter | 2.3 ps | 6.1 ps | ➢ 3.8 ps Improvement |
| Rise/Fall Time | 50 ps | 72 ps | ➢ 22 ps Improvement |

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*Table 1. Comparison of Signal Integrity at 4Gbps*

The return loss, insertion loss, and cross-talk all improve with the SWIFT design when compared to its equivalent laminate fan-in PoP package. At 2 GHz, the return loss of the SWIFT PoP design w/1L Top RDL improves by 6 dB and cross-talk improves by 6 dB compared to an Interposer PoP. The SWIFT PoP structure acts as a wideband low-pass filter, whereas Interposer PoP acts as a narrowband low-pass filter with a steep roll off. This data is illustrated in Figure 4.

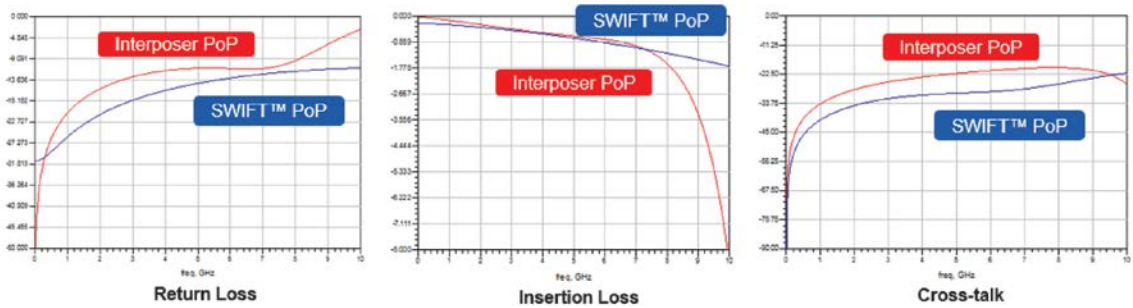


*Figure 4. Signal Integrity Comparison*

A matched impedance between the driver to the transmission line is strongly suggested for DDR4 to eliminate reflections that return to the driver. By eliminating these reflections, the eye has cleaner edges and is more open [7]. The SWIFT PoP structure is better suited to a matched impedance since its impedance curve is more stable as shown in Figure 5.

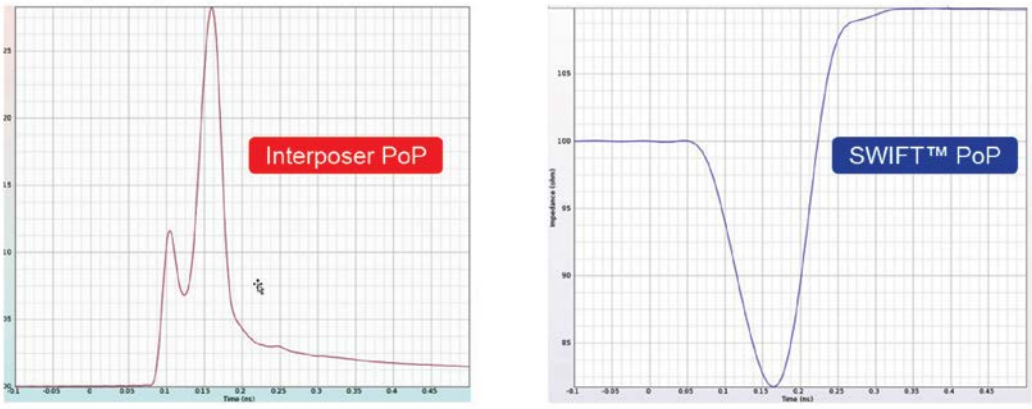


*Figure 5. Time-Domain Reflectometry Comparison*

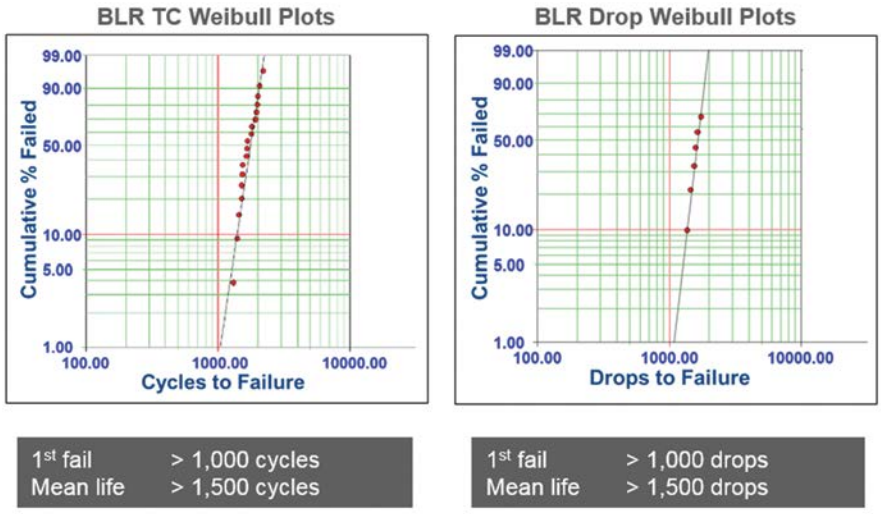


*Figure 6. Board Level Temperature Cycle and Drop Test Results*

## Reliability Data

In order to assess the component level reliability (CLR) and board level reliability (BLR), a 15 x 15-mm body package was used with three RDL layers with a memory stacked in PoP configuration. The chip last HD-FO package TV passed MSL3/260°C CLR tests including High Temp Storage (HTS) 150°C / 1000 hrs, unbiased Highly Accelerated Stress Test (uHAST) 96 hrs and TCB 1000 cycles. BLR tests were passed with TC 2000 cycles (JEDEC condition G) and completed 1000 drops with first failure obtained at 442 drops. Figure 6 shows the temp cycle and drop test results and Weibull analyses.

## Conclusions

An innovative semiconductor packaging technology has been developed that extends the physical and electrical performance of traditional laminate-based PoP structures for mobile applications. SWIFT technology incorporates the advanced feature size and thin film dielectric benefits of wafer level packaging coupled with the device integration capabilities of flip chip assemblies. The SWIFT structure has passed industry-standard component level and board-level reliability requirements. In comparison to a traditional Interposer PoP structure for logic and memory device integration, SWIFT technology exhibits enhanced electrical signal integrity, superior impedance matching, and optimized power distribution. The distinctive characteristics of SWIFT technology are due, in part, to the fine feature capabilities associated with this innovative wafer level packaging technique. This allows much more aggressive design rules to be applied compared to traditional WLFO and laminate-based assemblies. SWIFT technology is truly a versatile, high performance packaging approach for next generation mobile devices and is positioned to serve the semiconductor industry for many years to come.

## Acknowledgements

The authors would like to thank David Ladick, Moh Kolbehdari and Ruben Fuentes from Amkor's Tempe, Arizona Design Center for their design and simulation support. The authors would also like to thank Ron Huemoeller and JuHoon Yoon from Amkor's executive management team for their leadership and vision in pursuing SWIFT packaging technology.

## References

[1] J.-C. Souriau et al., "Wafer level processing of 3D system in package for RF and data Applications," 55th Electronic Components Technology Conference, Lake Buena Vista, FL, pp. 356-361, June 2005.
[2] T. Meyer et al., "Embedded Wafer Level Ball Grid Array (eWLB)," EPTC Proceedings, 2008, Singapore.
[3] A. Palesko, "An Analysis of Key Cost and Yield Drivers for Fan-Out Wafer Level Packaging," IWLPC Proceedings, October 2015.
[4] B. Baloglu et al., "Silicon Wafer Integrated Fan-out Technology," IWLPC Proceedings, October 2016
[5] Altera Corporation, "Designing for DDR4 Power and Performance," 2013.
[6] G. Findley, "General Memory (MASBZ01)," in Intel Developers Forum, San Francisco, 2016.
[7] Micron Technology, "TN-40-40: DDR4 Point-to-Point Design Guide DDR4 Layout and Design Considerations," Micron Technology, Boise, ID, 2015.

# Characterizations of Fan-out Wafer-Level Packaging

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*Huawei Technologies Co. Ltd.*

## *Abstract*

*The calling for smaller form factor, higher I/O density, higher performance and lower cost has made fan-out wafer level packaging (FOWLP) technology the trend. Good control of die position accuracy and molded wafer warpage are some of the keys to achieve high-yield production for FOWLP. In this study, 10mm x 10mm test chips were fabricated and attached (chip-first and die face-up) onto 12-inch glass wafer carriers using die-attach-film (DAF). These reconfigured wafers were compression-molded with selected epoxy molding compounds (EMC). Cu bumps (contact-pads) were revealed by grinding, and redistribution layers (RDLs) were fabricated by lithography and electroplating process. The fan-out wafers were evaluated and characterized after each process step with the main focus on the die-misplacement/die shift, re-configured wafer warpage, compression molding defects and RDL fabrication defects. The root causes of these defects were investigated and analyzed, while the possible solutions to overcome the defects were proposed and discussed.*

*Key words*

*Fan-out wafer level packaging (FOWLP), die-attach, compression molding, warpage control, RDL (re-distribution layer) process, defect characterization*

## I. Introduction

Die-shift/misalignment and warpage are the key points to achieve successful and high yield fan-out packaging devices [1, 2]. Die-attach pitch and position accuracy are important as the Cu bump (contact-pad) positions should match with the RDL masks, which are designed and cannot be modified [3]. Die-attach process should be carefully designed and controlled to meet the required tolerance. Warpage is another concern as it involves plenty of problems, including wafer handling difficulty and out-of-focus during RDL development. Warpage control has been widely investigated [4, 5], and it was reported that materials selection, fan-out ratio, package structure design and molding parameters are key factors for controlling the warpage within an acceptable level. Molding process is another step that might involve defects and cause yield loss or reliability failure in the fan-out packaging manufacturing process [6]. Understanding the physics leading to the deformation behavior in wafer-level molding is crucial for minimizing warpage through process optimization.

## II. Materials and Experiments

The schematic illustration of the chip-first and die-up/fan-out sample structure in this study is shown in Figure 1.

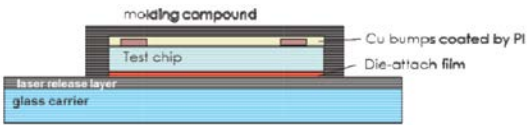


*Figure 1. Chip-first and die face-up sample structure.*

To achieve the designed structure, samples were fabricated by the following process steps:

### A. Test vehicle structure design and fabrication

In this study, a 10mm x 10mm Si chip was designed as the test vehicle. The die thickness is 150µm. There are 1988 pads on one chip, with a minimum pitch of 150um. The diameter of the Cu bumps (contact pads) is 60µm, and the height of the Cu bumps is 25 µm. The top-view of the test die is shown in Figure 2. Daisy-chains on the chip and RDL layout were designed as well for yield verification and reliability test.

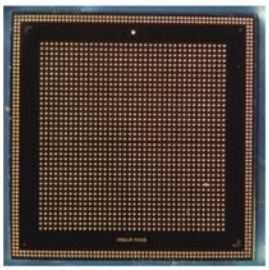

*Figure 2. Top view of the 10mm x 10mm test chip with Cu bumps.*

### B. Die-attach process

One reconstructed wafer contains 325 units of test chips populated on a 12-inch glass carrier. The package outline is 13.42mm x 13.42mm with a fan-out ratio of 1.8.

Glass wafer carriers were used in the die-attach process. Carriers (die-attach side) were coated by 3M light-to-heat-conversion (LTHC) layer, as the molded fan-out wafer need to be released by laser from the glass carrier

before package singulation. The test chip vehicle wafer was grinded to 150μm and DAF was laminated to the backside of the wafer. Carriers of 3 different coefficient thermal expansion (CTEs) values, including 3.25ppm/°C, 7.6ppm/°C and 8.1 ppm/°C, were used for the sample building. The die-attach process was carried out at 120°C (both bond-head and the bond-stage) with the bond force of 2.0 kg and the bond time of 2000ms, using an ASM Nucleus multi-purpose precision die-bonder.

After die attach, post-cure was carried out at 125°C for 1 hour, die position data were then collected at room temperature (25°C). Bonding quality was checked by die-shear test and die-tilt measurement.

### C. Molding process

The molding process was carried out using an ASM ORCAS molding machine. The illustration of the mold chase set-up is shown in Figure 3. First, the glass carrier (die-attached) was fixed onto the top mold chase by vacuum. Then the molding compound was dispensed on the bottom plunger. Compression molding was then carried out with different molding speeds and packing forces. Molding temperature was 120°C and the mold clearance (from die-top to mold surface) was controlled at 100μm. KOZ (keep-out-zone) method was used and the mold cap diameter is Ø295mm (2.5mm clearance from the 12-inch glass carrier edge). The samples were then put into post-mold-cure process with 15kg deadweight, for a better warpage control. After cooling to room temperature, warpage level of the fan-out wafers were measured, and molding quality was then checked by optical microscope and C-SAM.

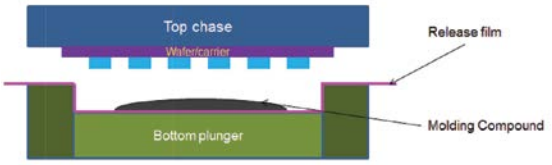


*Figure 3. Mold chase set-up illustration.*

### D. Grinding and RDL process

Grinding and polishing processes were carried out on a Disco grinder. Cu bumps were revealed and the grinding quality was checked by optical microscope.

RDL layers were then built by stepper lithography and plating process. The alignment accuracy and quality of RDL layers were checked and verified, before moving to the next step.

## III. Results and Discussion

### A. Carrier material selection

It was widely mentioned that CTE of the glass carrier affects the warpage of the molded fan-out wafer [7, 8]. Hence, simulation was carried out to estimate the best carrier CTE, molding compound CTE and the package thickness, as have already been included in our previous publication [5].

The model was established based on this packaging structure design, and the simulation result of CTE's effect on warpage level is shown in Figure 4. Based on the simulation result and glass carrier availability, three different glass carriers, with CTE of 3.25ppm/°C (for comparison), 7.6ppm/°C and 8.1ppm/°C (close to the optimized CTE by simulation result) were used for this evaluation.

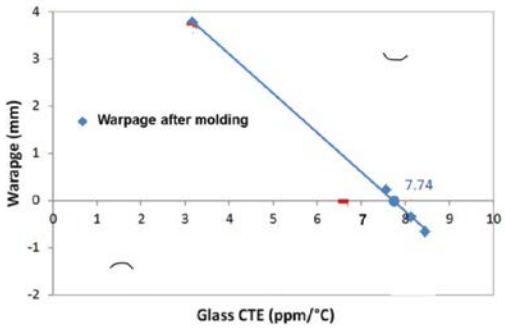


*Figure 4. Simulation of glass carrier CTE on molded wafer warpage (EMC volume shrinkage was assumed to be 0.27%).*

### B. Re-constructed wafer and die-attach process

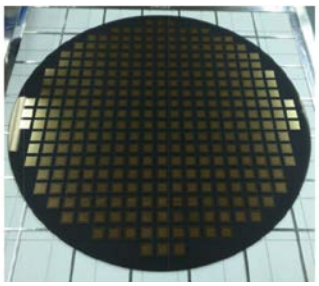

*Figure 5. Re-constructed wafer after die-attach process.*

The reconstructed wafer was shown in Figure 5. The X and Y pitch offset (the measured pitch subtracted from the designed pitch) was plotted against the column and row, separately, as shown in Figure 6(a). Without pitch compensation, large position offset (~100 μm) was observed. Since die-attach was performed at 120°C, but the final pitch aligned for RDL process was carried out at room temperature. Therefore, pitch compensation (caused by heating during die-attach process) was needed which can be calculated by the following equation:

$$P_A = P_R + \alpha_L \Delta T$$

where $P_A$ is die-attach pitch, $P_R$ is the designed RDL pitch, $\alpha$L is the linear thermal expansion coefficient of the glass carrier, $\Delta T$ is the temperature difference between die-attach temperature and RDL temperature.

From the equation, it clearly showed that the accurate temperature control for both die bonding and RDL process are affecting significantly on the pitch compensation. Results in Figure 6(b) were obtained after compensation and process optimization, the placement offset was reduced from ±100μm (without pitch compensation) to ±4.0 μm (with pitch compensation), and this is a good performance that can meet the process specifications.

Die-shear test was performed to assess the bonding strength, as the dice were subjected to a shear force during the compression molding process. Shear speed used was 300μm/s and shear height was 40μm. For all the dice tested, the shear force was larger than 80kg, which could ensure the die-position stability during molding process as explained in the next molding session.

It is important to ensure the leveling of the Cu bumps on a same plane, as the molded wafers would be grinded to reveal the Cu bumps for RDL process. In this study, there are several factors that might contribute into the Cu bump leveling variation:

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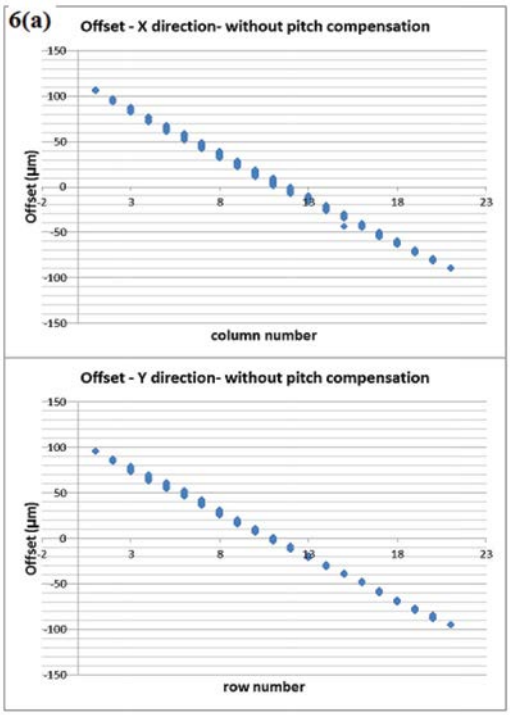


*Figure 6(a). Position offset data: X and Y direction (without pitch compensation).*

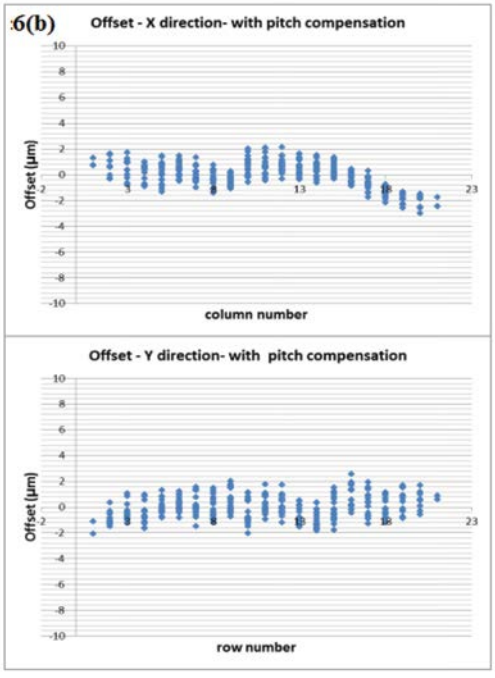


*Figure 6(b). Position offset data: X and Y direction (with pitch compensation).*

a. Total thickness variation (TTV) of the glass carrier. In this study, the glass TTV is less than 3.0µm as provided by the vendor.
b. Thickness variation of DAF material.
c. Thickness variation of Si chips. In this study, the thickness variation of the test chips was measured and the variation range is 9.3µm.
d. Cu bump plating variation. In this study, the Cu bump height variation range is 5.3µm as measured.
e. Die-tilt during die-attach process.

Die-tilt is one of the main causes of leveling variation of the Cu bumps. If there's die-tilt during die-attach process, the bumps could not be exposed at the same time during grinding process, even within one die. The die tilt defect was observed on the preliminary samples of this study, as shown in Figure 7(a). After process optimization, die tilt could be controlled much better to eliminate Cu bump exposure failure. The maximum leveling difference on the whole wafer could be controlled within 11.2µm. The Cu revealing with optimized die tilt is shown in Figure 7(b). This leveling variation range is acceptable for this project, as it could be compensated by the Cu bump height, which is 25µm.

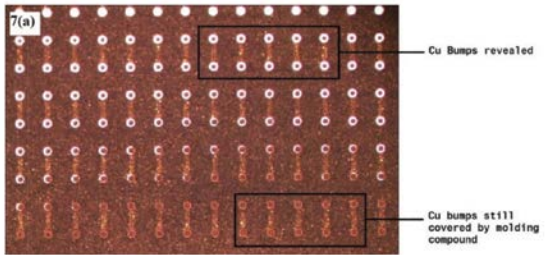


*Figure 7(a). Cu-bump revealing defect caused by die-tilt.*

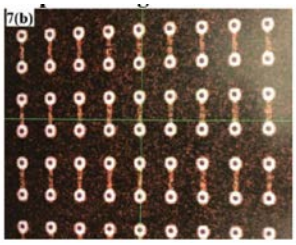


*Figure 7(b). Cu-bump revealing with optimized die tilt level.*

### C. Molding process and characterization

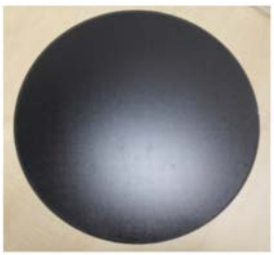

*Figure 8. Molded fan-out wafer.*

The molded wafer sample is shown in Figure 8. Molding quality was characterized in the following areas: incomplete fill, molding voids, warpage, and die shift after molding.

Incomplete fill is an important issue for fan-out wafer quality. Before optimization of the molding parameters (dispensing pattern, molding speed and packing force), coverage defects on top of the die were observed by optical microscope. Some of the incomplete fill points are at Cu bump positions and causing Cu bumps visible at top-view, as shown in Figure 9. The un-covered Cu bumps were easily damaged during grinding process and lead to yield loss.

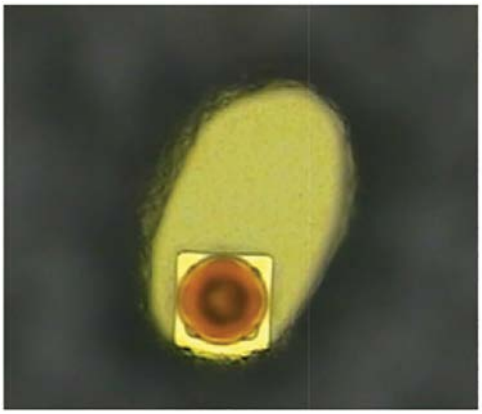

*Figure 9. Top view of the Cu bump exposed at the incomplete fill defect.*

Inspections for molding voids were carried out by C-mode scanning acoustic microscope (C-SAM). To balance the resolution and signal penetration depth, a transducer of 75MHz was selected for the voids observation. Before molding parameter optimization, around 10 molding voids were detected in each of the molded wafers, especially located at the die-edge. The corners between wafer-carrier and die-edge could trap voids easily when liquid molding compound flows rapidly. Acoustic signals at suspicious void positions and normal positions were captured and compared, as shown in Figure 10. During process optimization, it was found that the incomplete fill and voids could be eliminated when the packing pressure was between 40 to 50 kg/cm2 with a circle dispensing pattern.

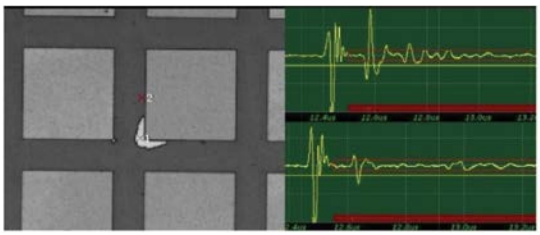

*Figure 10. Scanning acoustic microscope observation of the molding voids.*

Thicknesses of the molded wafers were checked and confirmed. After that, warpage of the molded wafers were measured using a Shadow Moiré system and contour was plotted. It has already been discussed in our former report that warpage after molding can be affected by glass carrier CTE and thickness, fan-out ratio, die thickness and molding thickness [5].

In this research, glass carriers with CTE = 3.25ppm/°C, 7.6 ppm/°C, and 8.1ppm/°C were used for sample building. After post-mold-cure with deadweight, the warpage of CTE 3.25ppm/°C carrier wafers were larger than 3mm and the warpage of CTE 7.6 ppm/°C and 8.1 ppm/°C glass carriers can be controlled within 0.4 mm. The data align with the simulation result [5]. Wafers with warpage under 0.5mm are acceptable for the following RDL processes requirements. Warpage data were collected by measuring the z leveling of the sample surface, and the contour of CTE 8.1 ppm/°C and CTE 3.25 ppm/°C glass carrier samples were plotted as Figures 11(a) and (b). Average warpage level of molded samples with different glass carriers are listed in Table I. The result proved that it is a must to optimize glass carrier CTE to control warpage level.

| Glass CTE | average warpage level |
|---|---|
| 3.25ppm/°C | 4.003mm |
| 7.6 ppm/°C | 0.380mm |
| 8.1ppm/°C | 0.250mm |

*Table I Average Warpage Level of Molded Samples with Different Glass Carriers (Measured Result)*

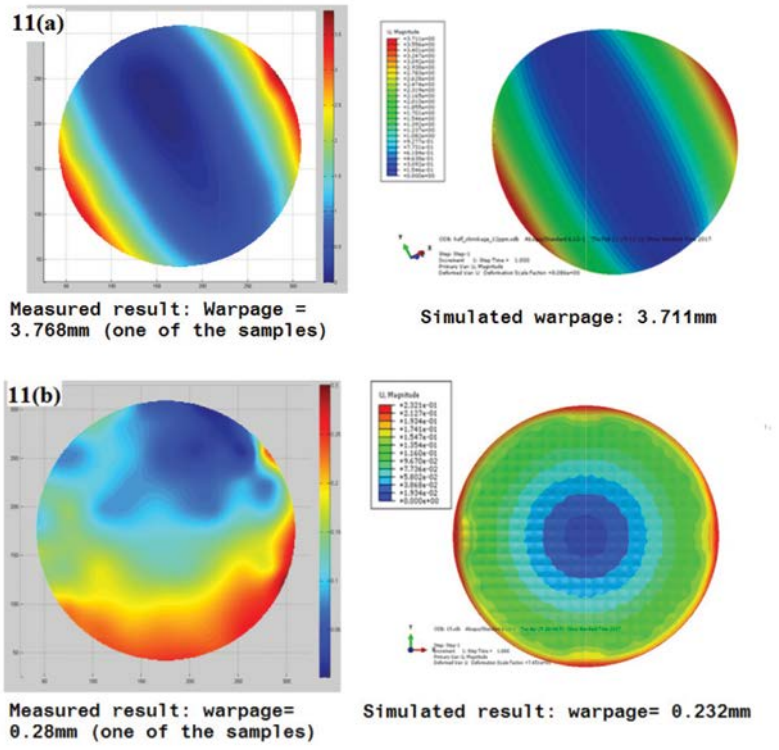


*Figure 11. Measured warpage and simulation contour of the molded wafers with (a) carrier CTE of 3.25ppm/°C and (b) carrier CTE of 8.1ppm/°C.*

For chip-first and die face-down, die-shift was reported by Robert L. Hsieh and his colleagues [1], that the location-change of the chips from the designed position causes alignment problem in the RDL exposure processes. In this study (chip-first and die face-up with DAF), the position of each die was recorded before and after molding. Then the die-shift caused by the molding process was calculated by deducting the position coordinates before-and-after. Molding caused die-shift data were then statistically plotted in Figure 12. It was proved (together with the die-shear test result) that the adhesion between die and carrier is very strong. The position difference could be controlled within ±4.0um. It is within the expected

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tolerance and acceptable for the RDL process, based on the designed Cu diameter size and sample structure in this study.

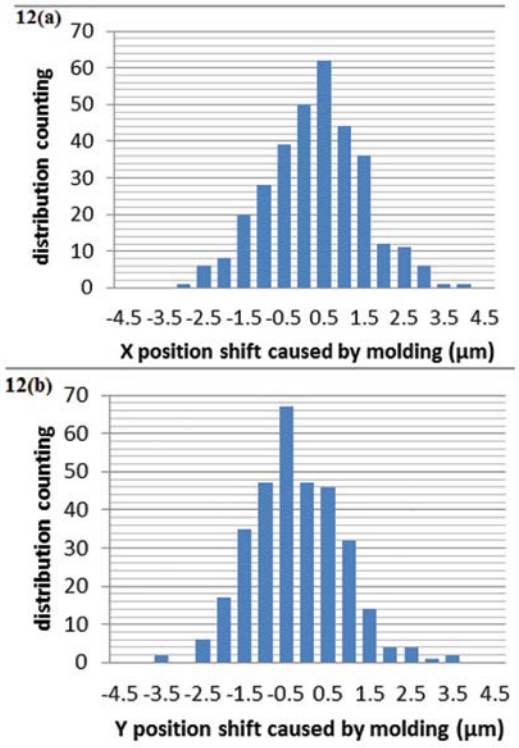


*Figure 12. Molding induced die-shift distribution data (a) X direction and (b) Y direction.*

**D. Grinding and RDL characterization**

Grinding process quality was checked by optical microscope and Cu smear was observed before parameter optimization, as Figure 13(a) shows. It was found that Cu smear issue could be eliminated by optimizing grinding wheel and polishing process, together with soft etching. The optimized result is shown in Figure 13(b).

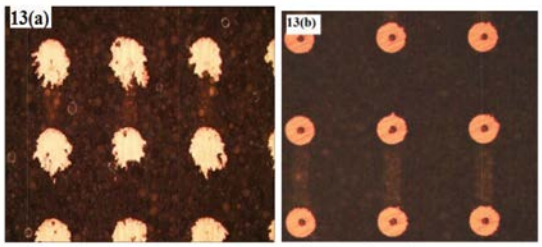


*Figure 13. (a) Cu smear during grinding process; (b) optimized Cu exposure result.*

In the RDL process, quality issues include exposure misalignment, development opening size error or residue, electroplating thickness control and over-etching/residue in etching process.

In this study, misalignment was checked by optical microscope, and it was found that the first RDL mask alignment accuracy was affected by the grinding quality. Cu smear might cause difficulty in the alignment mark matching, and lead to misalignment in exposure process. The misaligned exposure and accurately aligned RDL pattern were shown in Figures 14(a) and 14(b). Development process quality and etching quality were also evaluated by microscope. Cu RDL layer thickness was checked and confirmed by 3D profiler system, after each plating process.

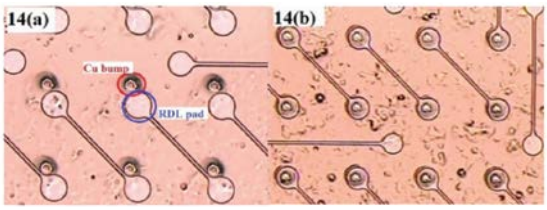


*Figure 14. RDL pattern with (a) misaligned exposure and (b) accurately aligned exposure.*

After RDL fabrication and solder ball mounting, the fan-out wafers were released from the carriers by laser-debonding process. 355nm DPSS Nd: YAG UV laser source was used. The laser spot-size was 240µm, the scanning speed was 500mm/s and the scanning pitch was 100µm. The laser-debonded wafer is shown in Figure 15(a). The units on the fan-out wafer were diced into singulated packages, as shown in Figure 15(b), and tested for daisy-chain continuity.

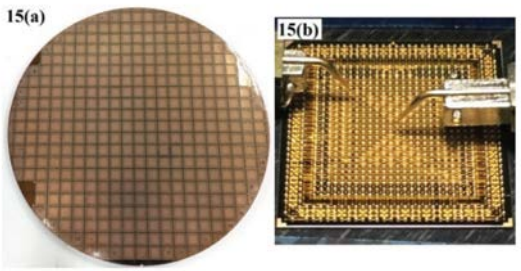


*Figure 15. (a) laser-debonded fan-out wafer and (b) singulated package and continuity testing.*

## IV. Conclusions

In this study, fan-out wafer level packaging samples were fabricated and the process quality after each process step was characterized. Results are summarized in the following:

- Die-attach accuracy and pitch compensation are key issues that need to be evaluated and controlled, for the position accuracy in RDL process. Factors including bond-stage temperature accuracy, RDL process temperature control and glass carrier CTE affect the compensation accuracy.
- Die tilt is an important factor that affects Cu bump (contact-pad) revealing (during grinding), and the die-bonder should be carefully optimized to control the leveling.
- Die-attach strength was verified by die-shear test, as die position should be kept accurate during molding.
- The position data before and after molding was compared, and it was proved that molding induced die-shift could be controlled within an acceptable level.
- Apart from die shift during molding, there are two other concerns for the molding process: warpage level and voids. CTE of the glass carriers should be optimized based on simulation in order to minimize wafer warpage.

- For the designed fan-out ratio and package structure in this research, samples which were built with optimized carrier CTE showed very low warpage level and samples with large CTE mismatch warped severely. Molding compound selection is another factor that is important for the warpage control. Molding voids were characterized by optical microscope and scanning acoustic microscope. Defects can be eliminated by optimizing the molding process parameters.
- De-bonding of the glass carrier from the fan-out molded wafer has been successful performed by a YAG UV laser.

**Acknowledgment**

The authors would like to thank the kindness of 3M, Nagase, Hitachi, and Disco for providing them with useful help and materials for this project.

**References**

[1] Hsieh, R., D. Fuchs, W. W. Flack, and M. Ranjan, "Lithography Challenges and Considerations for Emerging Fan-Out Wafer Level Packaging Applications," *Proceedings of International Wafer Level Packaging Conference,* 2009 (Oct).

[2] Che, F., D. Ho, M. Ding, D. MinWoo, "Study on Process Induced Wafer Level Warpage of Fan-Out Wafer Level Packaging," *Proceedings of IEEE/ECTC,* May 2016, pp. 1879-1885.

[3] Flack, W., R. Hsieh, G. Kenyon, K. Nguyen, M. Ranjan, N. Silva, and P. Cardoso, et al., "Lithography technique to reduce the alignment errors from die placement in fan-out wafer level packaging applications," *Proceedings of IEEE/ECTC,* May 2011, pp. 65-70.

[4] Farrugia, R., I. Grech, O. Casha, E. Gatt, J. Micallef, I. Ellul, R. Duca, and I. Borg, "The analysis of warpage in wafer-level compression molding, *Microsystem Technology,* December 2015, pp. 1-10.

[5] Lau, J. H., M. Li, D. Tian, N. Fan, E. Kuah, W. Kai, M. Li, J. Hao, et al., "Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* pp. 1-10.

[6] Boyd, R., C. Scanlan, and T. Olson, "Implementation of a fully molded fan-out packaging technology" *Proceedings of International Wafer-Level Packaging Conference,* 2013 (Nov).

[7] Li, H., A. Chen, S. Peng, G. Pan, and S. Chen, "Warpage Tuning Study for Multi-chip Last Fan Out Wafer Level Package," *Proceedings of IEEE/ECTC,* May 2017, pp. 1384-1391.

[8] Hayashi, K., "Carrier glass substrates for fan-out wafer/panel level packaging," *International Conference on Electronics Packaging (ICEP),* 2017, pp. 494-497.

# nnovative Integration Solutions for SiP Packages Using Fan-Out Wafer Level eWLB Technology

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## *Abstract*

*Fan-Out Wafer Level Packaging (FOWLP) has been established as one of the most versatile packaging technologies in the recent past and already accounts for a market value of over 1 billion USD due to its unique advantages. The technology combines high performance, increased functionality with a high potential for heterogeneous integration and reduced overall form factor as well as cost effectiveness. The increasing complexities in achieving a higher degree of performance, bandwidth and better power efficiency in various markets are pushing the boundaries of emerging packaging technologies to smaller form factor packaging designs with finer line/width spacing as well as improved thermal/electrical performance and the integration of System-in-Package (SiP) or 3D capabilities.*

*SiP technology has been evolving through utilization of various package technology building blocks to serve the market needs with respect to miniaturization, higher integration, and smaller form factor as cited above, with the added benefits of lower cost and faster time to market as compared to silicon (Si) level integration, which is commonly called system-on-chip or SoC. As such, SiP incorporates flip chip (FC), wire bond (WB), and fan-out wafer-level packaging (FOWLP) as its technology building blocks and serves various end applications ranging from radio frequency (RF), power amplifiers (PA), Micro-Electro-Mechanical-Systems (MEMS) and sensors, and connectivity, to more advanced application processors (AP), and other logic devices such as graphics processing units (GPUs)/central processing units (CPUs). FOWLP, also referred to as advanced embedded Wafer Level Ball Grid Array (eWLB) technology, provides a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D SiP configurations.*

*This paper presents developments in SiP applications with eWLB/Fan-out WLP technology, integration of various functional blocks such as wire bonding, Package-on-Package (PoP), 2.5D, 3D, smaller form factor, embedded passives, multiple redistribution layer routing and z-height reduction. Test vehicles have been designed and fabricated to demonstrate and characterize these low profile and integrated packaging solutions for mobile products including Internet of Things (IoT)/wearable electronics (WE), MEMS and sensors. Finer line/width spacing of 2/2mm with multiple redistribution layers (RDL) are fabricated and implemented on the eWLB platform to enable higher interconnect density and signal routing. Assembly process details, component level reliability, board level reliability and characterization results for eWLB SiP will be discussed.*

## I. Introduction

The semiconductor industry is constantly faced with complex integration challenges as consumers want their electronics to be smaller, faster and higher performance with more and more functionality packed into a single device. The demand for such requirements has driven many new trends and innovations in advanced packaging technology.

One of the solutions is System-in-Package (SiP). System-in-Package is a functional electronic system or subsystem that includes two or more heterogeneous semiconductor die (often from different technology nodes optimized for their individual functionalities), usually with passive components. The physical form of the SiP is a module, and depending on the end application, the module could include a logic chip, memory, integrated passive devices (IPD), RF filters, sensors, heat sinks, antennas, connectors and/or power chip in packaged or bare die form. This paradigm shift from chip scaling to system level scaling will continue to reinvent microelectronics packaging and help sustain Moore's Law [7]. The challenge of the semiconductor industry is to develop a disruptive packaging technology capable of rapidly achieving these goals.

To meet the above challenges, embedded Wafer Level Ball Grid Array (eWLB) is a technology platform that offers additional space for routing higher input/output (I/O) on top of the silicon chip area which is not possible in conventional wafer level packaging or wafer level bump. Figure 1 shows the eWLB packages and package evolu-

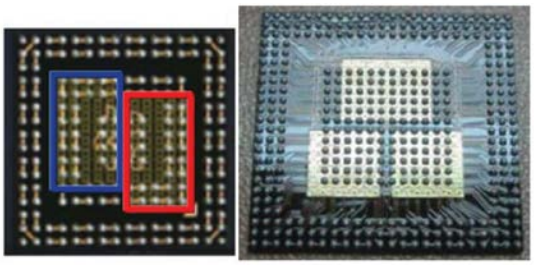

*Figure 1a. SiP in eWLB.*

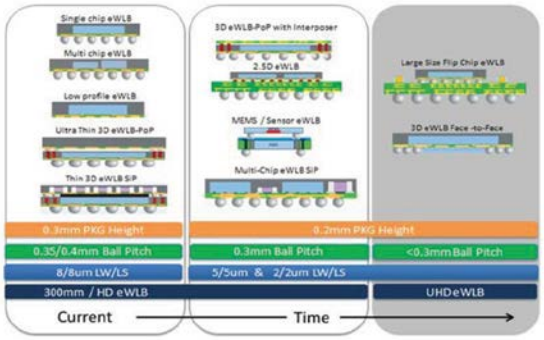


*Figure 1b. SiP in eWLB trend.*

tion to 2.5D and 3D SiP. eWLB also offers comparatively better electrical, thermal and reliability performance at a reduced cost with the possibility to address additional advanced technology Si nodes with low k-dielectrics in a multi-die or 3D eWLB package.

**Embedded Wafer Level BGA (eWLB) Technology**

Fan-Out eWLB is an innovative approach designed to provide flexibility to accommodate an unlimited number of interconnects between the package and the application board for maximum connection density, finer line/width spacing, improved electrical and thermal performance and small package dimensions. A Wafer Level Chip Scale Package (WLCSP) structure, also known as Fan-In Wafer Level Packaging, is compared to a Fan-Out eWLB structure in Figure 2.


*Figure 2. Fan-In WLP vs. Fan Out-WLP.*

Unlike conventional WLCSP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Following singulation, an artificial wafer (or panel) is then created by embedding the diced silicon chips onto a blank metal carrier. The main reconstitution steps shown in Figure 3 include:

1) The reconstitution process starts by laminating an adhesive foil onto a carrier (artificial wafer/panel).
2) Singulated die are placed faced down with a pick and place tool.
3) Die are encapsulated with molding compound.
4) After curing the mold compound, the carrier and foil are removed, resulting in a reconstituted wafer. The molding compound will only surround exposed die surfaces.

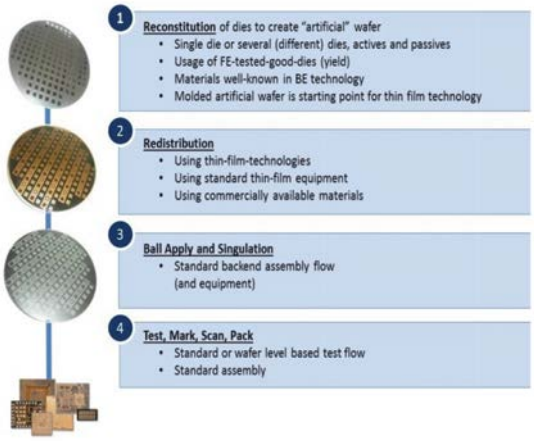


*Figure 3. Process flow for eWLB.*

## II. Various Applications of eWLB in SiP

**Mobile RF, PMIC, Connectivity**

eWLB/FOWLP in a SiP configuration is a growing trend for advanced application processors, MEMS and sensors in IoT/WE as a way to cost effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor [7].

Figure 4 shows a 3D eWLB SiP/module with several discrete components in the top package and is pre-stacked on the bottom eWLB-PoP to form a 3D SiP/module with a thin package profile of 1.0mm total height. Twelve discretes, including inductors and multilayer ceramic capacitors (MLCCs) were removed from the motherboard and relocated in the top package for a reduction in space on the motherboard.

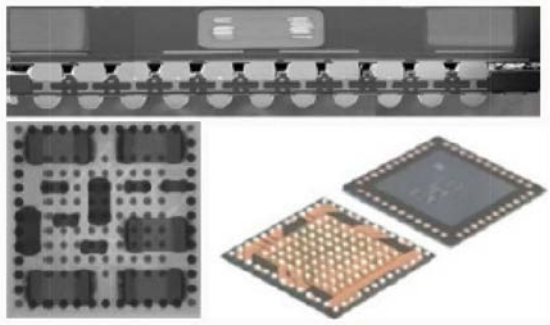

*Figure 4. 3D SiP eWLB-PoP with discretes in interposer on top package.*

The discretes are also more power efficient when they are close to the device, significantly improving the overall electrical performance as well as providing a power saving advantage.

Functional test samples were prepared with power management integrated circuit (PMIC) as shown in Figure 4. The SiP has a 6mm x 6mm body size with a 4mm x 4mm Si die and 12 discretes on the top. This eWLB SiP demonstrated more power efficiency performance compared to other embedded package technology and is representative of a significantly smaller package solution [5,7].

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**MEMS/Sensor eWLB**

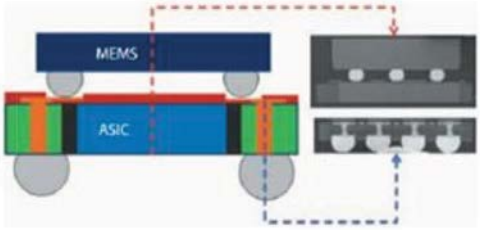


*Figure 5. 3D eWLB for MEMS/sensor devices [2].*

Figure 5 illustrates an eWLB sensor which has been miniaturized from the original side-by-side land grid array (LGA) package. It has a 3D vertical interconnection and multi-die stacking. It provides over 20% footprint reduction and less than 1mm thickness with a lower cost high volume manufacturing (HVM) solution. The smaller body sizes (5mm/side or less) are typically a good fit for sensor devices such as health monitoring and environmental sensors.

Since sensor devices typically require at least a two chip solution (example application specific integrated circuit and MEMS/Sensing silicon), advanced eWLB/FOWLP stack up solutions can enable a very small pitch LGA and ball grid array (BGA) eWLB PoP footprint at a competitive cost vs. the incumbent wire bond solutions.

The package architecture enables routing on both sides of the package by embedding a direct via across the top to pad side of the package. The top MEMS device is bumped through standard lead frame wafer processing, singulated and assembled by pick and place tooling and reflow on the application specific integrated circuit (ASIC) in the eWLB bottom package. This assembly will eliminate the need for die attach material, assembly wires, protective glob-top and also the typical metal cap or molded package with access cavity thus removing the typical laminate or leadframe for routing. Consequently, 3D eWLB SiP offers a much smaller footprint, simplified bill of material and is assembled with a cost competitive panel level manufacturing process [7,10].

**Integrated Passives in eWLB-SiP**

In mobile applications for GSM/WCDMA /EDGE technologies, many functional blocks such as Power Amplifier (PA), Baluns, transceiver, filters, etc., play a key role in the performance of the module. Even though a PA made from gallium arsenide (GaAs) is widely used due to its good electrical and thermal properties, they are quite expensive. In an RF circuit, a power amplifier has an impedance matching circuit consisting of capacitors and inductors which consume a significant portion of the die size and can be potentially replaced by an IPD and successfully used for RF modules/SiP in PA impedance matching and coupling circuits [8].

For this PA module, a multi-chip eWLB has been developed with a PA and IPD integrated side-by-side.

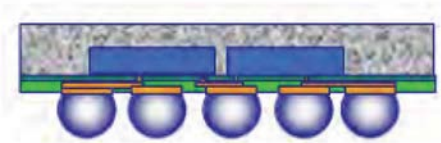

*Figure 6. Side view of PA and IPD in SIP.*

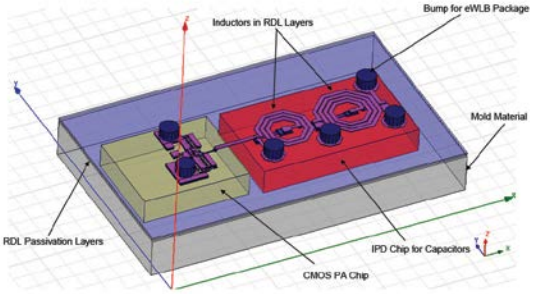


*Figure 7. Illustration of a PA die and silicon IPD die embedded in mold substrate.*

Figures 6 and 7 illustrate an eWLB package, which includes a PA chip and an IPD chip. The IPD die mainly serves as an impedance matching network for the PA.

In this multi-die eWLB package the connection from the RDL to the PA chip is made through the via connecting the RDL layer and the top metal layer in the PA chip. The connection between the RDL and the IPD chip is made through via connecting the RDL layer and the top thick metal layer in the IPD. There are three different substrates in this package: a complementary metal-oxide-semiconductor (CMOS) substrate; IPD substrate; and mold compound substrate are shown in Figure 7. The passivation redistribution layers are fabricated through a standard thin film process, plating in wafer fabrication process, thus forming a multi-die eWLB package after standard backend processes.

**2/2um Line Width and Spacing (LW/LS) with 3-Layer RDL [2]**

High I/O with fine pitch area array continues to be one of the greatest challenges in wafer level packaging. Redistribution layer (RDL) allows signal and supply I/Os to be redistributed to a footprint larger than the chip footprint in eWLB. Required line widths and spacing of 2/2um for eWLB applications support the bump pitch of less than 40um. Finer line width and spacing are critical for multi die design and routing flexibility.

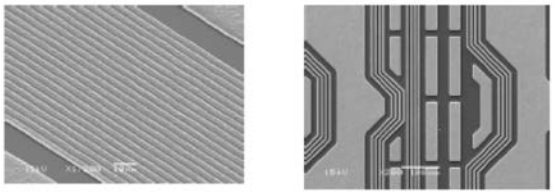

*Figure 8. SEM of 2/2um LW/LS RDL with coarser RDL LW/LS.*

Figure 8 shows 2/2um (LW/LS) alongside coarser LW/LS in eWLB/FOWLP. Scanning Electron Microscope (SEM) images show uniform and well defined micro structure. Copper (Cu) RDL thickness and critical dimensions (CD) are also well controlled with verified process robustness using current HVM equipment and process flow [7].

## III. Reliability Performance

**Electrical Performance of 3D eWLB PoP/SiP vs. fcPoP**

The RLC parasitic values for eWLB-PoP/SiP and flip chip package-on-package (fcPoP) were extracted by computer simulation using commercial 2D electromagnetic field solver. The S-parameter of each package was extract-

ed by using ANSOFT HFSS. Simulated results are compared with RLC parasitic values and S parameters (Table 1). The simulation modeling design was carried out with functional devices to investigate package level performance in real applications. In 3D simulation works, a few critical pins were selected and evaluated, such as clock, VDD as well as Data pins [7].

| Net | Inductance, L (nH) | | | Resistance, R (mΩ) | | |
|---|---|---|---|---|---|---|
| | fcPoP | eWLB -PoP | Δ (%) | fcPoP | eWLB -PoP | Δ (%) |
| 1 | 1.77 | 0.43 | -76% | 240 | 67 | -72% |
| 2 | 2.03 | 0.24 | -88% | 308 | 42 | -86% |
| 3 | 1.51 | 0.57 | -62% | 348 | 112 | -68% |
| 4 | 1.08 | 0.25 | -77% | 268 | 66 | -75% |

*Table 1. Electrical Parasitic Values of RLC of eWLB-PoP/SiP vs. fcPoP @ 1GHz*

For signal integrity study with specific data pins, eWLB showed more than 10dB better cross-talk than flip chip due to its thinner CuRDL and overall shorter interconnection length as shown in Figure 9. In addition, smooth CuRDL surface of wafer fab process contributed significantly with less conductance loss.

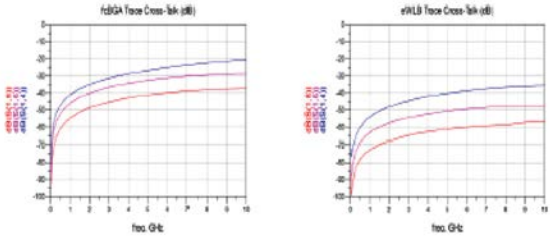

*Figure 9. The cross-talk with frequency of signal routing of (a) flip chip and (b) eWLB.*

### Board Level Reliability of 3D eWLB-PoP/SiP

For board level reliability tests, eWLB-PoP (stacked with top package) was pre-stacked with top memory and mounted on the printed circuit board (PCB). For PoP assembly, a 0.4mm body thickness Fine Pitch Ball Grid Array (FBGA) top package was assembled separately with standard wirebonding process and finally pre-stacked on eWLB-PoP bottom package. The total eWLB-PoP stacked package height was less than 0.8mm in height after surface mount technology (SMT) manufacturing on the PCB. Those samples were tested in JEDEC Temperature Cycling on Board (TCoB) and drop test reliability conditions.

| Tests | Conditions | Status |
|---|---|---|
| TCoB | JEDEC JESD22-A103 -40°C to 125°C | Pass |
| Drop Test | JEDEC JESD22-B111 1500G | Pass |

*Table 2. Board Level Reliability Test Results of 3D eWLB PoP/SiP*

Table 2 shows 3D eWLB-PoP board level reliability of JEDEC TCoB and drop test results of test vehicles 1 and 2. The first TCoB failure was after 1000 cycles. Drop reliability performance was robust and showed no failure after 300 drops. These test results show the robustness of board level reliability of 3D eWLB-PoP [7].

## III. Conclusions

eWLB technology is addressing a wide range of packaging concerns, from packaging cost to test. In parallel, there are physical constraints such as its foot print and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for small ships with a high pin count as need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency).

Advanced low profile and integrated 3D eWLB-PoP/SiP was developed using eWLB/FOWLP Technology. 3D reliability conditions board level reliability tests of pre-stacked PoP were run through JEDEC standard conditions and showed robust reliability in TCoB and drop tests. Electrical characterizations were also performed with functional devices and signal integrity simulation and showed enhanced performance of 3D eWLB-PoP compared to conventional fcPoP devices. Integrated Passives with PA modules in eWLB-SiP show impedance improvement and passed Board Level Reliability (BLR) requirements.

Advanced eWLB SiP technology provides a smaller form factor and increased performance value, proving to be a new SiP packaging platform than can expand its application range to various types of emerging mobile, Internet of Things, Wearable Electronic applications, MEMS/sensors or automotive applications [9].

## References

[1] M. Brunnbauer, et al., "Embedded Wafer Level Ball Grid Array (eWLB)," Proceedings of 8th Electronic Packaging Technology Conference, 10-12 Dec 2009, Singapore (2006).

[2] Seung Wook Yoon, Meenakshi Padmanathan, Andreas Bahr, Xavier Baraton and Flynn Carson, "3D eWLB (embedded wafer level BGA) Technology: Next Generation 3D Packaging Solutions," San Francisco, Proceedings of IWLPC 2009 (2009).

[3] Meenakshi Prashant, Seung Wook Yoon, Yaojian Lin and Pandi C. Marimuthu, "Cost effective 300mm large scale eWLB (embedded wafer level BGA) Technology," Proceedings of 13th EPTC 2001, Singapore Dec (2011).

[4] Hamid Eslampour, SeongMin Lee, SeongWon Park, TaeKeun Lee, InSang Yoon, VoungChul Kim, "Comparison of Advanced PoP Package Configurations," Proceedings of ECTC 2010, Reno, US (2010).

[5] Yaojian Lin, Chen Kang, Linda Chua, Won Kyung Choi and Seung Wook Yoon, "Advanced 3D eWLB-PoP (embedded wafer level BGA – Package on Package) Technology," Proceedings of ECTC 2015, Las Vegas, US (2016).

[6] W.K. Choi, DJ Na, KO Aung, Andy Yong, Jaesik Lee, Urmi Ray, Riko Radojcic, Bernard Adams and Seung Wook Yoon, "Ultra Fine Pitch RDL Development in Multi Layer eWLB (embedded wafer level BGA) Packages," Proceedings of IMAPS 2015, Orlando, US (2015).

[7] Yaojian Lin, Chen Kang, Linda Chua, Won Kyung Choi and Seung Wook Yoon, "3D Integrated eWLB/FO-WLP Technology for PoP and SiP," Proceedings of ICEPT 2016, Wuhan China (2016).

[8] Meenakshi Prashant, Kai Liu, Seung Wook Yoon and Raj Pendse, "Integrated Passive Devices (IPD) Integration with eWLB (Embedded Wafer Level BGA) for High Performance RF Applications," Proceedings of EPTC 2010, Singapore (2010).

[9] Seung Wook Yoon, Boris Petrov, Kai Liu, "Advanced Wafer Level Technology: Enabling Innovations in Mobile IoT and Wearable Electronics," Chip Scale Review, May/June 2015, pp 54-57 (2015).

[10] Babak Jamshidi, "Fan-Out Wafer Level Packaging Enables MEMS and Sensors to Meet Future IoT Requirements," MEPTEC Report Summer 2016, p23-24 meptec.org (2016).

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## Advanced Technical Workshop on

# *Advanced Packaging for Medical Microelectronics*

www.imaps.org/medical

## January 23-24, 2018

Handlery Hotel, San Diego, California

**General Co-Chairs**:
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**Organizing Committee:**
Steve Annas, Samtec | Matt Apanius, SMART Microsystems | Caroline Bjune, Draper |
Rick Elbert, Cicor | Tim LeClair, Cerapax | Vern Stygar, Asahi Glass Company

***Program and Registration Online – Exhibits/Sponsorships Still Available***

**Overview:** The International Microelectronics Assembly and Packaging Society (IMAPS) will host an Advanced Technical Workshop in San Diego on ***Advanced Packaging for Medical Microelectronics*** on January 23 and January 24, 2018. The workshop will bring together technologists in semiconductor packaging with life science experts interested in applying advanced packaging methods to enable the next generation of medical microelectronic devices. The workshop will provide a venue for presentations and discussions focused on traditional and emerging packaging technologies for wearable, portable and implantable devices, medical instrumentation, and life sciences consumables. Attendees and Exhibitors will be exposed to a wide variety of disciplines to encourage new products, discussions and collaborations. This two-day event will draw invited experts in medicine, sensing, microelectronics, and semiconductor packaging. Session are planned on:

| Implantable Devices | Diagnostic and In Vivo | Portable and Wearable | Technology |
|---|---|---|---|
| Pacemakers and Defibrillators | Interventional Catheters | Remote Diagnostics | Biosensors and MEMS |
| Neurostimulators | Pillcams | Defibrillators | Batteries and Energy Harvesting |
| Deep Brain Stimulation | Ultrasound and Imaging | Point of Care | Biocompatible Materials |
| Drug Delivery | Lab-on-Chip | Patient Monitoring | Encapsulation/Hermeticity |
| Cochlear Implants | Micro Reactors | Ambulatory Care | HDI Flex and Packaging |
| Retinal/Ophthalmic | Surgical Devices | Hearing Aids | Wireless Communications |
| Electroceuticals and Injectables | | Neurostimulators | Reliability |
| | | Prosthetics | |

***Program and Registration will be available at: www.imaps.org/medical***

*Priced at $550 for IMAPS members, $650 for non-members, and $300 for speakers, attendance will be limited to maintain a workshop atmosphere. Workshop will feature panel discussions for increased open engagement and networking. 20 tabletop spaces are available this year to allow for more company participation. For further information and to submit abstracts or to register, visit www.imaps.org/medical or email bschieman@imaps.org.*

*Topical Workshop & Tabletop Exhibition on*

# WIRE BONDING

www.imaps.org/wirebonding

**October 8, 2018**
**Pasadena Convention Center, Pasadena, CA**

**General Chair:**
**Lee Levine |** Process Solutions Consulting | Phone: 610-248-2002 | levilr@ptd.net

**Wire Bonding Workshop Organizing Committee:**
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## ABSTRACTS DUE: MARCH 30, 2018

***New 1-Day Workshop Format – Maximum of 12 Speaking Spots Available***

**Wire Bonding Workshop Focus:**
The objective of the Wire Bonding Workshop is to have a unique forum that brings together scientists, engineers, manufacturing, academia, and business people from around the world who have been working in the area of Wire Bonding. This workshop has been specifically organized to allow for the presentation and debate of some of the latest and hottest technologies out there related to the use of Wire Bonding in semiconductor and microelectronic packaging.

- Cu/Low-K packaging processes
- Terminal pad structures and modifications
- Cu/Low-K packaging materials
- Assembly processes and handling issues
- Wirebonding and Bumping
- Novel packaging and design
- Failure Analysis and Reliability
- Electromigration and Interfacial Adhesion
- Testing and Probing Challenges
- Simulation and Modeling

Those wishing to present at the Wire Bonding Topical Workshop must submit a ~300 word abstract electronically **BEFORE MARCH 30, 2018,** using the on-line submittal form at: www.imaps.org/abstracts.htm. Full written papers are not required. All Speakers are required to pay a reduced registration fee and are required to attend the entire workshop to make the presentation in-person. Please contact Brian Schieman by email at bschieman@imaps.org if you have questions or need assistance submitting an abstract.

***Co-located with IMAPS 2018***

## Atotech Celebrates the Sale of its 888th Electrolytic Copper Plater

Berlin, December 20, 2017 – Atotech, a leading global provider of chemicals, equipment and services for the specialty plating industry, announced the sale of its 888th electrolytic copper plater which goes to Evertek Electronic (Kunshan) Co. Ltd., China. Manufactured in Feucht, Germany, the plater is currently on its way to China where it will be installed. The anniversary plater is a Uniplate® Cu 24 InPulse® 2 plating system. It operates on a UTS-s transportation system at a speed of 1.0 m/min to provide flash copper, BMV and through-hole filling for HDI mobile printed circuit boards which will be supplied to local Chinese smartphone OEMs.


*Installed in Feucht, Germany, the 888th plater is ready for shipment.*

Uniplate® is Atotech's leading horizontal mass production system for the pretreatment, metallization and electrolytic copper plating of demanding HDI PCB and IC substrates. A key advantage is the low chemistry and water consumption, as well as the reduced waste water results. Another highlight is the very high productivity and yield performance, which makes Atotech systems the production solution of choice. Uniplate® in the market is known as an energy and cost efficient system that can be applied to a wide range of board types at high throughput rates. In particular, Uniplate® Cu24 InPulse® 2, which is being delivered to Evertek Electronic (Kunshan) Co. Ltd., is equipped with unique rectifiers for pulse plate operation, ensuring that the highest rates of productivity, as well as the best throwing power performance and uniformity are achieved.

With the anniversary plater Atotech celebrates its long-standing relationship with Kingboard Chemical Holdings Ltd. and is very proud to deliver the first total production solution to Evertek Electronics Co. Ltd., a subsidiary of Kingboard Chemical Holdings Ltd. Over the past years, a total of 17 equipment lines – including 10 platers – were manufactured and delivered to the PCB companies of the Kingboard Group. "It is a great honor for us to deliver this anniversary plater to a company with whom we have such a good long-standing relationship. The figure "8" in Chinese stands for infinite luck and wealth, something we wish for our customers. So plater number 888 symbolizes very special fortune," states Chen Chen, System Manager Electronics Equipment at Atotech Asia Pacific Ltd.

Mr. Wang Shengwen, General Manager of Evertek Electronic Co. Ltd., added "Atotech's Uniplate® Cu24 InPulse®2 for BMV filling will contribute to our any-layer production process, help us improve our plating capability, and further strengthen our market position in the industry. We value this fruitful cooperation with Atotech, and look forward to an even deeper partnership in the future."

The sale of the 888th plater represents yet another highlight of Atotech's success story, which looks back on nearly 30 years of innovation, continual research and development, in addition to a well-established global sales and service network. The company prides itself on a successful history in equipment sales – and not only of electrolytic plating systems. To date, more than 1,600 Uniplate® and 230 Horizon® systems have been sold and installed, a success made possible by close partnerships and enduring positive relationships with customers.

The origins of the Uniplate® system can be traced back to 1988, when Atotech sold its first plater, a Uniplate® Cu3, in Germany. In 1991, sales were also made in Europe and Asia, and the 100th plater, a Uniplate® Cu18, was sold to Samsung in 1997. In 2006, only nine years later, Atotech sold its 400th plater – a Uniplate® Cu24 IP2 for BMV filling and panel plating – to Ibiden in China. The 500th plater was sold in 2008 to CCTC in Shantou, China; and three years later, the 600th plater was sold to AT&S in Shanghai, China. By the end of 2013, another 150 platers were sold, and the 750th plater, a Uniplate® Cu18 IP2 for superfilling, was delivered to Zhen Ding Technology Holding Limited (ZDT), part of the Foxconn Group. Since then, Atotech has sold an additional 133 platers and is proudly celebrating the sale of the 888th plater to Evertek Electronic Co. Ltd.!

Evertek Electronic Co. Ltd. is a subsidiary of Kingboard Chemical Holdings Limited, one of the world's major laminate producers and a leading printed circuit board manufacturer and chemical products supplier in China. Kingboard Chemical Holdings Ltd. is considered to be one of the leading Tech 100 companies (Bloomberg Businessweek, 2010). Evertek Electronic Co. Ltd. applies its technology to both single-layer and any-layer HDI boards, targeting products and services in the high-end segment such as mobile phones, tablet PCs, and network devices.

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**About Atotech**

Atotech is one of the world's leading manufacturers of specialty chemicals and equipment for the printed circuit board, IC-substrate and semiconductor industries, as well as for the decorative and functional surface finishing industries. Atotech has annual sales of USD1.1 billion. The company is fully committed to sustainability – we develop technologies to minimize waste and to reduce environmental impact. Atotech has its headquarters in Berlin, Germany, and employs more than 4,000 people in over 40 countries.

# INDUSTRY NEWS

## New Gore® Polyvent Ex+ Safety + Uncompromising Performance for Equipment in Explosive Atmospheres

Elkton, MD, November 29, 2017 – W. L. Gore & Associates announces the launch of GORE® PolyVent Ex+. The latest addition to Gore's Protective Vents Screw-In Series is certified according to explosion-proof safety standards, IECEx and ATEX. These certifications enable global integration of the product with fewer certification efforts, saving labor and testing costs. Further, the PolyVent Ex+ offers additional protection performance due to its unique design.


*Suitable for equipment used in potentially explosive environments, the new IECEx- and ATEX-approved GORE® PolyVent Ex+ offers reliable protection and venting performance to increase the lifetime of enclosures up to a 20 liter volume.*

GORE® PolyVent Ex+ has earned the IECEx and ATEX certification codes Ex II 2G Ex eb IIC Gb and Ex II 2D Ex tb IIIC Db. IECEx and ATEX directives describe general requirements for equipment, components and devices that are used in potentially explosive atmospheres. With this certification, PolyVent Ex+ is allowed in areas with potentially explosive atmospheres caused by combustible gases or dust as following:

- **Gas:** All non-mining, above-ground applications (equipment group 2) in Zones 1 and 2 with need for protection type "eb" (increased safety) for Equipment Category 2 Gb.
- **Dust:** All non-mining, above-ground applications (equipment group 2) in Zones 21 and 22 with need for protection type "tb" (standard protection by housing) for Equipment Category 2 Db.

Peter Kroker, Gore PolyVent Technical Project Manager, explains: "We developed this product to meet the needs of our customers who are working in industries that process, use or manufacture materials that may give rise to an explosive atmosphere. The new Ex-rated GORE® PolyVent Ex+ is the perfect fit for these tough environments."

Peter adds, "Ensuring that products and systems meet stringent IECEx and ATEX requirements is a complex, time consuming and costly process. Choosing GORE® PolyVent Ex+ can easily speed up time-to-market while reducing costs in the certification process."

GORE® PolyVent Ex+ offers additional features that truly deliver the uncompromising Gore performance required in these tough environments and add to the "safety aspect" for both operators and equipment.

### The Plus (+) means this product can do more

Due to its unique design, GORE® PolyVent Ex+ offers:

- **Uncompromising performance.** All materials selected for designing GORE® PolyVent Ex+ have been chosen as they support the vent's long-lasting exceptional behavior in the field. The vent body, cap and Gore's creative, patented membrane-sealing technology only use premium 1.4404 (316L) non-flammable, stainless steel.
  The latest GORE™ membrane, made of 100% ePTFE, delivers the remarkable performance for pressure-equalization customers expect, while achieving the highest flammability rating in its category (UL 94 VTM-0). Additionally, the silicone O-ring with the flammability resistance rating of UL 94 V-0 adds another layer of safety on which customers can depend.
  These high-quality materials combined with the GORE® PolyVent Ex+ innovative construction ensure comprehensive flammability resistance, excellent corrosion resistance and exceptional chemical robustness.

- **High "Ingress Protection to Airflow" ratio.** The GORE™ Membrane provides lasting oleophobic and hydrophobic protection. With an airflow rate of 1600 ml/min at 70 mbar and an ingress protection rating of IP68/IP69k, PolyVent Ex+ reliably protects enclosures up to 20l for a wide range of temperatures.

As Peter Kroker explains: "GORE® PolyVent Ex+ is made of materials of the highest quality. But most important, these vents deliver the exceptional venting performance and reliable protection our customers have come to rely on. This new product rounds out the already extensive Screw-In product portfolio by fulfilling the need for a venting application in potentially explosive environments."

For more information about the GORE® Protective Vents product portfolio, visit gore.com/protectivevents.

### About Gore™

W. L. Gore & Associates is a global materials science company dedicated to transforming industries and improving lives. Founded in 1958, Gore has built a reputation for solving complex technical challenges in the most demanding environments – from revolutionizing the outerwear industry with GORE-TEX® fabric to creating medical devices that improve and save lives to enabling new levels of performance in the aerospace, pharmaceutical and mobile electronics markets, among other industries. The company is also known for its strong, team-oriented culture and continued recognition from the Great Place to Work® Institute. Headquartered in Newark, Delaware,

continued on page 28

continued from page 27

Gore employs approximately 9,500 Associates and generates annual revenues that exceed $3 billion. www.gore.com

### About Gore Performance Solutions

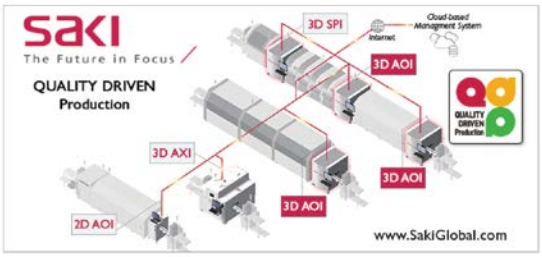
Gore Performance Solutions Division develops products and technologies that address complex product and process challenges in a variety of markets and industries, including aerospace, automotive, pharmaceutical, mobile electronics, oil and gas – and more. Through close collaboration with industry leaders across the globe, Gore enables customers to design their products and processes to be safer, cleaner, more productive, reliable, durable and efficient across a wide range of demanding environments.



## Saki Joins the ASYS PULSE Community for PCB Assembly Line Productivity

***Connects inspection and measurement systems to PULSE open architecture***

Fremont, CA, November 30, 2017 – Saki Corporation, an innovator in the field of automated optical and x-ray inspection systems, announces that it has joined the ASYS PULSE Community to network its automated inspection and measurement systems with electronic production equipment from other PULSE member companies.




ASYS (Dornstadt, Germany) created the PULSE Community to bring together system manufacturers in the electronics sector with products that are "PULSE-capable." These systems have custom connections that connect to the PULSE open interface.

"Our aim is to give customers a solution for the entire production line, and we're following that up across the board," said Erwin Beck, senior vice president product management and marketing at ASYS. "In our eyes, it means we will be able to respond appropriately to our customers' requirements in the future in an open way that is not manufacturer-dependent."

Herbert Natterer, product manager of the ASYS Industrie 4.0 solution, commented, "It's great that we can include Saki's inspection systems within the PULSE line so operators can monitor and control the operation of these systems through the PULSE network. We are looking forward to the collaboration and professional exchange. Thanks to the membership of Saki, we have approached our goal to establish one solution for the whole production operation."

"Joining the PULSE Community expands Saki's opportunity to maximize production-line productivity. PULSE provides a very practical, convenient, and visual way to monitor the assembly process. It complements the quality assurance and process controls built into our inspection and measurement systems. We are excited to be part of the PULSE Community," said Jarda Neuhauser, deputy general manager at Saki.

### About ASYS Group

The ASYS Group is a global technology company and a leading manufacturer of handling, process and special machines for the electronics, solar and life science industries. The corporate headquarters in Dornstadt near Ulm, Germany controls the activities of the subsidiaries in more than 40 countries. The ASYS Group employs over 1000 staff worldwide and supplies both standard products and customized solutions.

### About Saki

Since its inception in 1994, Saki has led the way in the development of automated recognition through robotic vision technology. Saki's 3D automated solder paste, optical, and x-ray inspection systems (SPI, AOI, AXI) have been recognized to provide the stable platform and advanced data capture mechanisms necessary for true M2M communication, improving production, process efficiency, and product quality. Saki Corporation has headquarters in Tokyo, Japan with offices, sales, and support centers around the world.

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## TechSearch International Analyzes New Automotive Packaging Trends

More than 80 companies are developing autonomous vehicles and many more are involved in providing sensors and computational systems for advanced driver assistance systems (ADAS). System design, package choices, materials, and process integration are critical to the successful implementation of new safety features that are part of ADAS and will ultimately be a part of autonomous driving. ADAS requires the use of cameras, light detection and ranging (LIDAR), radar, and other sensors, as well as communication systems and fast processing capability. The potential use of artificial intelligence or machine learning to provide the analytics enabling safety features is driving the adoption of advanced packaging and heterogeneous integration. Different combinations of sensors will be used in each vehicle and the particular combinations will be determined by each carmaker.

# Your IMAPS Member Benefits at Your Chapter Level

**Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar**

## Central Texas

The Central Texas Chapter of IMAPS, in conjunction with SMTA, had a very successful Expo with four technical presentations and about 40 vendors on October 10, 2017.

Our next meeting is being planned at National Instruments for Tuesday, February 13, 2018 with four technical presentations expected.



**Industry News...continued**

TechSearch International's *New Frontiers in Automotive Electronics Packaging* examines the packaging choices for these sensors. The report answers key questions: What type of semiconductor packages are used for image sensors, radar, ultrasonic, and LIDAR? Where are fan-out wafer level packages and flip chip interconnects being adopted? How do package reliability requirements differ from other applications? What are future challenges for new package adoption? The report also examines trends in interconnect technology such as the adoption of copper wire bonding and copper clip. Packaging trends in the powertrain for electric and hybrid vehicles are also analyzed. Automotive specific offerings from OSATs and IC package substrate makers are described.

The report's five-year market forecast focuses on new packages introduced as a result of ADAS adoption. Projections for the use of image sensors are presented. Unit volumes for radar modules with FO-WLP are provided. A market forecast for processors used in sensor fusion is included. Package types used in electric powertrains and a five-year forecast in unit volumes are provided.

The 110-page report provides full references and an accompanying set of 94 PowerPoint slides.

TechSearch International, Inc., founded in 1987, is a market research leader specializing in technology trends in microelectronics packaging and assembly. Multi- and single-client services are offered. TechSearch International professionals have an extensive network of more than 18,000 contacts in North America, Asia, and Europe.

For more information, contact Jan Vardaman, TechSearch at tel: 512-372-8887 or visit www.techsearchinc.com. Follow us on twitter @Jan_TechSearch.

IMAPS/ACerS 14th International Conference and Exhibition on

# *Ceramic Interconnect and Ceramic Microsystems Technologies* (CICMT 2018)

**18-20 April 2018**
University of Aveiro
Aveiro, PORTUGAL

**General Chair:**
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University of Aveiro
paula.vilarinho@ua.pt

**General Co-Chair:**
Robert Pullar
University of Aveiro
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**Technical Chair:**
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sxdai@sandia.gov

**Technical Co-Chair:**
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yxli@mail.sic.ac.cn

**Goal**
The Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT) conference brings together a diverse set of disciplines to share experiences and promote opportunities to accelerate research, development and the application of ceramic interconnect and ceramic microsystems technologies. This international conference features ceramic technology for both microsystems and interconnect applications in a dual-track technical program. The Ceramic Interconnect track focuses on cost effective and reliable high performance ceramic interconnect products for hostile thermal and chemical environments in the automotive, aerospace, lighting, solar, defense/security, and communications industries. The Ceramic Microsystems track focuses on emerging applications and new products that exploit the ability of 3-D ceramic structures to integrate interconnect/packaging with microfluidic, optical, micro-reactor and sensing functions. Tape casting, thick film hybrid, direct write and rapid prototyping technologies are common to both tracks, with emphasis on materials, processes, prototype development, advanced design and application opportunities.

**Ceramic Interconnect Track**
Conventional thick and thin film ceramic technologies are being revolutionized and extended through the development of low temperature co-fired ceramics, photo patterning, and embedded passive component materials and processes. These have contributed to increased circuit density, enhanced functionality, and improved performance that are being adopted for leading edge applications in wireless and optical communications, automotive, MEMS, sensors, and energy. Data communications and the Internet are driving the demand for bandwidth, sparking demand for optical communication equipment and new interconnect and packaging applications that perform at 40 Gb/sec and beyond. In under-the-hood electronics for automotive, engine/transmission control, communications, and safety applications continue to drive the growth of ceramic interconnect technology, while collision avoidance systems are creating interest in low loss ceramic materials for frequencies approaching 100 GHz.

**Ceramic Microsystems Track**
Enabled by the availability of commercial ceramic, metal and embedded passives materials systems, and the rapid prototyping capabilities of the well established multilayer ceramic interconnect technology, three dimensional (3-D) functional ceramic structures are spawning new microsystems applications in MEMS, sensors, microfluidics, bio-devices, microreactors, and metamaterials. These new devices and applications exploit the ability to integrate complex 3D features and active components (e.g., valves, pumps, switches, light pipes, and reaction chambers).

In addition, the Ceramic Microsystems track of the CICMT conference targets new developments in microsystems that include fabricating 3-D micro device structures enhanced with sol-gel, advanced printing and patterning technologies, high temperature materials technologies, and emerging applications like energy harvesting. Many of these innovative applications are taking advantage of the unique ability to integrate the thermal, chemical, mechanical and electrical properties of these multicomponent ceramic-metal systems.

**Special Features**
- Invited keynote and international presentations on the current status ceramic technology and future system directions.
- A focused exhibition for suppliers who support the use of the technologies.
- A technical poster session to promote student participation.
- Social events to promote new contacts.

IMAPS/ACerS 14th International Conference and Exhibition on

## *Ceramic Interconnect and Ceramic Microsystems Technologies* (CICMT 2018)

**Planned Session and Paper Topics Include:**

| Ceramic Microsystems | Ceramic Interconnect |
|---|---|
| **Markets and Applications**<br>• MEMS Technology and Markets<br>• Batteries and Fuel Cells<br>• Biological and Medical<br>• Chemical and Biochemical<br>• Photonics<br>**Materials and Properties**<br>• Materials Integration and Nano-materials<br>• Thermal Management and Reliability<br>• Piezoelectric Materials<br>• Optoelectronics<br>**Processing and Manufacturing**<br>• MEMS Manufacturing Technology<br>• Industrial Automation and Rapid Prototyping<br>• Nano-technology/Integration<br>• High Temperature Microsystems<br>**Devices**<br>• Sensors and Actuators<br>• Micro-reactors<br>• Fluidic Devices<br>• Biomolecular and Cell Transport Systems<br>• Energy Conversion Systems<br>**Characterization and Reliability**<br>• Materials and Process Characterization<br>• Systems Reliability, Lifetime, and Failure Estimation<br>• Reliability of High-Performance Microsystems<br>**Design, Modeling, and Simulation**<br>• Thermal and Heat Transfer<br>• Computational Fluid Dynamics | **Markets and Applications**<br>• Automotive<br>• Aerospace<br>• Lighting/Solar<br>• Wireless/Communication<br>• Medical Electronics<br>**Materials and Properties/Functions**<br>• Dielectric and Magnetic Materials<br>• Embedded and Integrated Passives<br>• Microwave/mm Wave Characterization<br>• Zero-shrink Ceramic Systems<br>**Processing and Manufacturing**<br>• LTCC and Multilayer Ceramics<br>• Roll to Roll and Continuous Manufacturing<br>• Direct WRite and Drop on Demand<br>• Advanced Thick Film Processing<br>• Fine Structuring Technologies<br>**Devices**<br>• Circuits, Antennas, and Filters<br>• Embedded Structures and Components<br>• Optical Devices and Optoelectronics<br>**Characterization and Reliability**<br>• Characterization of Green Tapes<br>• Life Testing, Quality Issues<br>• RF Performance<br>**Design, Modeling, and Simulation**<br>• High Frequency Design Software<br>• Design Rules |

| Integrated Ceramic Technology |
|---|
| **Advanced Packaging Technology**<br>• Next Generation Packaging Technologies<br>• Packaging and Integration in BioMEMS<br>• Packaging Issues for MEMS Devices<br>• Technologies for Microsystems Components and Substrates<br>• Packaging Standard for Microsystems<br>• Environmental Issues, Lead Free Systems<br>• Cost Reduction |

For more information visit

**www.imaps.org/ceramics**

# iMAPS New England – 45th Symposium & Expo

**The Largest Regional Symposium Dedicated to**

**Microelectronics, Assembly and Packaging**

**Boxboro Regency Hotel & Conference Center**

**Boxborough, Massachusetts**

## May 1, 2018

**EarlyBird Exhibitor Registration is Open!!**

**The Technical Program is Being Assembled**

**Visit www.imapsne.org**

The New England Chapter

## Planned Papers & Posters

- 2D-3D & Beyond
- Medical Device Packaging
- RF & Microwave Innovative Technologies
- Wire & Die Bonding, Flip Chip, Bumping, TSV
- SMT & Electronics Assembly-Packaging
- Thermal Management Materials & Designs
- Military, Defense & Space Microelectronics
- High Temperature Electronics
- MEMS Sensors & Nano Technology
- Wearables - Consumer Applications
- Advanced Semiconductor Packaging
- Printed Electronics - Additive Manufacturing
- Nanoelectronic - Optoelectronic Packaging
- New & Emerging Materials-Technologies


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**www.imapsne.org**

# Announcement and Call for Abstracts

## International Conference and Exhibition on

# High Temperature Electronics (HiTEC)

**www.imaps.org/hitec**

## May 8-10, 2018

Hotel Albuquerque
Albuquerque, New Mexico USA

**Overview:** HiTEC 2018 continues the tradition of providing the leading biennial conference dedicated to the advancement and dissemination of knowledge of the high temperature electronics industry. Under the organizational sponsorship of the International Microelectronics Assembly and Packaging Society, HiTEC 2018 will be the forum for presenting leading high temperature electronics research results and application requirements. It will also be an opportunity to network with colleagues from around the world working to advance high temperature electronics.

***Abstracts being requested include the following topics:***

- **Applications:**
  - Geothermal
  - Oil well logging
  - Automotive
  - Military/aerospace
  - Space
- **Device Technologies:**
  - Si, SOI
  - SiC
  - Diamond
  - GaN
  - GaAs
  - Contacts
  - Dielectrics
- **MEMS and Sensors:**
  - Vibration
  - Pressure
  - Seismic
- **Packaging:**
  - Materials
  - Processing
  - Solders/Brazes
  - PC Boards
  - Wire Bonding
  - Flip Chip
  - Insulation
  - Thermal management
- **Circuits:**
  - Analog
  - Digital
  - Power
  - Wireless
  - Optical
- **Energy Sources:**
  - Batteries
  - Nuclear
  - Fuel Cells
- **Passives:**
  - Resistors
  - Inductors
  - Capacitors
  - Oscillators
  - Connectors
- **Reliability:**
  - Failure mechanisms
  - Experimental and modeling results

**Student Competition sponsored by the Microelectronics Foundation:**

The Microelectronics Foundation sponsors ***Student Paper Competitions*** in conjunction with all Advanced Technology Workshops (ATWs) and Conferences. Students submitting their work and identifying that "Yes, I'm a full-time student" on the abstract submission form, will automatically be considered for these competitions. The review committee will evaluate all student papers/posters and award a total of $1,000 in award checks at the ATW/Conference. The selected student(s) must attend the event to present his or her work and receive the award. For more information on the student competition, go to www.microelectronicsfoundation.org.

# IMAPSource

## Microelectronics Research Portal

**IMAPSource transitioned to membership level plans for free downloads on April 1, 2016. The number of free annual downloads included in your membership corresponds to your member type.**

**Non-members can enjoy articles and proceedings from IMAPSource for $20 per download.**

IMAPS members are pre-registered with IMAPSource and receive a profile confirmation email from Allen Press. This will help members gain unlimited download access to IMAPSource. Non-members and guests will need to click Register Now at IMAPSource.org.

In 2018, free downloads will be subject to membership level below. Non-member downloads will be subject to a per-article charge.

| 2018 IMAPSource Membership Plans: | Number of downloads |
|---|---|
| Individual/Senior/Lifetime | 100 |
| Corporate | 300 |
| Premier Corporate/Academic Institutions | Unlimited* |
| Associate Corporate | 50 |
| Affiliate (International Chapters/Unemployed Members) | 50 |
| Student | 25 |
| Retired/Senior Retired/Corporate International | 25 |

**Unlimited package allows multiple IP range and unlimited access*

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International Microelectronics Assembly and Packaging Society

www.IMAPS.org

## CORPORATE MEMBERSHIPS

***Join now!***

IMAPS corporate memberships are designed to give your company a competitive advantage in the microelectronics packaging industry. Choose the right membership to meet your exhibition, advertising, discount registration needs and more.

| **Membership package inclusions** | Premier<br>*For organizations with more individual members or those seeking more marketing exposure* | Standard<br>*Our most popular corporate membership package* |
|---|---|---|
| Number of employees who receive individual membership benefits | No limit to number of individual members with full online access; up to 5 receive print magazine | 2 |
| Access to IMAPSource microelectronics research portal | IP recognition allowing unlimited access for all computers in one network | 150 downloads via two (2) selected member logins |
| Press releases in Corporate Bulletin | Up to 1 press release per bulletin (twice monthly) | Up to 1 press release per bulletin (twice monthly) |
| Member pricing for exhibitor events | Included | Included |
| JOBS Marketplace | Complimentary job postings | Complimentary job postings |
| Use of membership mailing list | 3x per year | 1x per year |
| IMAPS.org advertising | Complimentary | Member discount |
| Magazine advertising | One 1/4 page ad incl. annually, plus 15% discount on any additional ad | 15% discount |
| Online Industry Guide | Includes company listing, link to website, product and service categories | Includes company listing, link to website, product and service categories |
| Global Business Council | Membership included | Membership included |
| Webinar Sponsorship | 30% discount | 30% discount |
| Annual dues | $2,500 | $750 |

*Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!*

# Premier Corporate Members

IMAPS has introduced a new level of support for corporate members. These companies have decided to participate in our Society at the Premier Corporate Member level. We are extremely grateful for their dedication to the furtherance of our educational opportunities and technological goals.

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Sekisui Chemical Co., Ltd.
Unitron

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Sara Abbasi
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Nadeem Bhatti
Linkan Bian
Ghislain Bilodeau
Ankit Bisht
Paui Blais
Janice Booth
Christina Bottom
Robert Botts
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Tyler Bowman
Eric Bridot
Julia Brueckner
Jungsoo Byun
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Srinivasan Chakrapani
Basab Chatterjee
Timothy Chen
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| Indium | Rick Short | 315-381-7554 | rshort@indium.com | www.indium.com | 5 |
| Mini-Systems, Inc. | Craig Tourgee | 508-695-0203 | ctourgee@mini-systemsinc.com | www.mini-systemsinc.com | back cover |

## *Advancing Microelectronics* 2018 Editorial Schedule

| Issue | Theme | Copy Deadline | Ad Commitment I/Os Deadline |
|---|---|---|---|
| Mar/Apr | RF/Microwave, High-Frequency, High-Reliability | Jan. 8 | Jan. 15 |
| May/Jun | Heterogeneous Integration – System in Package (SiP) | Mar. 8 | Mar. 13 |
| Jul/Aug | IMAPS 2018 (Pasadena) Show Issue | May 8 | May 14 |
| Sep/Oct | Advanced Materials and Additive Manufacturing | Jul. 6 | July 13 |
| Nov/Dec | Chip Package Integration (CPI) | Sep. 7 | Sep. 13 |

# IMAPS HEADQUARTERS

## WHO TO CALL

**Michael O'Donoghue, Executive Director,** (919) 293-5300, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction

**Brian Schieman, Director of Programs,** (412) 368-1621, bschieman@imaps.org, Development of Society Programs, Website Development, Information Technology, Exhibits, Publications, Sponsorship, Volunteers/Committees

**Ann Bell, Managing Editor,** *Advancing Microelectronics,* (703) 860-5770, abell@imaps.org, Coordination, Editing, and Placement Management of all pieces of bi-monthly publication, Advertising and Public Relations

**Brianne Lamm, Marketing and Events Manager,** (980) 299-9873, blamm@imaps.org, Corporate Membership, Membership and Event Marketing, Society Newsletters/Emails, Event Management, Meeting Logistics and Arrangements, Hotel and Vendor Management

**Shelby Moirano, Membership Administration,** (919) 293-5000, smoirano@imaps.org, Member Relations and Services, Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support

# CALENDAR OF EVENTS

## 2018

| | start | end | |
|---|---|---|---|
| **JANUARY** | 1-23-18 | 1-24-18 | ATW on Advanced Packaging for Medical Microelectronics<br>San Diego, CA<br>www.imaps.org/medical |
| **MARCH** | 3-5-18 | 3-8-18 | International Conference and Exhibition on Device Packaging 2018<br>We-Ko-Pa Resort and Casino, Fountain Hills, Arizona<br>www.imaps.org/DevicePackaging |
| **APRIL** | 4-18-18 | 4-20-18 | CICMT 2018 (PORTUGAL)<br>University of Aveiro Aveiro, Portugal<br>www.imaps.org/ceramics |
| **MAY** | 5-1-18 | 5-1-18 | IMAPS New England - 45th Symposium & Expo<br>Boxborough, MA<br>www.imapsne.org |
| | 5-8-18 | 5-10-18 | HiTEC 2018 - High Temperature Electronics<br>Albuquerque, New Mexico<br>www.imaps.org/hitec |
| **OCTOBER** | 10-8-18 | 10-8-18 | Topical Workshop & Tabletop Exhibition on Wire Bonding<br>Pasadena, CA<br>www.imaps.org/wirebonding |
| | 10-8-18 | 10-11-18 | IMAPS 2018 - Pasadena<br>Pasadena, CA<br>www.imaps.org/imaps2018 |

## Visit www.imaps.org

**for links to all upcoming events including:**

- **full event descriptions**
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