DPC, Wafer-Level Packaging

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Wafer level packaging has been a popular choice for mobile devices as packaging is becoming smaller and more lightweight. The components have higher IO counts and are expected to be higher in performance. The smaller devices are becoming more demanding in many regards. Some of these demands are design, flexibility, fine pitch, thinner packages, and cost. With these demands come many challenges along every step of the process. The articles in this issue of Advancing Microelectronics are focused on the different complexities that occur in device and wafer level packaging from the plating process to the bonding process.

Packaging technology in the past such as flip-chip using C4 has been used over the last several years with success and reliability but cannot meet current technology requirements. A new trend to meet these requirements is using Cu pillars with Pb-free solder caps. This technology helps meet the fine pitch and stand-off height requirements along with others. To create these Cu pillars, a plating process is used. With this process are several complexities that need to be overcome such as pillar height uniformity, pillar shape control, purity of the Cu deposit, and maintenance of high plating speeds. These complexities are addressed in this issue’s first article entitled “High Quality Cu Deposits from Cu Electroplating Baths.”

Another packaging technology being used is eWLB (embedded Wafer Level Ball Grid Array) which is an interconnect system processed directly on the wafer. This technology allows for the highest density in 2D and is currently being advanced into 3D stacking, but there are several challenges when using this technology. One challenge in particular is the availability of routing and interconnecting high I/O fine pitch array. In the article “Ultra Fine Pitch RDL Development in Multi-Layer eWLB (embedded Wafer Level BGA) Packages,” this challenge, as well as the general advantages of eWLB, are discussed.

In flip-chip packages there is a continued trend of finer pitch. This trend typically creates a challenge of solder bridging. With conventional solder bumps on flip-chips and standard assembly solder bridging can occur. Changing the Cu pillars instead of solder bumps helps with some of the challenge. By changing the way they are assembled can also help. The article “Process Advantages of Thermocompression Bonding” discusses using a thermocompression bonding process to help overcome this challenge.

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From One Engineer To Another®
High Quality Cu Deposits from Cu Electroplating Baths

Matthew Thorseth, Mark Scalisi, Jonathan Prange, Inho Lee, Yil-Hak Lee, Jong-Hun An, Su-Han Woo, Yoon Joo Kim, Mark Lefebvre, Jeff Calvert

Advanced Packaging Technologies, Dow Electronic Materials, 455 Forest Street, Marlborough, MA 01752

As the microelectronics industry continues to advance and mature, the need for increases in device complexity while maintaining high reliability and pushing to small form factors necessitates new solutions for advanced packaging of semiconductor devices. Flip chip packages using controlled collapse chip connection (C4) with solder bumps have been used since the 1960s with great success and reliability[1], but cannot meet the requirements of new devices, such as fine pitch I/O connections, maintaining stand-off heights, thermal management, and low connection resistivity[2]. One leading technical strategy that is starting to gain market traction is the utilization of electroplated Cu pillars capped with electroplated Pb-free solders. Cu pillars with Pb-free solder caps have several technical advantages over Pb-free solders alone, including lower resistivity ($1.68 \times 10^{-8} \Omega \cdot m$ vs. $1.09 \times 10^{-7} \Omega \cdot m$), higher thermal conductivity (385 vs. 34.7 W m$^{-1}$ K$^{-1}$), and demonstrated ability to achieve I/O pitches of 6 μm (vs. ~50 μm for lead-free C4 bumps)[3].

Cu pillars are typically fabricated through the process of electroplating Cu into patterned photoresists that are coated on top of a Cu seed layer. The typical Cu electroplating bath consists of inorganic components (CuSO$_4$, H$_2$SO$_4$, and HCl) and organic components, usually an accelerator/brightener, suppressor/carrier, and a leveler. Inorganic components are needed as a source of Cu and to provide bath conductivity. Organic components are critical to the bath function as they provide a smooth, bright deposit with high uniformity.

The electroplating process for Cu pillars does present a number of challenges, including (1) pillar height uniformity within a die (WID) and across a patterned wafer (WIW), (2) pillar shape control, (3) purity of the Cu deposit, and (4) maintaining high plating speeds. Achieving low pillar height non-uniformity is critical to enabling finer pitch interconnects while minimizing warpage of the package. The height non-uniformity (% within-die non-uniformity, %WID) is measured by:

$$\text{%WID} = \frac{1}{2} \frac{\text{Height}_{\text{range}}}{\text{Height}_{\text{average}}}$$  \hspace{1cm} (1)

Another challenge for Cu pillar plating is maintaining a flat to slightly recessed profile on the top of the Cu pillar. When a solder-capped Cu pillar with a highly domed profile is subjected to solder reflow conditions, there is a higher chance of solder collapse off the pillar. Furthermore, in order to achieve high reliability of the Cu pillar-solder stack, a high purity Cu deposit is necessary to eliminate voiding at the intermetallic interface after solder reflow. Increased deposition speeds for Cu plating are needed to increase wafer through-put, making the aforementioned plating challenges even more difficult to overcome.

With these challenges in mind, Dow’s new Cu pillar plating product, INTERVIA™ 9000 Electroplating Copper Chemistry, was evaluated against a previous generation product, INTERVIA™ Cu 8540 Electroplating Copper Chemistry, across a wide variety of plating substrates, including Cu pillars with 20 μm and 50 μm feature sizes as well as RDL pads and traces[5, 6]. The products were tested in a variety of 300 mm plating tools and at various deposition rates. Performance toward within die and within wafer uniformity as well as deposit shape control was compared.

Figure 1. 20 μm diameter Cu pillars plated at 9 ASD (2.0 μm min$^{-1}$) with INTERVIA™ 8540 (a) and 9000 (b) baths.
Similar results have been observed with plating 50 μm diameter pillars with both products. INTERVIA™ 8540 deposits typically have a domed profile, while INTERVIA™ 9000 deposits can be tuned from a dished shape to a flat or domed shape by adjusting the Leveler concentration in the plating bath. INTERVIA™ 9000 baths also support higher deposition rates than INTERVIA™ 8540 baths, with the former able to achieve deposition rates of at least 20 ASD (4.4 μm min⁻¹) on 50 μm pillars, while the latter can plate up to 15 ASD (3.3 μm min⁻¹). As the plating rates increase, similar increases in %WID are observed with both products, with INTERVIA™ 8540 Cu pillar deposits exhibiting similar %WID than INTERVIA™ 9000 deposits.

Both INTERVIA™ 8540 and 9000 plating baths show versatility across many Cu deposition applications beyond Cu pillars, including redistribution layer (RDL) wiring. Plating of RDL lines and traces at 4.5 ASD (1 μm min⁻¹) with INTERVIA™ 8540 and INTERVIA™ 9000 chemistries result in similar %WID performances for both chemical packages. As shown in Figure 4, both products deposit Cu with smooth morphology and a bright finish. INTERVIA™ 9000 baths can be used to deposit Cu onto a variety of line/space features, from 20/20 μm down to 5/5 μm being demonstrated in Figure 5.

Figure 4. RDL traces plated with INTERVIA™ Cu 8540 (a) and 9000 (b) baths plated at 4.5 ASD (1.0 μm min⁻¹).

The Cu pillars were then evaluated for the reliability of the Cu-Sn interface when either SOLDERON BP TS 6000 Tin-Silver Plating Chemistry or SOLDERON BP SN 2000 Pure Tin Plating Bath solder was plated directly onto the Cu deposits obtained from both INTERVIA™ 8540 and 9000 baths. The voiding at the interface between Cu and solder was examined by focused ion-beam scanning electron microscopy (FIB-SEM) cross-sections of the deposits after solder reflow. The reflow conditions used reached a maximum temperature of 260°C to melt the solder, after which the deposits were cooled to RT. This reflow process was repeated ten times before the FIB-SEM images were collected. Cu pillars deposited from both INTERVIA™ Cu 8540 and 9000 baths were found to have void-free integration performance, as shown in Figure 6. This result is consistent with the expectation that low concentration of impurities in a deposit will result in high quality Cu-Sn interfaces. The interface between Cu and Sn has two different phases, the Cu₃Sn intermetallic directly on the Cu interface, and the Cu₆Sn₅ intermetallic closer to the Sn phase. The amounts of the intermetallic phases appear to be near the same volume for both INTERVIA™ 8540 and INTERVIA™ 9000 deposits.

Figure 5. RDL plated with an INTERVIA™ Cu 9000 bath plated at 7 ASD (1.5 μm min⁻¹) with a 5/5 μm (a) and 20/20 μm (b) line/space comb.

Figure 6. 20 μm diameter Cu pillars plated with INTERVIA™ Cu 8540 (a) and 9000 (b) baths capped with SOLDERON™ BP TS 6000 SnAg solder deposits after 10 times solder reflow.
INTERVIA™ 9000 Cu deposits exhibit void-free interfaces over a long bath age. As shown by Figure 7, void-free Cu-Sn interfaces can be achieved with INTERVIA™ 9000 deposits to at least 100 A hr L⁻¹ of bath age. Over the course of the aging experiment, the Cu deposits exhibited a very flat profile that did not change with the age of the bath, and the interface with SnAg solder deposited from SOLDERON BP TS 6000 Tin-Silver Plating Chemistry remained uniform without voiding in the deposits. The Cu pillar height uniformity did not significantly change (<1% standard %WID variation) over the age of the bath. Replenishment of the bath additives was performed after analysis of the concentrations with standard analysis techniques.

Comparison of INTERVIA™ Cu 8540 Electroplating Copper Chemistry and INTERVIA™ 9000 Electroplating Copper Chemistry deposits show many similarities. Both products produce highly uniform deposits of high purity Cu that enable void-free interfaces with Pb-free solder. INTERVIA™ 9000 baths, however, are able to plate at a higher deposition rate with a tunable shape when compared to INTERVIA™ 8540 baths. Bath lifetimes observed with INTERVIA™ 9000 baths are up to 100 A hr L⁻¹, while maintaining stable performance. All of the desirable characteristics of INTERVIA™ Cu 8540 deposits have been carried over to INTERVIA™ 9000 baths, while significantly improving the deposit profile, deposition speed, and bath stability.

References

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<td>Notification of Abstract acceptance</td>
<td>February 28, 2017</td>
</tr>
<tr>
<td>Paper submission deadline</td>
<td>March 31, 2017</td>
</tr>
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<td>Notification of Paper acceptance/revision/rejection</td>
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<td>Author registration deadline</td>
<td>May 10, 2017</td>
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Ultra Fine Pitch RDL Development in Multi-layer eWLB (embedded Wafer Level BGA) Packages

Won Kyoung Choi, Duk Ju Na, Kyaw Oo Aung, Andy Yong, Urmi Ray,* Riko Radojcic,* Bernard Adams** and Seung Wook Yoon***
STATS ChipPAC Pte. Ltd., 5 Yishun Street 23, Singapore 768442
*Qualcomm Technologies, Inc., San Diego, CA 92121
**STATS ChipPAC Inc., 10185 McKellar Court, San Diego, CA 92121 USA
***STATS ChipPAC Pte. Ltd., 10 Ang Mo Kio Street 65 Techpoint #04-08/09, Singapore 569059
seungwook.yoon@statschipapac.com

1. Introduction [1]
As a small, lightweight, high performance semiconductor package, wafer level chip scale packaging (WLCSP) has been a popular solution for space-constrained mobile devices and is a compelling solution for new Internet of Things (IoT) and wearable electronics (WE) applications. WLCSP was introduced in the late 1990s as a semiconductor package wherein all manufacturing operations are performed in wafer form with dielectrics, thin film metals and solder bumps applied directly on the surface of the die with no additional packaging [2]. The WLCSP provides the smallest possible package size since the final package is no larger than the die itself. The volume of WLCSP packages used in the industry has experienced steady growth since its introduction—driven by the small form factor and high performance requirements of mobile consumer products [3].

For emerging applications requiring significantly higher performance and bandwidth, a transition from fan-in WLCSP to fan-out wafer level packaging (FOWLP) is required to achieve maximum connection density, improved electrical and thermal performance and small package dimensions. FOWLP, also known as embedded Wafer Level Ball Grid Array (eWLB), is an interconnection system processed directly on the wafer and is compatible with motherboard technology pitch requirements. eWLB technology addresses a wide range of factors for mobile, IoT and WE applications. At one end of the spectrum is the need for a significant increase in input/output (I/O) density, a particular challenge as packages become progressively smaller and thinner. eWLB technology delivers fine line width and spacing as well as superior electrical performance, providing more design flexibility and a more significant reduction in size than is possible with printed circuit board (PCB) substrate technology. Along with this there is the need to integrate different active and passive elements, embedded very close to each other as a system-in-package (SiP). The complex thermal issues related to power consumption and the device’s electrical performance (including electrical parasitic and operating frequency) are successfully addressed by eWLB technology [3]. On the other side of the spectrum is the need to reduce assembly and test costs to meet consumer market requirements. The manufacturing process for eWLB is well established and lends itself to the use of large wafer and panel sizes, which has a direct impact on capital intensity and cost.

Figure 1. eWLB FOWLP Roadmap: Further 2.5D and 3D Integration [4].
At present, high volume ICs are primarily baseband, RF transceiver, power management integrated circuits (PMIC), NAND memory controller, connectivity, and security devices. Accelerated near-term customer adoption is taking place in logic processors, RF, audio and connectivity devices, automotive devices, and MEMS/sensor devices. eWLB solutions are now in high volume production on 28 nm silicon (Si) node and starting to ramp 16/14 nm devices. In a number of cases, eWLB achieved a 20~40% reduction in package size as compared to other packaging solutions and over 50% volume reduction due to its small and smaller form factor. For RF and high frequency devices, eWLB showed less parasitic electrical performance, therefore, it also significantly improved overall device performance. In one example, a 77 GHz Advanced Driver Assistance System (ADAS) packaged as an eWLB achieved excellent high frequency electrical performance due to small contact dimensions and short signal pathways which decreased parasitic effects. Increased power efficiency was found in eWLB solutions for PMIC devices compared to other package solutions.

II. Fine Line Width and Spacing with 3-Layer RDL Structure in eWLB

In situations where a device may have an interconnect pad arrangement or wafer level component, an additional layer of lateral connections may be employed to rearrange the connections in a manner suitable for wafer level processing. This additional layer is known as a redistribution layer or RDL and is fabricated from a thin layer of metal with dielectrics in between. RDL is for higher electrical performance and complex routing to meet electrical requirements.

In FOWLP/WLCSP designs, the I/O pads are often placed in an uneven distribution; therefore, a redistribution layer (RDL) is required to connect these pads to the ball. From package to board, a similar redistribution is also needed for the signal array to escape outward to other devices. A test vehicle was designed per the technical specifications shown in Table 1. It has 3-layer RDL structure with 2/2, 5/5, 10/10um line width/spacing (LW/LS) in a multi-die eWLB structure. Figure 2 shows the schematics of 3-layer RDL test vehicle cross-section and design. The 3-layer RDL was prepared with current high volume manufacturing (HVM) equipment used in a FlexLine™ process [4].

<table>
<thead>
<tr>
<th>Die Size</th>
<th>Die 1: 11.0 x 6.0 mm</th>
<th>Die 2: 11.0 x 6.0 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>PKG Size</td>
<td>15x15mm</td>
<td></td>
</tr>
<tr>
<td>Ball Pitch</td>
<td>400um</td>
<td></td>
</tr>
<tr>
<td>Die Thickness</td>
<td>200um</td>
<td></td>
</tr>
<tr>
<td>Package ball height/size</td>
<td>185um</td>
<td></td>
</tr>
<tr>
<td>PKG Thickness</td>
<td>400um</td>
<td></td>
</tr>
</tbody>
</table>

A. 2/2um and 5/5um Line Width and Line Spacing (LW/LS) RDL

One of the greatest challenges facing wafer level packaging at present is the availability of routing and interconnecting high I/O fine pitch area array. RDL allows signal and supply I/Os to be redistributed to a footprint larger than the chip footprint in eWLB. Required line widths and spacing of 2/2 μm for eWLB applications support the bump pitch of less than 40um. Finer line width and spacing are critical for further design flexibility as well as electrical performance improvement. For die-to-die interconnects of high I/O or multi channels, finer lines are critical for multi-die design and routing flexibility.

Figure 3 shows 5/5um and 2/2um LW/LS RDL, respectively. The micrographs show a uniform and well-defined micro structure. The Cu RDL thickness and CD are also well controlled, even with mixed design of finer and coarse LW/LS. With this process development, it is verified of robust process of fine RDL fabrication using current HVM equipment and process flow.

B. 3-layer RDL with fine LW/LS

Side-by-side multi-chip packaging can provide more design flexibility for System-in-Package (SiP) applications because a chip designer has more freedom in pad location as well as circuit block allocation. eWLB technology utilizes very fine pitch metal line width and space as well as multi-layer RDL process which provides better technical solutions for multi-chip packaging. eWLB uses fine pitch metallization and well controlled interconnection with wafer fab lithography process thus it has great advantage to provide better electrical performance compared to conventional flipchip technology. Figure 4 shows the cross-section of 3-layer RDL test vehicle with its CD measurements.

![Figure 2. (a) Schematics of cross-section and (b) 3-layer RDL design layout of test vehicle [1].](image-url)
continued from page 11

III. Reliability Test Results
A. Leakage Current Test
Leakage current test is to measure the undesirable leakage current that flows through or across the surface of the insulation or the dielectric of a capacitor. This test is generally carried out at 2 volts of the rated input voltage of the samples under test. This test is used to help ensure that the processes and assembly practices are satisfactory and reliable.

For 2/2um and 5/5um LW/LS test vehicles, leakage current was measured as shown in Table 2. It shows quite robust leakage current performance for both ultra fine LW/LS.

<table>
<thead>
<tr>
<th>TV #1</th>
<th>2/2um (pA)</th>
<th>5/5um (pA)</th>
<th>TV #2</th>
<th>2/2um (pA)</th>
<th>5/5um (pA)</th>
</tr>
</thead>
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<tr>
<td>AVG</td>
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<td>1.397</td>
<td>AVG</td>
<td>1.047</td>
<td>1.164</td>
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<tr>
<td>MAX</td>
<td>3.066</td>
<td>3.143</td>
<td>MAX</td>
<td>1.750</td>
<td>2.543</td>
</tr>
<tr>
<td>MIN</td>
<td>0.437</td>
<td>0.481</td>
<td>MIN</td>
<td>0.149</td>
<td>0.224</td>
</tr>
</tbody>
</table>

Table 2. Leakage current test results of 2/2um and 5/5um LW/LS of 3-L RDL eWLB [1].

B. Component Level Test
JEDEC standard reliability tests of test vehicles of 3-layer RDL and minimum 2/2um LW/LS were completed. It passed JEDEC standard reliability tests used in wafer level packaging. Component level reliability was completed with the test conditions shown in Table 3.

<table>
<thead>
<tr>
<th>Component Level Test</th>
<th>Condition</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL1</td>
<td>MSL1, 260oC Reflow (3x)</td>
<td>Pass</td>
</tr>
<tr>
<td>Temperature Cycling (TC) after Precon</td>
<td>-55oC to 125oC</td>
<td>1000 x Pass</td>
</tr>
<tr>
<td>HAST (w/o bias) after Precon</td>
<td>130oC / 85% RH</td>
<td>192 hrs Pass</td>
</tr>
<tr>
<td>High Temperature Storage (HTS)</td>
<td>150oC</td>
<td>1000 hrs Pass</td>
</tr>
</tbody>
</table>

Table 3. Component Level Reliability Results of 3L RDL eWLB [1].
IV. Conclusion

In this study, ultra fine 2/2um LW/LS with 3-layer RDL was demonstrated and characterized in eWLB technology. It also passed JEDEC component level reliability test results. It provides high density interconnection such as die-to-die connects or high IO applications, such as graphics, network or high performance devices. It would be a critical factor for next generation wafer level packaging, including 2.5D/3D integration.

Advanced packaging plays a crucial role in driving products with increased performance, low power, lower cost and smaller form factor. There are many challenges that have been and are being resolved in the application of cost effective materials and processes for various reliability and security requirements. The industry requires innovation in packaging technology and manufacturing to meet current and forecasted demands and the ability to operate equipment in high volume with large throughput.

eWLB technology is an important complementary solution to standard WLP, enabling the next generation of mobile, IoT and wearable applications. The benefits of standard fan-in WLPs such as low packaging/assembly cost, minimum dimensions and height as well as excellent electrical and thermal performance are equally true for eWLB packages. The ability to integrate passives like inductors, resistors and capacitors into the various thin film layers, active/passive devices into the mold compound and 3D vertical interconnection opens additional design possibilities for new Systems-in-Package (SiP) and 2.5D/3D packaging. Moreover, next generation, SiP-eWLB/3D eWLB technology provides more value-add in performance and promises to be the new packaging platform that can expand the eWLB application range to various types of devices for true 3D SiP/module systems.

References


Process Advantages of Thermocompression Bonding

Horst Clauberg, Tom Strohmann and Bob Chylak
Kulicke and Soffa Industries, Inc.

Introduction
High I/O devices such as microprocessors, applications processors and field programmable gate arrays have transitioned from wire bonding to flip chip interconnect as the I/O counts have increased above 2000. As the bump pitch shrinks, standard flip chip bonding faces fundamental problems [1]. One key challenge to overcome was solder shorting. For pitch below about 300μm, Cu pillars with solder caps are used instead of solder balls, as shown in Figure 1. These interconnects use much less solder for a given bondline thickness and thereby allow finer pitch without shorting. Above about 100μm pitch, these can still be assembled by a standard flip chip process. But as the pitch decreases to below about 100μm, additional factors begin to inherently limit accuracy and stress control in mass reflow. Thermocompression (TC) bonding, also perhaps more aptly referred to as local reflow, provides a substantially more robust assembly solution for devices with fine pitch interconnects, high I/O count, large die or thin die. In this process, the solder is reflowed as each die is placed while position and bondline are actively controlled. The main drawback of thermocompression bonding is that it is slower than flip chip bonding because of the need to heat to reflow temperature on every placement cycle. However, a detailed cost analysis has shown that at currently achievable throughput of about 1000 units per hour, the cost differential between thermocompression and standard flip chip processes is approaching the point where it is negligible [2]. When analyzing the cost, part of the consideration is that TC bonding eliminates the need for a reflow oven, with huge savings in cleanroom floor space in addition to the expense of the oven itself. As indicated in Table 1, TC bonding with pre-applied underfill eliminates the need for flux cleaning and capillary underfill. Especially the elimination of flux cleaning equipment provides yet another tremendous saving in cleanroom space. In the end, yield considerations, which favor TC bonding, dominate the cost analysis. Adoption of TC bonding appears to be limited more by up-front capital expenditure against an installed base of flip chip bonder platforms rather than an inherent cost-of-ownership disadvantage. K&S is addressing this last issue by offering a re-configurable bonder platform that allows standard flip chip bonding today and TC bonding tomorrow.

Accuracy Advantage of TC Bonding
In a standard flip chip process, the die and substrate are held together solely by the flux and the friction between the bumps and the substrate pads as they leave the bonder and enter the reflow oven. The motions in the bonder, conveyor system and oven risk uncontrolled motions of the die. Once in the reflow oven, the viscosity of the flux drops, greatly reducing its effectiveness in protecting the die from shifting due to vibrations. More
important, the substrate expands much more than the die. The coefficient of thermal expansion (CTE) of silicon is only about 3 ppm/ºC, whereas typical organic substrates used for high end devices have a CTE of about 15 ppm/ºC. For a 10mm die, the substrate expands at least 20μm more than the die during the reflow process – that’s 10μm center to edge and there is no guarantee that the expansion will be symmetrical about the center. We can see that if the die had a pitch of 50μm with 25μm pillar diameter, the expansion would cause the pillars at the edge of the die to be misaligned by about half their width at the peak temperature.

A more detailed analysis of the accuracy limitations of flip chip bonding are shown in Figure 2. The typically accepted maximum pillar-to-lead shift is between 20 and 50% of pillar diameter after reflow. In this analysis we will take this number to be 30% and also assume that the pillar diameter is half the pitch. The diagonal line in Figure 2 shows this maximum allowable misplacement as a function of pitch. We will take the center-to-edge expansion as the misalignment due to differential thermal expansion: 10μm for every 10mm of die size. On top of this, we can add a very conservative 3μm of placement error due to the bonder itself. Even high end flip chip bonders typically have an alignment capability of 6μm at 3σ. Only those bonders that use the same slower alignment scheme as thermocompression bonders can achieve about 3μm accuracy at 3σ. Furthermore, we will neglect the error due to vibrations and handling between the bonder and the reflow oven. The dashed horizontal lines in Figure 2 represent the sum of the errors due to thermal expansion and the bonder itself for several representative die sizes. In this graph, the area above the horizontal line and below the diagonal line then represents a best-case process window with respect to accuracy. We can see that even for small die there is no process window for a conventional flip chip process below about 30μm pitch. The situation is much worse for larger die.

Warpage and Stress Advantages of TC Bonding

The same CTE mismatch that causes accuracy problems for FC bonding can also cause warpage and stress. When the solder freezes in the mass reflow oven, the die and substrate are locked to each other. Below this temperature the substrate will shrink much more than the die. If the die and substrate are thin, they will warp in a concave shape. If they are thicker and stiff, the differential contraction will cause stress on the solder joints. Again TC bonding avoids this problem by heating the die much more than the substrate, so that the contraction upon cooling is much more matched and both stress and warpage are greatly mitigated.

TC bonding with pre-applied underfill, either Non-Conducting Paste (NCP) or Non-Conducting Film (NCF), takes stress control one step further in that the already smaller stress is now taken up by the underfill even from
the very first cycle back to room temperature. Additionally, NCF and NCP provide a solution to the challenges posed to the capillary underfill process itself as bondline thickness and pitch are reduced.

TC bonding also improves bondline thickness control because advanced TC bonders have submicron control of Z height and hold the die in place until the bonding process is completed. Very thin dies also have a tendency to warp by themselves due to stress caused by the redistribution layers. TC bonding keeps these die flat during the reflow process, ensuring a uniform bondline thickness. It is for this reason that TC bonding is the process of choice for creating advanced through-silicon via memory stacks.

Throughput Innovation in TC Bonding

We have enabled a substantial cycle time reduction for thermocompression bonding with pre-applied underfill film [3]. Pre-applying underfill film to the wafer is thought to be necessary as pillar pitch decreases on flip chip packages and capillary underfill becomes more difficult. Films are replacing pastes because of better volume control and reduced risk of contamination. We have previously demonstrated a TC-NCF process that achieves 1200+ UPH. Standard TC-NCF process requires cooling to about 80°C for every bonding cycle because the transfer tool is touching the film as it hands off the die to the place tool. If the place tool is hot, the film will begin to melt, contaminating the tool and deforming the NCF film. K&S has invented and applied for a patent on a contactless transfer that allows the die to be transferred at high temperature with greatly improved throughput. Without changing any other process parameter other than the handover and contact temperature a UPH above 1700 was demonstrated. A 30 – 40% improvement in throughput and hence cost-of-ownership can be realized (Figure 3). The bond quality is unaffected by this change and the cross-section in Figure 1 is actually for a TC-NCF process with contactless high-temperature transfer. For the case of TC bonding with capillary underfill we are exploring methods of applying the flux to the substrate rather than dipping the die. This promises similar improvements in throughput.

Traceability and Statistical Process Control

Thermocompression bonding offers another advantage over mass reflow that is not as fully appreciated as it should be. In TC bonding, the process of placing and reflowing the part can be monitored die by die. All critical process parameters, such as temperature profile, force, placement position (X, Y and Z), tool vacuum, time to solder melt and a host of other information can be recorded for each die. This is in sharp contrast to a mass reflow process, where process parameters are only recorded for the aggregate of the samples going through the oven and only much more indirectly. For example, in mass reflow, temperature profiles are measured by sending an instrumented board through the oven, but this is far from monitoring the temperature for every die placement on the actual part. Going forward, ability to monitor critical parameters for each die placement in TC bonding will be exploited to enable full statistical process control – adjusting the process parameters based on the recorded trends and ensuring even tighter control of process quality and allowing the process to adjust itself for small variations in incoming material.

How to Make a Safe Investment for the Future

There are many competing technologies under development for tomorrow’s advanced packages. Extending mass reflow, thermocompression bonding, and FOWLP are three of the key ones being pursued. Subcons and IDMs are hesitant to invest in one technology over another due to the uncertainty of the future packaging volumes. K&S proposes the idea of a flexible tool which can handle multiple package types with a conversion. The concept which K&S has branded FACTS (Flexible, Adaptable, Capable, Transformable, and Scalable) is a series of machines that have adaptability across mass reflow, TCB, and FOWLP bonding. This allows for an extremely high accuracy and fast flip chip machine to be converted to a thermocompression bonder if and when the technology takes over. The wafer version of this machine can also be converted for use in FOWLP, chip first face up and face down, and chip last bonding.

Summary

There is extensive R&D underway to find a solution for ultra-fine pitch flip chip. High accuracy flip chip bonders are being developed. Advanced processes to enable high productivity thermocompression bonding have been demonstrated. OSA Ts and IDMs are hesitant to make investments without a clear understanding of their future packaging needs. K&S has introduced a bonder which can perform high accuracy flip chip and be converted to a thermocompression later if and when the technology transitions.

References

iMAPS New England 44th Symposium & Expo

Tuesday May 2nd, 2017
Holiday Inn, Boxborough, Massachusetts

THEME: The Jetsons 2017

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# MONDAY, MARCH 6, 2017

## Professional Development Courses (PDCs)

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### MORNING Professional Development Courses (PDCs) – 8:00am-12:00pm

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<th>Time</th>
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| 8:00 am – 12:00 pm | PDC1: Introduction to Copper Pillar Flip Chip Interconnect  
Course Leader: Mark Gerber, ASE US |
| PDC2: Fundamentals of Aligned Wafer Bonding  
Course Leader: Eric Pabo, EV Group |
Course Leader: Dev Gupta, APSTL, LLC |
| PDC4: Polymers in Semiconductor Packaging  
Course Leader: Jeffrey Goto, InnoCentix, LLC |

### AFTERNOON Professional Development Courses (PDCs) – 1:00pm-5:00pm

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<th>Time</th>
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| 1:00 pm – 5:00 pm | PDC5: Electrical Modeling & Test Strategies for 3D Packages  
Course Leader: Bruce Kim, City University of New York |
| PDC6: Fan Out Packaging - Technology Overview and Evolution  
Course Leader: John Hunt, ASE US |
| PDC7: Emerging Challenges in Semiconductor Packaging  
Course Leader: Raja Swaminathan, Intel |
| PDC8: Stencil Printing Technology for Advanced Semiconductor and Assembly Applications  
Course Leader: Phani VallabhaJosyula, Photo Stencil |

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### Morning Professional Development Courses: 8:00am – 12:00pm

**PDC1: Introduction to Copper Pillar Flip Chip Interconnect**

- **Course Leader:** Mark Gerber, ASE US Inc.
- **Morning PDC:** 8:00am – 12:00pm  
  - **Pricing:** $400 (Through 2/1/2017) - $450 (after 2/1/2017)

**Course Description:**

This PDC course is an introduction to the Copper Pillar Flip Chip interconnect structure, process flows, materials and package integration process methods for evolving flip chip applications. Understanding the trade-offs between traditional solder based flip chip and Copper Pillar is key in determining the silicon device layout and the type of design rules that can be leveraged. As part of this course, Copper Pillar structure formation will be reviewed as well as multiple Cu Pillar flip chip attachment methods such as Mass Reflow and Thermo-Compression Non-Conductive Paste (TCNCP) bonding. Process and equipment challenges associated with the above processes will also be reviewed. Current market trends have led to additional questions regarding the longevity of flip chip versus other competing technologies such as Fan Out Wafer Level Packaging (FOWLP). These will also be reviewed as well as a comparison between technologies.

**Who Should Attend?**

Anyone wanting to learn more about evolving Flip Chip related technologies including the basics and more about the process, material and structure options of Copper Pillar interconnect.

**Mark Gerber** is Director of Engineering & Technical Marketing at ASE-US Inc, specializing in Flip Chip and Advanced Interconnect package technologies. Mark joined ASE in Feb of 2015, and brings a diverse set of semiconductor experiences from Texas Instruments, Motorola/Freescale, and Dallas Semiconductor, including advanced interconnect and IC package development, as well as a history of new product introductions. Mark holds a bachelor’s degree in Mechanical Engineering from Texas A&M University, and has worked in the Semiconductor Industry for the last 20 years, has written 20+ papers, and currently holds over 30 patents in the area of semiconductor packaging.

**PDC2: Fundamentals of Aligned Wafer Bonding**

- **Course Leaders:** Eric Pabo, Viorel Dragoi, EV Group
- **Morning PDC:** 8:00am – 12:00pm  
  - **Pricing:** $400 (Through 2/1/2017) - $450 (after 2/1/2017)

**Course Description:**

This course will provide an overview of the processes for mechanically and optically aligned wafer to wafer bonding and chip to wafer bonding. Also the application of these processes for MEMS device manufacturing; wafer level packaging (WLP) of MEMS; 3D Integration of CMOS, Memory, and or MEMS; the manufacture of power devices; and the manufacturing of engineered substrates.

The first part of the course will be an introduction to examination of the input, process, and output variables associated with alignment and bonding. These variables will form the basis for the rest of the course. These variables apply to mechanical and optical alignment and all known types of bonding regardless of whether...
the bonding is done at a wafer level or chip to wafer level, or the bonding is permanent or temporary. The second part of the course will review the currently available processes for wafer to wafer alignment covering both mechanical and optical and be followed by a detailed examination of the currently available wafer bonding processes (Anodic, Glass Frit, Adhesive, Liquid Metal, Metal Diffusion, Direct Bonding, and Temporary Bonding). Application examples will be included in the review of each process.

After an understanding of the alignment and bonding processes has been developed, the process for selecting the optimum bonding process will be presented and reviewed. The course will conclude by reviewing process control issues for aligned wafer bonding, applicable metrology techniques and process control plans.

Who Should Attend?
Anyone interested in learning the fundamentals of aligned wafer bonding including those involved with device design, integration, process, or technology management.

**Eric F Pabo** is business development manager for MEMS for EV Group. He is a registered Professional Engineer in the State of Colorado, a Six Sigma Black Belt and has been involved with wafer level packaging and wafer bonding for the last 16 years. He has been very active in the MEMS community for the last 8 years and is a recognized expert in wafer bonding. He has authored numerous papers on wafer bonding and is well known for his enthusiastic presentation style.

**Dr. Viorel Dragoi** is Chief Scientist for Wafer Bonding at EV Group. He graduated from the Faculty of Physics at the University of Bucharest, Romania in 1995 and received his PhD from Institute of Atomic Physics Bucharest in 2000. In 1998 he joined Max Planck Institute for Materials Physics (Halle/Saale, Germany) and started working on wafer bonding process technology. Fifteen years ago he joined EV Group, Austria. His current activities are focusing on wafer bonding process development internally, in partnership with customers or in the framework of multi-partners international project. He has co-authored over 120 papers in journals and conference proceedings, and is co-author of 5 book chapters on wafer bonding applications (Research Gate score 24.33).

**PDC3: Trends and Analyses of Advanced Packaging Technologies and their Applications: from Smart Phones to Super Computers**
Course Leader: Dev Gupta, APSTL, LLC
Morning PDC: 8:00am – 12:00pm
$400 (Through 2/1/2017) - $450 (after 2/1/2017)

**Course Description:**
Increasing difficulty in pursuing Moore’s Law combined with emerging applications like Machine Learning and IoT have brought about a wider interest in integration at the package level resulting in a bounty of Adv. Packaging technologies ranging from FO WLPS and SiPs to stacked dice interconnected with Through Silicon Vias (TSVs). In addition to traditional IDMs, now OSATs and even Foundries are involved in Package development. To select appropriate Package from the wide selection available now and to predict future needs it is necessary that the Package User, Designer and even Developers and their Suppliers are able to compare these emerging Packages on the basis of not just mechanical attributes like form factor and I/O density but performance metrics and cost.

This unique course bridges the gap between courses that cover only the physical and mechanical attributes of packages and those that go into their electrical performance, cost, applications and roadmaps. We will start with an in depth description of Adv. Packaging technologies ranging from varieties of Flip Chip, FO WLPS and SiPs to 2.5d stacked dice interconnected with TSVs, their typical applications that range from Smart Phones to Super Computers, key System requirements that guide their selection, as well as current implementations.

Status of novel features / processes associated with these new Adv. Packaging technologies, e.g., micro Pillar Flip Chip technology, bond / debond wafers to carriers, TSVs will be briefly reviewed.

Next fundamentals of electrical performance, e.g., signal integrity, losses in Packages, their dependence on interconnect and Package design and metrics, e.g., Bandwidth, Power dissipation in typical computing systems will be outlined.

Based on the above performance metrics we will discuss the latest applications of FO WLPS in Smart Phones, 2.5d modules and several types of GPUs and Servers incorporating versions of stacked Memory with TSVs. Next we will compare these emerging applications on the basis of their performance and packaging costs. Finally, based on the above, we will speculate on some future directions for Adv. Packaging.

Who Should Attend?
This is an expanded version of a PDC offered at DPC for the last several years. Introductory descriptive material has been added to compromising depth. It would be of interest to Engineers, Managers and Analysts involved in Adv. Packaging.

**Dr. Dev Gupta** is CTO at APSTL LLC, Scottsdale, AZ, USA. At Motorola and Intel he pioneered and managed the discovery and implementation of many of the Adv. Packaging technologies that are industry standards today. These include electroplated solder and pillar bump flip chip technology, assembly robotics, Sn capped micro pillar technology including thermo compression flip chip bonding, organic substrates, the design of Fabs for their HVM, integrated microwave passives, industry first flip chip of Gallium Arsenide power devices, etc. At APSTL he develops and licenses Adv. Packaging technologies as well as provides turnkey engineering and ramp of plants to manufacture them. At present he is involved in developing low cost approaches to high performance die stacks. He is a frequent speaker and instructor at Packaging Conferences.

**PDC4: Polymers in Semiconductor Packaging**
Course Leader: Jeff Gotro, InnoCentrix, LLC
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/1/2017) - $450 (after 2/1/2017)

**Course Description:**
This course will provide a broad overview of polymers and the important structure-property-process-performance relationships for electronic packaging. Topics to be covered are thermostetting polymers, curing mechanisms (heat and light cured), network formation, and an overview of key chemistries used (epoxies, acrylates, polyimides, bismaleimides, curing agents, and catalysts). The course will provide a more in-depth discussion of the chemistries, material properties, and process considerations for adhesives (both paste and film), underfills (capillary, pre-applied and wafer level), polymers for fan out wafer level packaging, substrate materials, and mold compounds. In most cases, adhesives, underfills, and mold compounds are applied as a viscous liquid and then cured. The flow properties are critical to performance in high volume manufacturing. The final portion of the PDC will provide an introduction to rheological characterization methods (various types of rheometers and viscometers) and the properties of adhesives (shear thinning, viscosity, time dependence, rheology changes during curing), underfills, and mold compounds.
Who Should Attend?
Packaging engineers and R&D professionals involved in product development, manufacturing and reliability testing of semiconductor packages would benefit from the course. Specific emphasis will be on the structure-property-processing-performance relationships in semiconductor packaging.

Dr. Jeff Gotro has over thirty years experience in polymers for electronic applications and composites having held scientific and leadership positions at IBM, AlliedSignal, Honeywell, and Ablestik Laboratories. He is an accomplished technology professional with demonstrated success solving complex polymer problems, directing new product development, and enabling clients to improve the financial impact of their polymer technologies.

At InnoCentrix, Jeff has consulting experience with companies ranging from early-stage start-ups to Fortune 50 companies. Jeff is an expert in thermosetting polymers used in electronic applications and has received invitations to present lectures and short courses at national technical conferences. He has published 60 technical papers (including 4 book chapters) in the field of polymeric materials for advanced electronic packaging applications, holds 15 issued US patents, and has 4 patent applications pending. In 2014 Jeff was awarded the IMAPS John Wagnon Technical Achievement Award and was named an IMAPS Fellow of the Society. Jeff has a Ph.D. in Materials Science from Northwestern University with a specialty in polymer science and a B.S. in Mechanical Engineering/Materials Science from Marquette University.

PDC5: Electrical Modeling and Test Strategies for 3D Packages
Course Leader: Bruce Kim, City University of New York
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/1/2017) - $450 (after 2/1/2017)

Course Description:
Today’s miniaturization and performance requirements result in the usage of high-density advanced packaging technologies, such as system-in-package (SIP), direct-chip-attach, chip-scale packaging (CSP), and ball-grid-arrays (BGA). Due to their physical access limitation, the complexity and cost associated with their test and diagnosis are considered major issues facing their use.

This course introduces comprehensive knowledge of electrical modeling and test solutions for 3D packages. We begin with a short tutorial on 3D packages including interposers and TSV. We then place particular emphasis on electrical modeling; test and debugging approaches for 3D packages for RF, bio, power and MEMS packages. Finally, we cover diagnosis and repair techniques for assembled packages.

Who Should Attend?
This course is beneficial to all design and test engineers, scientists, technical managers, design and manufacturing personnel, and production staffs in automotive, consumer, communication, computer, and aerospace industries. Although the course reviews most recent advances in 3D packaging, the course does not assume prior knowledge of these issues and hence is of interest to both experts and newcomers in this area.

Bruce Kim is a professor of the Department of Electrical Engineering at City University of New York. He has about 300 publications in packaging and testing areas. He has instructed previous PDCs at IMAPS, IEEE EPTC and ECTC conferences. He is a Fellow of IMAPS and received the IMAPS Outstanding Educator award in 2012. He has also been a student chapter advisor. His research interests are in 3D passive components modeling and testing.

PDC6: Fan Out Packaging – Technology Overview and Evolution
Course Leader: John Hunt, ASE US, Inc.
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/1/2017) - $450 (after 2/1/2017)

Course Description:
Mobile electronics has created the need for ever increasing density and performance in electronics packaging with the advent of smart phones and the burgeoning Internet of Things. This evolution has led to a need for higher levels of component density and functionality than has been traditionally available using standard packaging. The packaging industry has responded with a plethora of packaging options, each tailored for a specific set of customer requirements.

We will review how the integration of a wide variety of wafer level processing technologies, substrate evolution and Flip Chip packaging structures have come together into what is being called Fan Out Packaging. These packages are for Mobile and server applications, and have higher levels of integration and sophistication than has ever been possible in the past. These options include Wafer Level Fan Out, Panel Level Fan Out with embedded die, and Chip Last Fan Out packaging. All of these can combine low cost materials and varied process flows to create both simple low density devices, and more complex System in Package and Package on Package applications. This course will provide an overview of the drivers, technology, advantages and disadvantages of various structural and processing options, as well as a view of potential future trends of Fan Out Packaging.

John Hunt is Senior Director for Engineering, Technical Promotion, at ASE (US) Inc., and provides technical support for the Introduction, Engineering, Marketing, and Business Development activities for Advanced Wafer Level and Fan Out Packaging Technologies at ASE. John has more than 40 years of experience in various areas of manufacturing, assembly and testing of electronic components and systems, with emphasis on the development of new technologies and processes, with a B.S. from Rutgers and an M.S. from University of Central Florida.
PDC7: Emerging Challenges in Packaging
Course Leader: Raja Swaminathan, Intel Corporation
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/1/2017) - $450 (after 2/1/2017)

Course Description:
The course will introduce the role of packaging in the interconnect hierarchy and introduce packaging trends per industry. We will then deep dive into key elements driving the definition of a package architecture (scaling challenges, high speed signaling, power delivery, thermo-mechanical integration as well as thermal challenges). The interactions between these elements toward enabling a successful package architecture for a given product will be reviewed. The second half of the course will focus on the package, assembly, test and silicon integration and surface mount challenges towards enabling high volume manufacturing of the package architectures.

Who Should Attend?
Attendees are expected to have an in depth understanding of the fundamentals of packaging.

Raja Swaminathan is an IEEE senior member and is a package architect at Intel for next generation server, client and SOC products. His expertise is on delivering integrated HVM friendly package architectures with optimized electrical, mechanical, thermal solutions. He is an ITRS author and INEMI TWG chair on packaging and design. He has also served on IEEE microelectronics and magnetics technical committees. He has 18 patents and 23 peer reviewed publications and holds a Ph.D. in Materials Science and Engineering from Carnegie Mellon University.

PDC8: Stencil Printing Technology for Advanced Semiconductor and Assembly Applications
Course Leader: Phani Vallabhajosyula, Photo Stencil
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/1/2017) - $450 (after 2/1/2017)

Course Description:
Stencils are used for printing flux, solder paste and inks for various assembly applications. This course will cover a wide variety of stencil printing applications including:

1. significance of stencil printing, overview of stencil manufacturing and comparison
2. stencil printing for wafer and substrate solder bumping applications
3. stencil Tools for wafer and substrate level ball drop
4. stencil printing for SMT / FC assembly
5. stencil printing on uneven substrate surfaces, including printing into deep cavities for embedded component packages

Section 1 will review the significance of stencil printing in various applications. Details of stencil printing using various printers, various tooling needed and saving in production time will be discussed. This section also reviews the different parameters that need to be considered during stencil design, followed by discussion of various stencil manufacturing technologies and comparing the same in terms of print performance.

Section 2 will review stencil design requirements to achieve specific bump height after reflow. The bump height delivered depends on the volume of solder paste printed which depends on stencil thickness, aperture size, pad pitch, % paste transfer, and Area Ratio. This section will demonstrate how to achieve maximum bump height and bump height uniformity.

Section 3 will review stencil tool requirements for ball drop at the wafer-level. First flux is printed on the wafer with a normal single thickness stencil then a special step stencil tool with a stand-off on the wafer side is used to drop balls into the flux on each pad site on the wafer. Flux stencil and ball drop stencil tool design for ball sizes ranging from 250um down to 30um and pitches ranging from 400um down to 60um will be shown.

Section 4 will review stencil printing options for SMT / FC Assembly. Typically flux is printed for FC and solder paste for SMT. Two Print Stencil printing will be reviewed. Option A is to print flux 1st and paste 2nd with a relief pocket in 2nd stencil for printed flux. Option B is to print paste 1st and flux 2nd with a relief pocket in 2nd stencil for printed paste. Advantages of both options will be discussed.

Section 5 will review 3-dimensional stencils for printing when the substrate has cavities for embedded FC on the substrate (printing into a lower surface on the PCB) and printing on the substrate having protrusions above the substrate such as mounted components. Reservoir printing into the cavities and special squeegee blades for printing around the protrusions will be discussed in detail.

Who Should Attend?
Engineers and managers responsible for advanced packaging development, package design and characterization in semiconductor, SMT, Optical (LED), automotive and aerospace industries. Both newcomers and experienced practitioners are welcome.

Phani Vallabhajosyula is Director of Applications Engineering at Photo Stencil, a stencil manufacturing company in Golden, CO. The company is involved with producing for stencils for various FC and SMT applications since 1979. Dr. Vallabhajosyula leads the company’s R&D and provides advance printing solutions to engineers from various semiconductor, LED and automotive industries. Prior to that she worked at Intel and was involved with substrate assembly process development as well as substrate design for various path finding platforms. She received her doctoral degree in materials science and engineering (Specialization in 3D printing) from the University of Texas at Austin, in 2011. She is currently a Senior member with IEEE, member of IMAPS, SMTA and serves as a reviewer for Rapid Prototyping Journal, Additive Manufacturing Journal and for Transactions on Component Packaging and Manufacturing Technology 2016.

PDC8: Stencil Printing Technology for Advanced Semiconductor and Assembly Applications
ADVANCING MICROELECTRONICS

TUESDAY, MARCH 7, 2017 Morning Technical Sessions

KEYNOTE 1:
Heterogeneous Integration: Packaging the Future
Technology innovation in the semiconductor industry continues to march forward at an incredible pace, with advancements in new silicon node technology continuing on one end of the spectrum with innovation in packaging solutions coming forward at the other in a complementary fashion. As the pace of innovation has quickened, so have the investments required to bring such technologies to production. At the packaging level, the investments required to support the advancements in silicon miniaturization and heterogeneous integration have now reached well beyond $500M USD per year. One needs to look no further than the complexity of the most advanced package technologies being used today and coming into production over the next year to understand why.

Advanced packaging technologies have increased in complexity over the years, transitioning from single to multi-die packaging, enabled by 3-dimensional integration, system-in-package (SiP), wafer-level packaging (WLP) and creative approaches to embedding die. These new innovative packaging technologies enable more functionality and offer higher levels of integration within the same package footprint, or even more so, in an intensely reduced footprint. Today, the latest in advancements in heterogeneous integrated semiconductor packaging are able to provide reduced form-factor, increased data transfer rate, improved signal integrity and memory bandwidth, all with reduced power and improved thermal performance. As we truly live in a connected world and the proliferation of connected devices is forcing continually higher system level performance, not surprisingly, it is semiconductor packaging that has stepped up to play a pivotal role in providing solutions to the new system level requirements.

Ron Huemoeller, Amkor
Ron is Corporate Vice President, Worldwide R&D, at Amkor Technology. Ron joined Amkor in 1995 and has since served in multiple senior to executive level roles. Currently, Ron is responsible for global R&D and technology strategy.

Prior to joining Amkor, Ron was Director of Engineering at Cray Computer Corp. in Colorado Springs for 5 years, leading the facilitation, startup and development of state of the art motherboards for the world’s fastest supercomputer. Ron has authored numerous technical publications, co-authored a chapter in the Handbook of 3D Stacking (McGraw Hill) and has been granted more than 100 U.S. patents. Ron holds a B.S. in Chemistry from Augsburg College with highest honors, a MBA in Business Management from Arizona State University and a Masters in Technology Management from the University of Phoenix.

KEYNOTE 2:
Neither IoT nor 5G Without New Technology!
5G networks are expected to unleash solutions that will help overcome barriers to widespread IoT adoption, such as technology hurdles leading to high connectivity costs, limited impact on user experience as well as security and privacy concerns.

Beyond the 28-nm node, new design costs increase exponentially. We cannot continue focusing on tinier transistors in the More-than-Moore era, when technology roadmaps call for heterogeneous integration, 3D and advanced packaging. Microelectronics is now led by system-driven roadmaps, and new drivers for 5G systems are diverging IoT services that require innovative flexibility and scalability from the technology. There is a new complexity in the drive of the technology roadmap since the transistor takes part of advanced system architectures where the software part is increasing.

The next step along the path of the digital era is a leap as roadmapping should be re-invented. Trends and examples of new integrated systems for IoT and 5G will be discussed in this presentation.

Lionel Rudant, CEA-Leti
Lionel Rudant is currently Strategic Marketing Manager at Leti. He draws up innovation strategies for conquering IoT markets through key enabling technologies that unleash innovative business. He has successfully transferred Leti wireless technologies to automotive, aeronautics, and industrial and consumer electronics industries, among others. He works on projects in France, Europe and the USA, and regularly presents technologies and system roadmaps at conferences and workshops.

He was awarded a postgraduate degree in electronics and digital technology by Nantes University (France) and a technology research degree by Grenoble Institute of Technology in 2003 and 2004 respectively. He then managed antenna projects for Radiall automotive and military systems. He joined Leti in 2006 and has since undertaken electromagnetics and antenna and propagation research, prompting publications on compact smart and disruptive super-directivity antennas.
**TUESDAY AFTERNOON SESSIONS**

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>TP1: 3D DEVICES and APPLICATIONS</td>
<td>TP2: FAN-OUT WAFER LEVEL PACKAGING APPLICATIONS and MATERIALS</td>
<td>TP3: PACKAGING and INTEGRATION Chair; Catherine Bunel, IPDIA; Maaike M. Visser Taklo, SINTEF This session focuses on packaging and integration technologies for engineered micro devices and systems.</td>
<td>TP4: CHAOTIC &amp; NONLINEAR SYSTEMS Chair; Ned Corron, U.S. Army; Edmon Perkins, Auburn University This session focuses on the utilization of chaos theory to enhance engineered systems.</td>
</tr>
</tbody>
</table>

**EVENING PANEL – FOWLP PRESENTED BY YOLE**

**WEDNESDAY, MARCH 8, 2017**

**GBC Keynote and Plenary Session**

**OPENING COMMENTS:**

GBC Chairs: Lee Smith, (UTAC) United Test & Assembly Center; Rich Rice, ASE Group; Kazumi Allen, Invensas

**GBC KEYNOTE:**

**GETTING THE SEMICONDUCTOR INDUSTRY GROWING AGAIN**

Since the Great Recession, the global economy has definitely had its tumultuous times. Financial and political instability along with low interest rates have resulted in “muddle through” worldwide growth. For the semiconductor industry, smartphone growth has somewhat peaked. Many are hoping that the IoT is the next growth driver, but it hasn’t blossomed yet.

The last two years have seen practically no growth in the semiconductor marketplace. What about 2017? Will it be any better? How will the semiconductor industry relate now to the “Make America Great Again” movement?

To understand this key issue, an overview analysis of the semiconductor market will be presented and its relationship to worldwide GDP, electronic products, capital spending, Foundry, and the SATS/OSAT markets.

*Jim Walker, WLP Concepts*

**Market Drivers and Packaging Trends for Automotive Electronics**

Jan Vardaman, TechSearch International

Electronic content in automotive applications has increased dramatically over the past few years. Automobiles are on the threshold of a radical change in technology. Vehicles have increased connectivity, improved self-diagnostics, a greater number of safety features including crash-avoidance technology and advanced driver assistance. What type of semiconductor packages are used in automotive electronics and what are the future challenges as new package types are adopted?

**What’s Happening in the China Advanced Semiconductor Packaging Landscape?**

Santosh Kumar, Yole Developpement

This talk will discuss the advanced packaging market in China including a forecast by the packaging technology, key Chinese and global players’ activities and government IC policy/ initiatives. Further it will include the supply chain evolution and analysis about the strategy/direction of OSATs as well as the opportunities/challenges of both local and global players in China advanced packaging space.

**Integrated Packaging and Substrate Technologies for Next-Generation Smart Devices**

Eric Huenger, Rozalia Beica, Dow Electronic Materials

This presentation will provide an overview of global trends driving the growth of Advanced Packaging, highlighting trends of packaging platforms and substrates seen today in mobile applications. An overview of the various materials and interconnect processes required at both wafer and PCB/Substrate level, across various packaging platforms (WLP, SiP, 3DIC) will be included, highlighting current industry challenges and solutions that Dow Electronic Materials is bringing to enable current and future development of smart devices.

**Title to Come**

Brandon Prior, Prismark
### INTERACTIVE POSTER SESSION and HAPPY HOUR – Wednesday Afternoon

(additional abstracts in regular session will also be invited to participate)

#### THURSDAY, MARCH 9, 2017  
**Morning Technical Sessions**

**KEYNOTE 3: Title to Come**  
Sitaram Arkalgud, Invensas

**KEYNOTE 4: Title to Come**  
Hannes Voraberger, AT&S

#### THURSDAY MORNING SESSIONS

<table>
<thead>
<tr>
<th>Interposers, 3D IC and Packaging</th>
<th>Fan-Out, Wafer Level Packaging and Flip Chip</th>
<th>SiP &amp; Engineered Micro Systems/Devices (including MEMS and Sensors)</th>
</tr>
</thead>
</table>
| THA1: 3D PROCESS TECHNOLOGY      | THA2: APPLICATIONS FCBGA ASSEMBLY and PROCESS FC ASSEMBLY | THA3: HIGH FREQUENCY  
Chairs: Li-Anne Liew, University of Colorado, Boulder / NIST;  
Keaton Rhea, Auburn University  
This session focuses on high frequency applications for engineered micro devices and systems, from GHz to optical frequencies. |

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### Exhibitors at DPC

DuPont announces new guide to non-halogenated flame-retardant polymers for the electrical and electronics industry

Latest white paper to help engineers and specifiers select polymers that comply with regulatory, environmental, safety and performance requirements

GENEVA, November 28, 2016 — Today, the electrical and electronics (E&E) industry is under unprecedented regulatory pressure to conform to tough health, safety and environmental directives that render many commonly used plastics and elastomers non-compliant. Now help is at hand with a new E&E White Paper just published by DuPont Performance Materials (DPM) that provides a step-by-step guide to the latest materials that comply with tough non-halogen, flame retardant (NHFR) requirements, looks at key emerging trends, and outlines DPM’s materials and applications development expertise.

DuPont Highlights Non-Halogen, Flame Retardant (NHFR) Options

Entitled DuPont Non-Halogenated Flame Retardant Polymers for Electrical and Electronic Applications, it is intended to help design engineers and material specifiers select DuPont products that will bring the greatest benefits to their application, by improving performance while reducing the health and environmental impact of the materials used.

“A fast track to NHFR compliance”

“DuPont is committed to solving the most challenging customer requests by providing safe, innovative and cost effective solutions backed by the broadest portfolio of NHFR products and a group of experts who can support customers globally. With that aim, I hope engineers and specifiers across the industry will download the new E&E White Paper available at now at https://goo.gl/y9lDfL — it will help provide a fast track to NHFR compliance,” says Antonio Nerone, Development Program Manager, DuPont Performance Materials.

The white paper reviews current legislation requiring the plastics and elastomers used by the industry to be halogen-free and flame-retardant, produce low smoke emissions, be recyclable, and comply with the WEEE and RoHS Directives, and the REACH Regulation on managing chemical risks and substitution. It also outlines key standards and tests for E&E industry compliance, including IEC 60335 and UL 94 for the safety of electrical appliances and the flammability of plastics used, EN 45545 for the fire testing of materials and components for trains, and UL 746 to evaluate the physical, electrical, flammability and thermal properties of polymers for electrical equipment.

Also included are DuPont solutions to many urgent E&E market needs from new energy saving and delivery systems to materials substitution, and from downsizing and lightweighting to miniaturization — accomplished by tailoring products to applications from the company’s portfolio of high-performance fully compliant NHFR products for electrical components including Crastin® PBT, Hytrel® TPE, Rynite® PET and Zytel® PPA and PA66 polyamides — backed by DuPont know-how in processing predictive engineering and Computer Aided Design.

DuPont Non-Halogenated Flame Retardant Polymers for Electrical and Electronic Applications can be downloaded at https://goo.gl/y9lDfL.

DuPont Performance Materials (DPM) is a leading innovator of thermoplastics, elastomers, renewably-sourced polymers, high-performance parts and shapes, as well as resins that act as adhesives, sealants, and modifiers. DPM supports a globally linked network of regional application development experts who work with customers throughout the value chain to develop innovative solutions in automotive, packaging, construction, consumer goods, electrical/electronics and other industries. For additional information about DuPont Performance Materials, visit plastics.dupont.com.

DuPont (NYSE: DD) has been bringing world-class science and engineering to the global marketplace in the form of innovative products, materials, and services since 1802. The company believes that by collaborating with customers, governments, NGOs, and thought leaders we can help find solutions to such global challenges as providing enough healthy food for people everywhere, decreasing dependence on fossil fuels, and protecting life and the environment. For additional information about DuPont and its commitment to inclusive innovation, please visit www.dupont.com.

Contact: Sandrine Gessier, +41 (0) 22 717 55 25, sandrine.gessier@dupont.com

Thermally Conductive, High Temperature Resistant Epoxy Passes NASA Low Outgassing Tests

Certified to meet ASTM E595 NASA low outgassing standards, Master Bond EP46HT-2AO Black is well suited for the aerospace, electronic, opto-electronic industries and can be used in vacuum environments. This two-component system blends thermal stability with a high strength profile for a variety of bonding, sealing and encapsulation applications.

EP46HT-2AO Black combines superior thermal conductivity of 9-10 BTU•in/ft2•hr•°F [1.2981-1.4423 W/
continued from page 25

(\text{m}^\circ\text{K})$ and reliable electrical insulation with a volume resistivity exceeding $10^{14}$ ohm-cm at room temperature. It has a glass transition temperature of 200-210$^\circ$C and is serviceable over the wide temperature range of -100$^\circ$F to +500$^\circ$F [-173$^\circ$C to +260$^\circ$C]. This dimensionally stable system delivers a tensile strength of 6,000-7,000 psi, compressive strength of 26,000-28,000 psi and tensile lap shear strength of 1,400-1,600 psi at 75$^\circ$F. EP46HT-2AO Black also withstands a variety of chemicals including oils, water, acids, bases and fuels.

Unlike most traditional two-part epoxies, EP46HT-2AO Black cures with the addition of heat, which allows it to have a working life of over 24 hours. It has a forgiving 100 to 30-35 mix ratio by weight and upon mixing, this thixotropic system has a viscosity of 140,000-280,000 cps. It bonds well to metals, composites, glass, ceramics, rubbers and many plastics.

This epoxy is available in 1/2 pint, pint, quart, gallon and 5 gallon container kits. Part A of this system is black in color and Part B is gray. EP46HT-2AO Black has a minimum 6 month, maximum 1 year shelf life at ambient temperatures in original, unopened containers.

**Master Bond Thermally Stable Adhesives**

Master Bond EP46HT-2AO Black is a thermally conductive and electrically insulative adhesive, sealant and potting compound that meets NASA low outgassing requirements. This high strength, two component epoxy withstands temperatures up to +500$^\circ$F. Read more about Master Bond’s heat resistant adhesives at http://www.masterbond.com/properties/high-temperature-resistant-bonding-sealing-and-coating-compounds or contact Tech Support. Phone: +1-201-343-8983 Fax: +1-201-343-2132 Email: technical@masterbond.com.

**PRODUCT FOCUS**

**Adhesives for your specific needs**

**X5TC: One Part, Thermally Conductive Elastomeric System**

Elastomeric adhesive system, X5TC delivers thermal conductivity of 10-12 BTU/min/ft$^2$/hr°F [1.44-1.73 W/m•K] while maintaining excellent electrical insulation properties. It is well suited for bonding dissimilar substrates and performs well when subjected to thermal cycling, vibration, shock and related forces. This system offers solid tensile lap shear and T-peel strength. X5TC has a paste-like consistency and cures at room temperature or more quickly with the addition of heat.

X5TC bonds well to many substrates including metals, glass, composites, ceramics, rubbers and plastics. Since it is elastomeric, this compound is suitable for bonding dissimilar substrates and performs well when subjected to thermal cycling, vibration and shock.

X5TC can be used in aerospace, electronic and specialty OEM applications. The service temperature range of this product is from -80$^\circ$F to +230$^\circ$F; although it can withstand brief exposure to temperatures as high as 350-400$^\circ$F. It has good resistance to water and oils. This compound is available for use in ounces, 1/2 pints and pints containers.

**Master Bond Elastomeric Adhesives**

Master Bond X5TC is a thermally conductive, electrically insulative adhesive with superior strength properties. This one-part elastomeric system has convenient handling properties. Read more about Master Bond’s elastomeric adhesives at http://www.masterbond.com/products/elastomeric-systems or contact Tech Support. Phone: +1-201-343-8983 Fax: +1-201-343-2132 Email: technical@masterbond.com.


**EP76MHT: Nickel Filled Epoxy Withstands Temperatures Up to +400$^\circ$ F**

Two component EP76MHT is an adhesive, sealant and coating that features impressive electrical conductivity with a volume resistivity of 5-10 ohm-cm. This easy to handle system is formulated to cure at room temperature or more rapidly at elevated temperatures. When fully cured, EP76MHT, has a lap shear strength of over 2,100 psi. It has superior dimensional stability and low shrinkage upon cure. This epoxy also offers excellent thermal conductivity of 8-9 BTU•in/ft$^2$/hr°F [1.15-1.30 W/m•K].


**EP21TPLV: Compound with Excellent Resistance to Chemicals**

Featuring a unique blend of outstanding toughness and chemical resistance, EP21TPLV can withstand exposure to water, gasoline, oils, hydrocarbons, fuels, hydraulic fluids and many acids and bases. Often used as a sealant, it is also very effective as an adhesive, coating and encapsulant. This two-part epoxy polysulﬁde is easy to handle with a convenient, one to one mix ratio by weight or volume. Shore D hardness is 60-65.


**MasterSil 713: Low Viscosity, One Component Fast Curing Silicone**

Ideal for smaller encapsulations and conformal coating applications, MasterSil 713 is an easy to use one component silicone with an exceptionally low viscosity. This self leveling system cures rapidly at room temperature and is non-corrosive. Speed of cure depends upon the level of humidity and the thickness of the layer being cured. It can be cured in thicknesses up to 1/4 inch deep with superb flexibility and elasticity. MasterSil 713 also offers outstanding electrical insulation properties and is serviceable up to +400$^\circ$F [+204$^\circ$C].

Michael Dalan Glover

The Department of Electrical Engineering and the College of Engineering of the University of Arkansas are mourning the loss of Michael Dalan Glover, 45, research assistant professor, who passed away October 27, 2016.

Glover graduated from Watson Chapel in 1989 and then attended the University of Arkansas, receiving his B.S.E.E. in 1993, his M.S.E.E. in 1994, and after many years of hard work, he received a doctorate in electrical engineering in 2013. He worked at the university for 22 years, most recently as a research assistant professor of electrical engineering.

Glover was director of the Ceramic Integration Laboratory at the High Density Electronics Center (HiDEC). Having contributed at the center in various roles since 1993, he managed a number of electronic integration-related projects and produced hundreds of mask and printed circuit board designs for various thin film, ceramic, and hybrid electronic projects. His research interests included the packaging/integration of wide bandgap power devices. He also had interests in computer-aided design and manufacturing, computer architecture, programming, microelectronic packaging and fabrication, and digital systems.

Glover had a great impact on everyone he met. He was a mentor to many students and was a friend to faculty and staff at the electrical engineering department, at the College of Engineering and across the university. His work as a research associate and then as a research assistant professor made him a valuable member of the HiDEC team, as well as other research efforts in the department. He was also a liaison to many industry partners who worked with HiDEC and the department through the years.

Glover received the William D. and Margaret A. Brown Staff Excellence Award in 2011. He was active in the Farmington Cub Scouts and enjoyed spending time with his family. He was a member of the IEEE Components, Packaging and Manufacturing Technology Society, the IEEE Power Electronics Society, and Eta Kappa Nu. Michael was also a member of the Amateur Radio Club of the University of Arkansas and enjoyed using Ham Radio to make contacts all over the world.

The comments of department head Juan Balda expressed the feelings of everyone in the department: “Mike was a fine individual who took joy and pride in teaching students; many have completed their graduate degrees because of Mike being there to support their experiments or prototype fabrication. He is leaving behind a large space that will be difficult to fill with one individual.”

Simon Ang, professor of electrical engineering and director of the High Density Electronics Center, said, “This is a great loss to HiDEC. Mike dedicated his professional career to this center and his legacy extends way beyond its boundaries.”

A funeral service was held November 4 at Little Elm Missionary Baptist Church in Farmington, Arkansas, with burial in the Farmington Cemetery. In lieu of flowers, memorials may be made to an education account for Glover’s children at First Security Bank, Attn: Beverly Pergeson, P.O. Box 249, Springdale, AR 72765.

Industry News...continued from page 26

EP42-2LV: Low Viscosity Epoxy Features Outstanding Chemical Resistance

Master Bond EP42-2LV is a two-component epoxy adhesive, sealant, coating and casting compound featuring outstanding chemical resistance and electrical insulation properties. It is castable to thicknesses exceeding 2-3 inches and is serviceable from -60°F to +300°F [-51°C to +149°C]. The low viscosity of EP42-2LV enables it to be particularly desirable for potting and encasulations as well as coatings. This epoxy system is ideal for aerospace, electronic, electrical, fiber-optic and optical applications.


EP3HTMed: Chemically Resistant Polymer Adhesive Meets USP Class VI Specifications

Master Bond EP3HTMed fully meets USP Class VI requirements and is formulated to cure at elevated temperatures. It has excellent resistance to radiation, EtO, autoclaving and chemical sterilants. EP3HTMed has a service operating temperature range of -60°F to +400°F [-51°C to +204°C], is 100% reactive and does not contain any diluents or solvents. Another benefit of this single component, no mix epoxy adhesive is its unlimited working life and its thixotropic paste viscosity.


CONTACT: James Brenner, Marketing Manager, Email: jbrenner@masterbond.com, Tel: +1-201-343-8983, Fax: +1-201-343-2132
Master Bond
154 Hobart Street, Hackensack, New Jersey 07601
United States
IMAPS ATW on Advanced Packaging for Medical Microelectronics

January 31 and February 1, 2017
San Diego, CA
www.imaps.org/medical

Early Registration and Hotel Deadline: January 6, 2017

THANK YOU TO OUR PREMIER SPONSORS!

The International Microelectronics Assembly and Packaging Society (IMAPS) will host an Advanced Technical Workshop in San Diego on Advanced Packaging for Medical Microelectronics on January 31 and February 1, 2017. The workshop will bring together technologists in semiconductor packaging with life science experts interested in applying advanced packaging methods to enable the next generation of medical microelectronic devices. The workshop will provide a venue for presentations and discussions focused on traditional and emerging packaging technologies for wearable, portable and implantable devices, medical instrumentation, and life sciences consumables. Attendees and Exhibitors will be exposed to a wide variety of disciplines to encourage new products, discussions and collaborations. This two-day event will draw invited experts in medicine, sensing, microelectronics, and semiconductor packaging.
# Keynote Presentation: Challenges for Hermetic Packaging of Wireless Brain Implants for Chronic Use

**Abstract:** A key challenge for the development of high data rate implantable electronic brain interfaces for chronic use is the hermetic sealing of the microelectronics to small form factor, electro-magnetically transparent enclosures. One contemporary challenge is implants on the microscale where biocompatible packaging is required on sub-mm scale active integrated circuits.

**Arto Nurmikko | Brown University**

Arto V. Nurmikko, a native of Finland, is a L. Herbert Ballou University Professor of Engineering and Physics at Brown. Professor Nurmikko conducts research in neuroengineering, brain sciences, nanophotonics and microelectronics, especially for the translation of device research to new technologies in biomedical, life science, and photonics applications. His current interests include development of implantable wireless neural interfaces, nanoscale neural circuit sensors, and compact red/green/blue semiconductor lasers. Nurmikko has published in several fields (about 400 articles), led many multi-institutional research teams, advised federal funding agencies, and lectured worldwide. Professor Nurmikko is a Fellow of the American Physical Society, Fellow of the Institute of Electrical and Electronics Engineers, and Fellow of the Optical Society of America. He has been elected to the American Academy of Arts and Sciences and the Academy of Letters and Science of Finland.

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### SESSION 1  MICROELECTRONIC BIO-DEVICES, APPLICATIONS, BUSINESS TRENDS

**Session Chair:** Tim LeClair, Cerapax

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<thead>
<tr>
<th>Time</th>
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<tr>
<td>10:00am-10:30am</td>
<td>TITLE to Come</td>
<td>Carrie So, Illumina</td>
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<tr>
<td>10:30am-11:00am</td>
<td>Coffee Break in the Exhibit/Session Room (Crystal Ballroom)</td>
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<td>11:00am-11:30am</td>
<td>System Integration and Hermetic Encapsulation of an Active Neural Probe for Intra-Fascicular Implantation in the Peripheral Nervous System</td>
<td>Maaike Op de Beeck, IMEC</td>
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<td>Tzannis Alexios, IMT</td>
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<td>12:00pm-1:00pm</td>
<td>Lunch in the Terrace Room</td>
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<td>PANEL DISCUSSION:</td>
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<td>Moderator: Kedar Shah, Verily Life Sciences</td>
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### SESSION 2  COMPONENT “ULTRA-MINIATURIZATION” STRATEGIES

**Session Chair:** Matt Nowak, Qualcomm

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<tr>
<td>2:00pm-2:30pm</td>
<td>Development of Deep Discharge Capable Micro-Batteries for Implantable Medical Devices</td>
<td>Ryo Tamaki, EnerSys Quallion (Sor Mohanty, Hiroshi Nakahara)</td>
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<tr>
<td>2:30pm-3:00pm</td>
<td>Challenges Designing Highly-Integrated Implantable Microsystems: Intraocular Pressure Measurement</td>
<td>Razi Al Haque, Dose Medical</td>
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<tr>
<td>3:30pm-4:00pm</td>
<td>Benefits of Packaging for RF Communications in Implantable Medical Devices</td>
<td>Perry Li, St. Jude Medical</td>
</tr>
<tr>
<td>4:00pm-4:30pm</td>
<td>Advanced Chip Mounting Technologies for Ultra-Miniaturized Implants</td>
<td>Gaston Boulard, Valtronic (Rainer Platz)</td>
</tr>
<tr>
<td>4:30pm-5:00pm</td>
<td>The Use of Advanced Microelectronic Packaging Techniques to Miniaturize an Implantable Neuro Stimulator</td>
<td>Jim Ohneck, AEMtec GmbH</td>
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<tr>
<td>5:00pm-5:30pm</td>
<td>Cocktails and Networking in the Exhibits Area</td>
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**IMAPS ATW on Advanced Packaging for Medical Microelectronics**

**TUESDAY, JANUARY 31**

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<thead>
<tr>
<th>Time</th>
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<tr>
<td>7:00am-5:00pm</td>
<td>Registration Open</td>
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<tr>
<td>9:00am-6:00pm</td>
<td>Exhibits Open <em>(when not in session)</em></td>
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<tr>
<td>8:00am-8:45am</td>
<td>Breakfast</td>
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<tr>
<td>9:00am-9:15am</td>
<td>Opening Remarks: General Co-Chairs – Tim LeClair, Cerapax; Vern Stygar, Asahi Glass Company; Matt Nowak, Qualcomm</td>
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<tr>
<td>9:15am-10:00am</td>
<td><strong>KEYNOTE PRESENTATION:</strong> Challenges for Hermetic Packaging of Wireless Brain Implants for Chronic Use</td>
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Abstract: A key challenge for the development of high data rate implantable electronic brain interfaces for chronic use is the hermetic sealing of the microelectronics to small form factor, electro-magnetically transparent enclosures. One contemporary challenge is implants on the microscale where biocompatible packaging is required on sub-mm scale active integrated circuits.

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**MICROELECTRONIC BIO-DEVICES, APPLICATIONS, BUSINESS TRENDS**

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<td>Development of Deep Discharge Capable Micro-Batteries for Implantable Medical Devices</td>
<td>Ryo Tamaki, EnerSys Quallion (Sor Mohanty, Hiroshi Nakahara)</td>
</tr>
<tr>
<td>2:30pm-3:00pm</td>
<td>Challenges Designing Highly-Integrated Implantable Microsystems: Intraocular Pressure Measurement</td>
<td>Razi Al Haque, Dose Medical</td>
</tr>
<tr>
<td>3:00pm-3:30pm</td>
<td>Coffee Break in the Exhibit/Session Room (Crystal Ballroom)</td>
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</tr>
<tr>
<td>3:30pm-4:00pm</td>
<td>Benefits of Packaging for RF Communications in Implantable Medical Devices</td>
<td>Perry Li, St. Jude Medical</td>
</tr>
<tr>
<td>4:00pm-4:30pm</td>
<td>Advanced Chip Mounting Technologies for Ultra-Miniaturized Implants</td>
<td>Gaston Boulard, Valtronic (Rainer Platz)</td>
</tr>
<tr>
<td>4:30pm-5:00pm</td>
<td>The Use of Advanced Microelectronic Packaging Techniques to Miniaturize an Implantable Neuro Stimulator</td>
<td>Jim Ohneck, AEMtec GmbH</td>
</tr>
<tr>
<td>5:00pm-5:30pm</td>
<td>Cocktails and Networking in the Exhibits Area</td>
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**continued on page 30**

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### ADVANCING MICROELECTRONICS

**IMAPS ATW on Advanced Packaging for Medical Microelectronics**

#### WEDNESDAY, FEBRUARY 1

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
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<tbody>
<tr>
<td>7:30am-5:00pm</td>
<td>Registration Open</td>
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<tr>
<td>8:30am-5:00pm</td>
<td>Exhibits Open (when not in session)</td>
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<tr>
<td>7:30am-8:30am</td>
<td>Breakfast</td>
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<tr>
<td>8:30am-8:45am</td>
<td>Opening Remarks: General Co-Chairs –</td>
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<td></td>
<td>Tim LeClair, Cerapax; Vern Stygar, Asahi Glass Company; Matt Nowak, Qualcomm</td>
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<tr>
<td>8:45am-9:30am</td>
<td><strong>KEYNOTE PRESENTATION:</strong></td>
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<tr>
<td></td>
<td>Material Solutions for RF Connected Medical and Healthcare Devices</td>
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<td></td>
<td>Abstract: In the last decade, we have experienced tremendous change in mobility of personal devices. During this period, “anywhere” and “anytime” has become very common in our daily lives. Wireless technology has emerged as the key enabler for this functionality. In addition to these functionalities, “any device formats” have become more common in personal devices. Under these circumstances, new devices for medical and healthcare are connected through advanced personal device networks. To orchestrate wireless technologies for medical and healthcare needs, we believe there are new opportunities in the packaging industry. It is so-called “Smart phone centric” world. “Any device formats” can expand the new business opportunities. Many of these new devices require new technology both in materials and packaging technologies. In material, chemical durability, electrical properties and optical properties are required. In packaging technologies, small form factor and mechanical durability are also required. Combining knowledge from both industries, we can bring these new devices from lab to road. AGC is a leader in specialized glass compositions not only for electronics and RF devices, but medical devices. AGC has lead the way to commercialize specialize forms, chemistry and surface functionality to enable convergence of such disciplines as chemistry, photonics and electronics. AGC’s nano and micro fabrication technologies will enable the designer to produce devices both in electronics and biomedical applications. AGC has developed in via formation, metallization, coatings and nanoimprint capabilities. These technological platform in electronics will offer a synergistic discipline approach for the next generation of medical devices. In this presentation we will elaborate on material solutions for “being connected”: the blurring of the lines between RF and medical devices. Nobuhiko Imajyo</td>
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<td>GM, Technology Planning &amp; Development, Technology Development General Div., AGC Electronics</td>
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<tr>
<td>9:30am-10:00am</td>
<td><strong>SESSION 3</strong> MATERIALS DEVELOPMENT, ASSEMBLY, AND RELIABILITY</td>
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<td>Session Chair: Vern Stygar, Asahi Glass Company</td>
</tr>
<tr>
<td>9:30am-10:00am</td>
<td>Embedding of Active Components in LCP for Implantable Medical Devices</td>
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<td>Eckhardt Bihler, Dyconex AG / MIST (Marc Hauer, Susan Bagen)</td>
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<tr>
<td>10:00am-10:30am</td>
<td>Advanced Cermet Ceramic Composites for Encapsulation of Medical Devices</td>
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<td>Robert Dittmer, Heraeus Medical Components (Ulrich Hausch, Jens Trötschel)</td>
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<tr>
<td>10:30am-11:00am</td>
<td>Coffee Break in the Exhibit/Session Room (Crystal Ballroom)</td>
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<tr>
<td>11:00am-11:30am</td>
<td>High-Density Flex Circuits Serve as Enabling Interface for Medical Sensors</td>
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<td></td>
<td>Scott Corbett, MicroConnex Inc.</td>
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<td>11:30am-12:00pm</td>
<td>TITLE to come</td>
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<td></td>
<td>Ray Karam, Invenios</td>
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<tr>
<td>12:00pm-1:00pm</td>
<td>Lunch in the Terrace Room</td>
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<tr>
<td>1:00pm-2:00pm</td>
<td><strong>PANEL DISCUSSION:</strong></td>
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<td>TOPIC to come</td>
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<tr>
<td></td>
<td>Moderator: Caroline Bjune, Draper Labs</td>
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</tbody>
</table>
2:00pm-2:45pm  
KEYNOTE PRESENTATION:  
Medical Application Opportunities Enabled by Microelectronics Technology Evolution 

Microelectronic sensors are a key enabling technology for health and wellness monitoring, one of the most exciting growth areas on the horizon. A recent study predicts that sensors will enable a $75 billion wearables technology market by 2025—with health and wellness as a significant application area. The study forecasts 3 billion wearable sensors by 2025, with about 1/3 being new sensor types. Where there are sensors, there are needs for other microelectronic components, e.g., analog frontend, microprocessor, memory, wireless radio, charging modules, etc. To the extent that these microelectronic components have to be collocated with the sensors, the sensor packaging requirements also extend to them.

Use of microelectronic sensors to monitor the health condition of chronic disease patients is key to the quality of life of the patient and to reduction of cost of health care—by keeping the patient out of the hospital and emergency rooms. Chronic diseases account for 75%+ of the US health care expenditures, i.e., $2 trillion; 141 million (45% of the population) have at least one chronic disease, 72 million of which have two or more. Examples of prevalent chronic diseases are hypertension, obesity, arthritis, asthma, chronic kidney disease, depression, chronic obstructive pulmonary disease (COPD), diabetes, sleep disorder and heart failure.

This presentation will elaborate on sensor packaging technology and cost evolution, as well as areas of application opportunity for microelectronic sensors.

Mehran Mehregany, Ph.D. | Case School of Engineering San Diego

Mehran Mehregany is an innovator, researcher, educator, and an entrepreneur. His interests are in sensors, micro/nano-electro-mechanical systems, silicon carbide microsystems, wearables, wireless health, and innovation models. He has made notable research and/or commercialization contributions in each of these areas.

He received his M.S. and Ph.D. in Electrical Engineering from Massachusetts Institute of Technology in 1986 and 1990, respectively. Thereafter, he joined Case Western Reserve University as an assistant professor in the Electrical Engineering and Computer Science Department. He is currently the Founding Director of Case School of Engineering San Diego, where he developed and launched the wireless health and wearable computing graduate programs in 2011 and 2014, respectively. He holds the Veale Professor of Wireless Health Innovation endowed chair, and previously held the Goodrich (2000-2015) and the George S. Dively (1997-2000) endowed chairs. He has a secondary appointment in the Biomedical Engineering Department.

SESSION 4  
EXPEDITING NEW PRODUCTS, APPROVALS, ROADMAPS

Session Chair: Susan Bagen, MST

2:45pm-3:15pm  
Development of a Catheter: A Case Study in Material Selection, Design and Process Development for a High Yield and Reliable Medical Device  
Dennis Barbini, Universal Instruments

3:15pm-3:45pm  
Coffee Break in the Exhibit/Session Room (Crystal Ballroom)

3:45pm-4:15pm  
Bio-Device Forecasts  
Steve LaFerriere, Yole

4:15pm-4:45pm  
Electrodeposited Platinum-Iridium Alloys for Enabling Flex Circuit Leads for Implantable Neuromodulation Applications  
Jack Whalen, Platinum Group Coatings, LLC

4:45pm-5:00pm  
Closing Remarks

continued on page 32
**Registration Information:** Register Online: www.imaps.org/medical

Full attendee registrations (not exhibits only) includes the sessions, meals, breaks, exhibit attendance, reception, and lunches. Also includes one Download of the post-workshop presentation slides, and an automatic one-year IMAPS membership renewal for individual and student members in good standing at the time of registration. All prices below are subject to change. **No refunds issued after January 6, 2017.**

<table>
<thead>
<tr>
<th>Type</th>
<th>Advance/Onsite Fee After 1/6/2017</th>
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<tr>
<td>IMAPS Member</td>
<td>$600</td>
</tr>
<tr>
<td>Non-Member</td>
<td>$700</td>
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<tr>
<td>Speaker</td>
<td>$300</td>
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<tr>
<td>Chair</td>
<td>$300</td>
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<tr>
<td>Chapter Officer</td>
<td>$400</td>
</tr>
<tr>
<td>Student</td>
<td>$150</td>
</tr>
<tr>
<td>Premier Event Sponsorship w/ Exhibit Tabletop</td>
<td>$1500</td>
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<tr>
<td>(includes: 1 tabletop exhibit w/ 1 booth badge, 1 attendee registration, print advertisement in programs, flyer/giveaway distributed to all attendees, logo/advertisement on event webpages)</td>
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</tbody>
</table>

**Hotel Information** – Reservations must be made directly with:

Handlery Hotel
950 Hotel Circle N.
San Diego, CA 92108

Single/Double: $109/night + taxes/fees

**Phone Reservations ONLY** - Contact hotel directly: 800-238-6111 and request the group rate of $109+tax for the International Microelectronics Assembly and Packaging Society. **There is no online booking link for this hotel.**

**Note:** This is not a block, but a courtesy rate. It is subject to availability of rooms, so guests are encouraged to book as soon as possible to get the rate. There is no pre-determined cutoff date.

**Tabletop Exhibition** – Be sure to visit companies in the exhibit area during your time at Medical 2017!

**EXHIBITOR HOURS:**
- Tuesday, January 31: 9:00am-6:00pm (when not in session)
- Wednesday, February 1: 8:30am-5:00pm (when not in session)
CHAPTER NEWS

Your IMAPS Member Benefits at Your Chapter Level

Your participation in these IMAPS chapter events greatly increases the value of your member benefits by providing industry insight, technical information, and networking opportunities. See more event information at www.imaps.org/calendar

Indiana Chapter

The Indiana Chapter held its November 13th meeting with a tour of MicroScreen in South Bend, Indiana. We had 8 people present for the tour. Tom Thomas, founder of Syscon and MicroScreen, gave us a brief history of the company. Mark Loudermilk and Holly Wise gave us a very thorough tour of their screen and stencil areas along with capabilities. A Certificate of Appreciation was presented after the tour.

After the tour, we had our dinner at the ever-popular Tippecanoe Place Restaurant. Due to the long-distance travel schedules of everyone, we had a brief business meeting with our meal.

Treasurer Keith Magiera gave a report on Chapter finances with $10,014.96 in our account. Keith is also working on a tour for our March, 2017 meeting at Wood Mizer in Indianapolis. Details will be forthcoming early in the year. This sounds to be a very interesting tour of their wood cutting machinery.

President Larry Wallman gave quick summaries and updates. Tim Brooks, formerly of Grote, is now VP at Key Electronics in Jeffersonville. Long time chapter supporter of our Vendor’s Day and advertiser, Steve Beigle of Henkel, is retiring December 1. We wish him the best since we are losing a good friend. Our Electronics Technology Exchange at WestGate/Crane is scheduled for May 9, 2017 at WestGate Academy. Numerous suggestions have been given for speakers and topics as well as very good ideas for the supplier area. We had a very good 2016 event and are looking forward to an even better 2017. Larry Wallman is working on a planning meeting with the Crane and West Gate people mid to late January to get the ball rolling for May 9. As usual, additional comments and suggestions are always welcome and taken seriously.

It was also a pleasure that Mark Loudermilk, Holly Wise and Kathy Thomas, all of MicroScreen could join us for dinner. The dinner meeting adjourned at 7:30 PM.

Submitted by,
Larry Wallman
Indiana IMAPS President

MEMBER NEWS

Welcome New IMAPS Members!

October - December 2016

Organization Members
Essentec USA
Bach Resistor Ceramics GMBH
Semplexics LLC
SCREEN Finetech Solutions Co., Ltd
Enzo Technology Corp
TEN TECH LLC
SMART Microsystems Ltd
Mitsui Mining & Smelting Co., Ltd
Dexterials America Corporation

Individual Members
Sara Abbasrzagaleh
Gil Aguilar
Omar Ahmed
Elham Vakil Asadollahei
Hiromichi Asahara
Jan Paul Bach
Brian Barry
Wendy Barry
David Belliveau
Robert Buchanan
Andrew Burns
Zach Burton
Rodd Cairns
Michael Carr
Juan Castro
Wen-Chen Chen
LS Chen
Mike Cole
Mark Colgan
Jolanda Creech
Arturs Dunbergs
Jonathan Dixon
Peter Donegan
Bill Easter
Bill Evans
John Federici
Risei (Paul) Furuya
Amir Ghosh
Stephen Giardini
Yuan Gu
Anne Hackney
Matthew Hagedon
Ehsan Hajisaeid
Casey Hamann
Erik Hardy
Dana Hankey
John Hannafin
Elica Harper
Sean Hart
Mary Herndon
Travis Hillyer
Daniel Hines
Kyle Homan
Jeng-Shien Hsieh
Nathan Isser
Golarch Jalilvand
Ronald Janek
William Jarvis
Kalana Jayawardana
Bharath Kumar Kadimella
Himal Khatri
Ed Kingsley
Mari Kovach
Tim Lai
Thomas Lawrence
Claire Lepont
Richard Lewis
Anny Lo
Alina Lusebrink
Scott MacKenzie
Jose Martinez
Randi McQuarrie
Joey Mead
Craig Miller
Vincent Miyeli
Adrien Morard
Amir Namin
Kristian Oliebro
Kenny Ogawa
Kristi Pance
Zhenlin Pei
Steve Pollock
Oshadha Ranasingha
Benjamin Redman
Carolyn Reistad
Seth Rhodes
Amanda Rickman
Ricardo Rodriguez
Sam Song
Susan Stanievich
Bob Stevenson
Brandon Summey

Submitted by,

Larry Wallman
Indiana IMAPS President
ABSTRACTS DUE: JANUARY 18, 2017

Goal
The Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT) conference brings together a diverse set of disciplines to share experiences and promote opportunities to accelerate research, development and the application of ceramic interconnect and ceramic microsystems technologies. This international conference features ceramic technology for both microsystems and interconnect applications in a dual-track technical program. The Ceramic Interconnect track focuses on cost effective and reliable high performance ceramic interconnect products for hostile thermal and chemical environments in the automotive, aerospace, lighting, solar, defense/security, and communication industries. The Ceramic Microsystems track focuses on emerging applications and new products that exploit the ability of 3-D ceramic structures to integrate interconnect/packaging with microfluidic, optical, micro-reactor and sensing functions. Tape casting, thick film hybrid, direct write and rapid prototyping technologies are common to both tracks, with emphasis on materials, processes, prototype development, advanced design and application opportunities.

Ceramic Interconnect Track
Conventional thick and thin film ceramic technologies are being revolutionized and extended through the development of low temperature co-fired ceramics, photo patterning, and embedded passive component materials and processes. These have contributed to increased circuit density, enhanced functionality, and improved performance that are being adopted for leading edge applications in wireless and optical communications, automotive, MEMS, sensors, and energy. Data communications and the Internet are driving the demand for bandwidth, sparking demand for optical communication equipment and new interconnect and packaging applications that perform at 40 Gb/sec and beyond. In under-the-hood electronics for automotive, engine/transmission control, communications, and safety applications continue to drive the growth of ceramic interconnect technology, while collision-avoidance systems are creating interest in low loss ceramic materials for frequencies approaching 100 GHz.

Ceramic Microsystems Track
Enabled by the availability of commercial ceramic, metal and embedded passives materials systems, and the rapid prototyping capabilities of the well established multilayer ceramic interconnect technology, three dimensional (3-D) functional ceramic structures are spawning new microsystems applications in MEMS, sensors, microfluidics, bio-devices, microreactors, and metamaterials. These new devices and applications exploit the ability to integrate complex 3D features and active components (e.g., valves, pumps, switches, light pipes, and reaction chambers).

In addition, the Ceramic Microsystems track of the CICMT conference targets new developments in microsystems that include fabricating 3-D micro device structures enhanced with sol-gel, advanced printing and patterning technologies, high temperature materials technologies, and emerging applications like energy harvesting. Many of these innovative applications are taking advantage of the unique ability to integrate the thermal, chemical, mechanical and electrical properties of these multicomponent ceramic-metal systems.

Special Features
• Invited keynote and international presentations on the current status ceramic technology and future system directions.
• A focused exhibition for suppliers who support the use of the technologies.
• A technical poster session to promote student participation.
• Social events to promote new contacts.
Planned Session and Paper Topics Include:

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<th>Ceramic Interconnect</th>
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<td><strong>Markets and Applications</strong></td>
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<td>• MEMS Technology and Markets</td>
<td>• Automotive</td>
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<td><strong>Materials and Properties</strong></td>
<td><strong>Materials and Properties/Functions</strong></td>
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<td>• Materials Integration and Nano-materials</td>
<td>• Dielectric and Magnetic Materials</td>
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<td>• Thermal Management and Reliability</td>
<td>• Embedded and Integrated Passives</td>
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<td>• Piezoelectric Materials</td>
<td>• Microwave/mm Wave Characterization</td>
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<td>• Optoelectronics</td>
<td>• Zero-shrink Ceramic Systems</td>
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<td><strong>Processing and Manufacturing</strong></td>
<td><strong>Processing and Manufacturing</strong></td>
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<td>• MEMS Manufacturing Technology</td>
<td>• LTCC and Multilayer Ceramics</td>
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<td>• Industrial Automation and Rapid Prototyping</td>
<td>• Roll to Roll and Continuous Manufacturing</td>
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<td>• Nano-technology/Integration</td>
<td>• Direct Write and Drop on Demand</td>
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<td>• High Temperature Microsystems</td>
<td>• Advanced Thick Film Processing</td>
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<td><strong>Devices</strong></td>
<td><strong>Fine Structuring Technologies</strong></td>
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<td>• Sensors and Actuators</td>
<td><strong>Devices</strong></td>
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<td>• Micro-reactors</td>
<td>• Circuits, Antennas, and Filters</td>
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<td>• Fluidic Devices</td>
<td>• Embedded Structures and Components</td>
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<tr>
<td>• Biomolecular and Cell Transport Systems</td>
<td>• Optical Devices and Optoelectronics</td>
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<tr>
<td>• Energy Conversion Systems</td>
<td><strong>Characterization and Reliability</strong></td>
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<td><strong>Characterization and Reliability</strong></td>
<td>• Characterization of Green Tapes</td>
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<td>• Materials and Process Characterization</td>
<td>• Life Testing, Quality Issues</td>
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<td>• Systems Reliability, Lifetime, and Failure Estimation</td>
<td>• RF Performance</td>
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<td>• Reliability of High-Performance Microsystems</td>
<td><strong>Design, Modeling, and Simulation</strong></td>
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<tr>
<td><strong>Design, Modeling, and Simulation</strong></td>
<td>• High Frequency Design Software</td>
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<td>• Thermal and Heat Transfer</td>
<td>• Design Rules</td>
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<tr>
<td>• Computational Fluid Dynamics</td>
<td><strong>Integrated Ceramic Technology</strong></td>
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Advanced Packaging Technology
• Next Generation Packaging Technologies
• Packaging and Integration in BioMEMS
• Packaging Issues for MEMS Devices
• Technologies for Microsystems Components and Substrates
• Packaging Standard for Microsystems
• Environmental issues, Lead Free Systems
• Cost Reduction

Abstracts Deadline: January 18, 2017
Notice of Acceptance: January 31, 2017
Final Manuscripts Due: February 28, 2017

Please send your 500+ word abstract electronically **ON/BEFORE JANUARY 18**, using the on-line submittal form at: [www.imaps.org/abstracts.htm](http://www.imaps.org/abstracts.htm). Full written manuscripts are required on/before February 28. **These proceedings papers will be assigned DOIs, archived into the new IMAPS Microelectronics Research Portal ([www.IMAPSource.org](http://www.IMAPSource.org)), and fully citable.** All papers will be presented and published in English. All speakers are required to pay a reduced registration fee. If you are having problems with the on-line submittal form, please email Brian Schieman bschieman@imaps.org.

Registration & Hotel Reservations *(Full details will be available soon)*
60 min from Kansai Airport by Train
45 min from Kyoto by Train
SYSTEM-IN-PACKAGE (SiP) TECHNOLOGY
Inaugural Conference and Exhibition
June 27-29, 2017 | Doubletree Sonoma Wine Country
Sonoma, California USA
www.IMAPS.org/SiP

General Chair
Nozad Karim
VIP, Amkor Technology

Technical Chair
David Lu
Sr. Dir, Huawei Technology

SiP Executive Team
Rozala Beica
Dir, Dow Chemical

Jan Vardaman
CEO, TechSearch

Simon McElreay
CEO, Semblant

Urmil Ray
Principal Engineer, Qualcomm

Dr. Dongkai Shangguan
CMO, Stats ChipPac

SiP 2017 is the first System-in-Package (SiP) conference fully dedicated to covering all aspects related to SiPs - market trends, system integration/miniaturization, and new technology innovation enablers to meet current and future SiP challenges. This conference will bring the entire SiP supply and design chain from OEM, Fabless, IDM, OSAT, EMS, EDA, silicon foundries, and equipment and material suppliers together under one roof.

Speakers, sponsors, exhibitors and attendees will focus on the insights of SiP technology in the relaxing Sonoma wine country of California, away from big city distractions.

Featuring three full days of technical sessions, panel discussions, exhibitors and local activities, SiP 2017 will provide dynamic learning and technology updates for SiP related trends and new engineering innovations from the industry’s world SiP leaders.

Speaking and presenting opportunities are by invitation from the technical committee.
**Inaugural System in Package (SiP) Technology Conference and Exhibition**

June 27-29, 2017 | Doubletree Sonoma Wine Country

*Learn more at [www.IMAPS.org/SiP](http://www.IMAPS.org/SiP)*

### Technical Program Preview

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<th>June 27</th>
<th>June 28</th>
<th>June 29</th>
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<tr>
<td>SiP market overview, SiP in cellphone teardown of latest cellphones, SiP innovation challenges in mobile applications, active and passive components trends, MEMS and sensors technology trends, SiP package level conformal and compartmental shielding methods, human factor impacts on SiP, and SiP opportunity in China.</td>
<td>RF frontend SiP, connectivity SiP (WiFi, BT, GPS...), medical and wearable SiP, power module, analog SiP, MEMS, sensors and automotive SiP, SiP miniaturization techniques.</td>
<td>Embedded active and passives technology, Integrated Passive Devices (IPD), thin substrate technology, Fan-out solution OSAT and foundry perspectives, water proved Products/NanoCoating technology, assembly process improvement ENS perspective, enhanced new materials for SiP design and EDA tools, EMI shielding equipment.</td>
</tr>
</tbody>
</table>

### Sponsorship and Exhibition Opportunities

Limited event sponsorship opportunities are available and won't last long. Contact Brian Schieman at bschieman@imaps.org to secure your organization’s sponsorship for SiP 2017 before they are filled.

A tabletop exhibition will be held in conjunction with the technical program on June 27th and 28th.

Visit [www.IMAPS.org/SiP](http://www.IMAPS.org/SiP) for up to date conference updates, including the technical program, attendee and exhibitor registration, deadlines, and more. Contact IMAPS HQ to sponsor SiP 2017 or if you have any questions.
International Microelectronics
Assembly and Packaging Society
www.IMAPS.org

Publications
- Membership includes a one-year subscription to *Advancing Microelectronics*
- Access the online Journal of Microelectronics and Electronic Packaging through IMAPSSource
- Complimentary IMAPSSource downloads

Events
- Enjoy discounts on IMAPS events like the International Symposium on Microelectronics and year-round advanced technical workshops
- Convenient, informative webinars
- Speaking and publishing opportunities

Connections
- Local chapter membership and activities
- Post resumes and search for jobs in the JOBS Marketplace
- Participate in discussions through the Memberfuse Community website
- Maintain your professional listing

**IMAPS Source**
*Microelectronics Research Portal*

**START SEARCHING!**
IMAPS members have preferred access to thousands of digital documents and research papers from IMAPS publications, conferences and workshops—all exclusive content focused on the advanced microelectronics packaging industry.

Learn more at IMAPSSource.org!

Visit www.IMAPS.org to join or contact IMAPS at 919-293-5000 to start your membership today!
International Conference and Exhibition on
High Temperature Electronics Network (HiTEN 2017)

July 10-12, 2017
Queen’s College | Cambridge, United Kingdom

Abstract Deadline: January 31, 2017

Conference Chairs:

<table>
<thead>
<tr>
<th>Colin Johnston</th>
<th>R. Wayne Johnson</th>
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<tbody>
<tr>
<td>Oxford University</td>
<td>Tennessee Tech University</td>
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<tr>
<td><a href="mailto:colin.johnston@materials.ox.ac.uk">colin.johnston@materials.ox.ac.uk</a></td>
<td><a href="mailto:wjohnson@tntech.edu">wjohnson@tntech.edu</a></td>
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</table>

HiTEN Conference Focus:
The objective of the HiTEN Conference is to have a unique forum that brings together researchers and practitioners in academia and industry from all over the world. All styles of practical high temperature electronics design and implementation approaches are encouraged, along with a variety of high temperature application areas. Today the main semiconductor focus of HiTEN is silicon and silicon on insulator (SOI). Although, HiTEN is not simply a semiconductor-focused network. HiTEN provides a conduit for the exchange and dissemination of information on all aspects of high temperature electronics. It is a global network with users, suppliers, developers and fundamental researchers dealing in all aspects of High Temperature Electronics.

Abstracts are being requested in the following areas:

- Applications in the Aerospace, Automotive, Oil and Gas, and Geothermal Industries
- Devices and applications
- Novel devices
- ASICs for high temperature applications
- Memories
- Passive components
- Power devices
- Semiconductor materials
- Contacts and metallizations
- Materials
- Packaging and interconnects
- Sealants, adhesives, solders
- Reliability and failure mechanisms
- Lifetime predictions
- Accelerated life testing
- Testing at high temperatures

Those wishing to present a paper at the HiTEN 2017 Conference must submit a ~500 word abstract electronically by January 31, 2017, using the on-line submittal form at: www.imaps.org/abstracts.htm. All abstracts submitted must represent original, previously unpublished work. All speakers are required to pay a reduced registration fee. If your abstract is selected, a Final Manuscript for publication in the Conference Proceedings will be due on May 3, 2017.

The HiTEN Proceedings papers will be ARCHIVED into IMAPS new online research portal/library, IMAPSource® - www.imapsource.org. IMAPSource® currently features all of the IMAPS proceedings, journal papers, magazines, and other conference publications back to 2010. This portal is a fully searchable, user and Google Scholar-friendly database. The software allows for fully exportable citations, improved keyword and Boolean search functionality and customizable alerts, among many other features. The library is indexed by Google Scholar and many key scientific engines/indexes, and growing each day. The 2017 HiTEC papers will be added in May. For now, please visit www.imapsource.org and search. HITEN 2016 proceedings can be found at http://www.imapsource.org/toc/apap/2016/HiTEN and older HiTEC/HiTEN Proceedings can be found in our conference section: http://www.imapsource.org/loi/apap.

Accepted papers may also be considered for publication in the IMAPS Journal of Microelectronics and Electronic Packaging. If you need assistance with the on-line submission form, please email Brian Schieman (bschieman@imaps.org).

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<tr>
<td>Angel</td>
<td>Maurice Lowery</td>
<td><a href="mailto:maurice.lowery@ngc.com">maurice.lowery@ngc.com</a></td>
</tr>
<tr>
<td>Arizona</td>
<td>Jody Mahaffey</td>
<td><a href="mailto:jody@ereach.co">jody@ereach.co</a></td>
</tr>
<tr>
<td>California Orange</td>
<td>Bill Gaines</td>
<td><a href="mailto:William.gaines@ngc.com">William.gaines@ngc.com</a></td>
</tr>
<tr>
<td>Chesapeake</td>
<td>Lauren Boteler</td>
<td><a href="mailto:Lauren.m.boteler.civ@mail.mil">Lauren.m.boteler.civ@mail.mil</a></td>
</tr>
<tr>
<td>Carolinas</td>
<td>Matt Lueck</td>
<td><a href="mailto:mlueck@rti.org">mlueck@rti.org</a></td>
</tr>
<tr>
<td>Central Texas</td>
<td>Rick Prekup</td>
<td><a href="mailto:rprekup@iondsn.com">rprekup@iondsn.com</a></td>
</tr>
<tr>
<td>Cleveland/Pittsburgh</td>
<td>John Mazurowski</td>
<td><a href="mailto:jmazurowski@eoc.psu.edu">jmazurowski@eoc.psu.edu</a></td>
</tr>
<tr>
<td>Empire</td>
<td>Andy Mackie</td>
<td><a href="mailto:amackie@indium.com">amackie@indium.com</a></td>
</tr>
<tr>
<td>Florida</td>
<td>Mike McEntee</td>
<td><a href="mailto:Mike.McEntee@PrecisionTestSolutions.com">Mike.McEntee@PrecisionTestSolutions.com</a></td>
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<td>Sam Forman</td>
<td><a href="mailto:sam.forman@m-coat.com">sam.forman@m-coat.com</a></td>
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<tr>
<td>Indiana</td>
<td>Larry Wallman</td>
<td><a href="mailto:lwallman@sbcglobal.net">lwallman@sbcglobal.net</a></td>
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<tr>
<td>Metro</td>
<td>Scott Baldasserre</td>
<td><a href="mailto:Scott.Baldasserre@aeroflex.com">Scott.Baldasserre@aeroflex.com</a></td>
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<tr>
<td>New England</td>
<td>John Medernach</td>
<td><a href="mailto:jon.medernach@mrsystems.com">jon.medernach@mrsystems.com</a></td>
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<td>Mark Hoffmeyer</td>
<td><a href="mailto:hoffmeyer@us.ibm.com">hoffmeyer@us.ibm.com</a></td>
</tr>
<tr>
<td>Germany</td>
<td>Ernst Eggelaar</td>
<td><a href="mailto:ee@microelectronic.de">ee@microelectronic.de</a></td>
</tr>
<tr>
<td>France</td>
<td>Florence Vireton</td>
<td><a href="mailto:imaps.france@imapsfrance.org">imaps.france@imapsfrance.org</a></td>
</tr>
<tr>
<td>United Kingdom</td>
<td>Andy Longford</td>
<td><a href="mailto:Andy.longford@imaps.org.uk">Andy.longford@imaps.org.uk</a></td>
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<tr>
<td>Taiwan</td>
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<td><a href="mailto:wunyan@itri.org.tw">wunyan@itri.org.tw</a></td>
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<tr>
<td>Italy</td>
<td>Marta Daffara</td>
<td><a href="mailto:info@imaps-italy.it">info@imaps-italy.it</a></td>
</tr>
<tr>
<td>Japan</td>
<td>Orii Yasumitsu</td>
<td><a href="mailto:ORII@jp.ibm.com">ORII@jp.ibm.com</a></td>
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**Brian Schieman, Director of Programs,** (412) 368-1621, bschieman@imaps.org, Development of Society Programs, Website Development, Information Technology, Exhibits, Publications, Sponsorship, Volunteers/Committees

**Ann Bell, Managing Editor,** Advancing Microelectronics, (703) 860-5770, abell@imaps.org, Coordination, Editing, and Placement Management of all pieces of bi-monthly publication, Advertising and Public Relations

**Brianne Lamm, Marketing and Events Manager,** (919) 293-5600, blamm@imaps.org, Corporate Membership, Membership and Event Marketing, Society Newsletters/Emails, Event Management, Meeting Logistics and Arrangements, Hotel and Vendor Management

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<td></td>
<td>1-31-17</td>
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<td>Advanced Technology Workshop on Advanced Packaging for Medical Microelectronics</td>
<td>San Diego, CA</td>
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<td>System-in-Package Technology Conference and Exhibition 2017</td>
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<td>JUNE</td>
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<td>JULY</td>
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